Fully differential amplifier design in high-speed data acquisition systems

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Introduction

Signal integrity is paramount in high-speed data acquisition systems in applications such as communications, imaging, instrumentation, video, and multimedia; and many engineers are finding the solution to be fully differential signal processing. The advantages are inherent in the architecture:

- External common-mode noise sources (from the power supply and other circuitry) are rejected by the differential nature of the architecture.
- Even-order harmonics tend to cancel.
- The required voltage swing for each differential output is only half that of its single-ended counterpart, thus reducing distortion and easing power-supply requirements.

All high-performance, high-speed data converters are now using differential inputs to enhance performance. Most often, amplification, impedance matching, filtering, and level shifting are required in front of the ADC. Not only are fully differential op amps ideal for these functions, but they also greatly simplify the design task.

Fully differential signal processing represents a paradigm shift in the design process that has some nuances that are not obvious. The purpose of this article is to highlight these design issues and show how to deal with them.

TI's THS45xx family of fully differential op amps is designed with a combination of high bandwidth, low distortion, and low noise that makes them suitable for interfacing to 12-bit and 14-bit high-speed data converters.

The data acquisition problem can be broken into four parts as depicted in Figure 1—the overall system requirements, the source interface, the amplifier's role or function, and the ADC interface. The design strategy is to design the interfaces between the signal source and the ADC with the proper amplifier function to realize the system requirements.

Source to amplifier interface

There are two general categories of sources that need to be considered: single-ended and differential. Single-ended sources are most often referenced to ground, whereas differential sources are not. The following discussion considers the design issues when a fully differential op amp is used in both situations.

In amplifier design, the input impedance of the amplifier is typically of prime concern; and this holds true for fully differential op amps.

Interfacing to a single-ended, ground-referenced source

If the source is single-ended and referenced to ground, a fully differential op amp can be used to convert the signal to differential (and level shift) as shown in Figure 2. V_S is the input source, with associated output impedance R_S.

Balance and gain

It is important to maintain balance in the amplifier by setting $R_{F1} = R_{F2}$ and $R_{G1} + R_S = R_{G2}$. The effect of mismatching the resistors is discussed later.

The differential output voltage is given by

$$V_{OD} = \frac{2(V_S)(1-\beta_1)+2V_{OCM}(\beta_1-\beta_2)}{(\beta_1+\beta_2)}, \text{ where}$$

$$\beta_1 = \frac{R_{G1}+R_S}{R_{G1}+R_S+R_{F1}} \text{ and } \beta_2 = \frac{R_{G2}}{R_{G2}+R_{F2}}.$$

If the resistor ratios are matched, the ratio of single-ended input to differential output gain is given by

$$\frac{R_{F2}}{R_{G2}} = \frac{R_{F1}}{R_{G1}+R_S}.$$

Note that the source resistance affects the gain of the amplifier.

Figure 1. The data acquisition problem

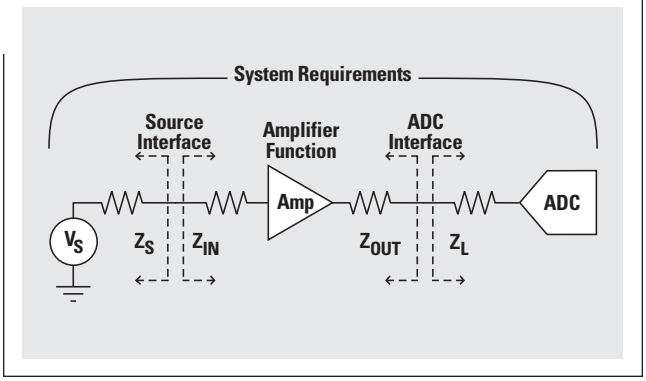
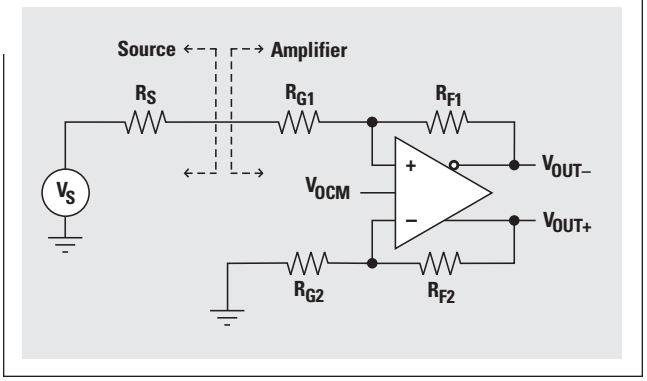


Figure 2. Single-ended source



The input impedance equals

$$\frac{R_{G1}}{1-\frac{K}{2\times(1+K)}},$$

where K is the gain of the amplifier. At high gain this converges to $2 \times R_{G1}$.

Input common-mode voltage

It is important not to violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming that the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most; so finding the voltage at one input pin will determine the input common-mode voltage range to the op amp. In Figure 2 it is easiest to find the voltage at the negative input pin of the op amp, given by

$$V_{OUT+}\times\frac{R_{G2}}{R_{G2}+R_{F2}}.$$

To determine the required V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

The input common-mode voltage range is more likely to present a problem when the amplifier is operated with single-supply voltages and higher gains. For instance, take two amplifiers, each configured as shown in Figure 2, operating from +5 V with V_{OCM} = +2.5 V and the differential output voltage V_{OD} = 2 $V_{p–p}$. (Details on V_{OCM} are covered later under "Interfacing to the ADC.") One amplifier has a gain of 1 and the other has a gain of 10.

- With gain = 1, the required voltage range is 1 to 1.5 V—fairly relaxed limits.
- With gain = 10, the required voltage range is 0.18 to 0.27 V. The amplifier's V_{ICR} must go very near the negative supply voltage rail.

For this type of application, the IC designer must pay special attention to ensure that the op amp's V_{ICR} includes the negative rail. Take, for example, the THS4501; special level-shifting circuitry is used so that V_{ICR} can actually go below the negative rail.

Interfacing to a differential source

A differential input source is depicted in Figure 3. V_S is the differential input source, with associated output impedances R_{S1} and R_{S2}.

Balance and gain

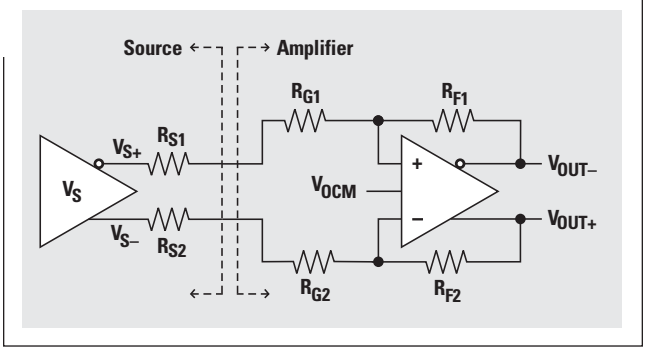
Again, it is important to maintain balance in the amplifier by setting $R_{F1} = R_{F2}$ and $R_{G1} = R_{G2}$. The input source must also be balanced with $R_{S1} = R_{S2}$. The effect of mismatching the resistors is discussed later.

The differential output voltage is given by

$$V_{OD}=\frac{2\left[(V_{S+})(1-\beta_1)-(V_{S-})(1-\beta_2)\right]+2V_{OCM}(\beta_1-\beta_2)}{(\beta_1+\beta_2)},$$

$$\text{where } \beta_1=\frac{R_{G1}+R_{S1}}{R_{G1}+R_{S1}+R_{F1}} \text{ and } \beta_2=\frac{R_{G2}+R_{S2}}{R_{G2}+R_{S2}+R_{F2}}.$$

Figure 3. Differential source



If the resistor ratios are matched, the ratio of differential input to differential output gain is given by

$$\frac{R_{F1}}{R_{G1}+R_{S1}}=\frac{R_{F2}}{R_{G2}+R_{S2}}.$$

Note that the source resistance is included in the gain equation again. The input impedance is equal to $R_{G1} + R_{G2}$.

Input common-mode voltage

Again, it is important not to violate the input common-mode voltage range (V_{ICR}) of the op amp. The analysis is not quite as easy as with a single-ended input, but still we can analyze one input pin and assume that the other has the same voltage due to amplifier action.

If we treat the positive input as a summing node, the voltage is given by

$$\left(V_{OUT-}\times\frac{R_{G1}+R_{S1}}{R_{G1}+R_{S1}+R_{F1}}\right)+\left(V_{S+}\times\frac{R_{F1}}{R_{G1}+R_{S1}+R_{F1}}\right).$$

To determine the required V_{ICR} of the op amp, the voltage at the positive input is evaluated at the extremes of $V_{OUT–}$ and V_{S+}.

The input common-mode voltage range is more likely to present a problem when the source has a high or low common-mode voltage and the amplifier has high gain.

Let's look at an example of interfacing a CCD sensor to an ADC. The CCD sensor has 500 mV differential output centered around +9 V. The amplifier has a gain of 2 powered by +9 V referenced to ground, and V_{OCM} = +2.5 V; so the amplifier's output is 1 $V_{p–p}$ centered around +2.5 V. The voltage range at the positive input to the op amp is +7.17 to +7.33 V. This is close to the positive rail, but not so close as to present a problem. If the sensor's output were lower and a high gain were required, the voltage range would approach the positive rail and the op amp might not work properly.

If the common-mode voltage of the source can be adjusted, centering it within the amplifier's V_{ICR} provides for optimal performance.

The impact of mismatched resistors

As stated earlier, the resistors need to be matched to maintain balance in the amplifier. What happens if the resistors are not matched?

In the following discussion:

- R_F is the feedback resistor from the output to the input on either side of the op amp; i.e., R_{F1} or R_{F2}.
- R_G is the resistance from the source to the input on either side of the op amp and includes the source resistance; i.e., $R_{G1} + R_S$, $R_{G1} + R_{S1}$, or $R_{G2} + R_{S2}$.

If the resistor ratios (R_F/R_G) are mismatched between the two sides of the op amp, the gain will vary proportionately to the mismatch, being a little higher than the average of the two sides. The internal common-mode feedback circuit will still maintain the output common-mode voltage equal to V_{OCM}. The output signals therefore remain balanced, swinging plus and minus with reference to V_{OCM}.

Ratio matching errors in the external resistors will degrade the circuit's ability to reject input common-mode noise. A 1% mismatch will result in about a 46-dB input CMRR.

Similarly, if the dc common-mode voltages at the input and output are different, matching errors will result in an offset in the differential output voltage. For the example given ($G \approx 1$, 1% mismatch, ground-referenced input signal, and $V_{OCM} = 2.5$ V), the output offset equals 12 mV.

To further illustrate the impact of mismatched resistors, the node voltages of the circuits shown in Figures 2 and 3 are analyzed with a 10% mismatch:

- Table 1 shows the effect of mismatched resistors in the single-ended source amplifier circuit shown in Figure 2: $R_{F1} = R_{F2} = R_{G2}$, but $R_{G1} + R_S = 0.9(R_{G2})$, and V_{OCM} = +2.5 V. Since the source's common-mode voltage is different from the output common-mode voltage of the op amp, the mismatch causes an offset in the differential output ($V_{OD} = -0.135$) with zero input. The gain is 0.946 + 0.135 = 1.081.
- Table 2 shows the effect of mismatched resistors in the differential source amplifier circuit shown in Figure 3: $R_{F1} = R_{F2} = R_{G2} + R_{S2}$, but $R_{G1} + R_{S1} = 0.9(R_{G2} + R_{S2})$; common-mode voltage of the source = +2.5 V; and V_{OCM} = +2.5 V. With the common-mode voltage of the source equal to the output common-mode voltage of the amplifier, the mismatch does not cause an offset in the differential output ($V_{OD} = 0.000$) with zero input. The gain of the amplifier is 1.054.

V_{OCM} is used to set the op amp's output to the common-mode voltage of the ADC's input.

At dc and lower frequencies, if the ratio R_F/R_G is equal between the two sides, the amplifier will be balanced. However if $R_{F1} \neq R_{F2}$ (or $R_{G1} \neq R_{G2}$), parasitic capacitance will unbalance the op amp at higher frequencies. For best operation, the feedback (and input) resistors should be equal.

Table 1. Effect of 10% resistor mismatch with a single-ended, ground-referenced source

V_S	V_{OCM}	V_{OUT+}	V_{OUT-}	V_{OD}	GAIN
0	2.5	2.432	2.568	–0.135	—
1	2.5	2.973	2.027	0.946	1.081

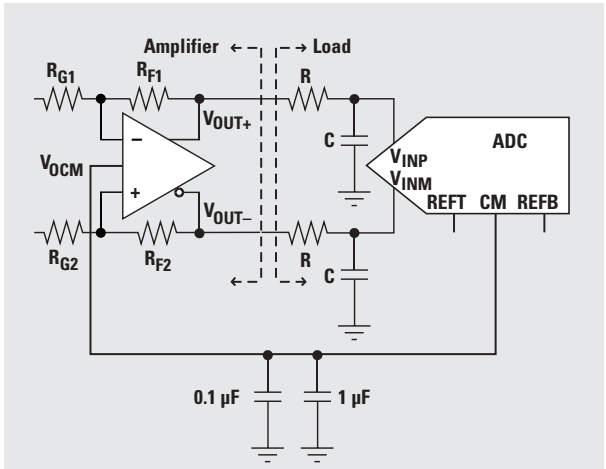
Table 2. Effect of 10% resistor mismatch with a differential source

V_{S+}	V_{S-}	V_{OCM}	V_{OUT+}	V_{OUT-}	V_{OD}	GAIN
2.5	2.5	2.5	2.500	2.500	0.000	—
3	2	2.5	3.027	1.973	1.054	1.054

Interfacing to the ADC

A primary function of the amplifier is to process the incoming signal so that it is at the correct bias point and amplitude to get optimal performance from the ADC. Obviously, it must have the bandwidth and ac performance to do this without compromising the signal. A simple, fully differential op amp-to-ADC interface is shown in Figure 4. The primary design issues in the interface are the load the amplifier drives and setting the proper output common-mode voltage.

Figure 4. Fully differential op amp-to-ADC interface

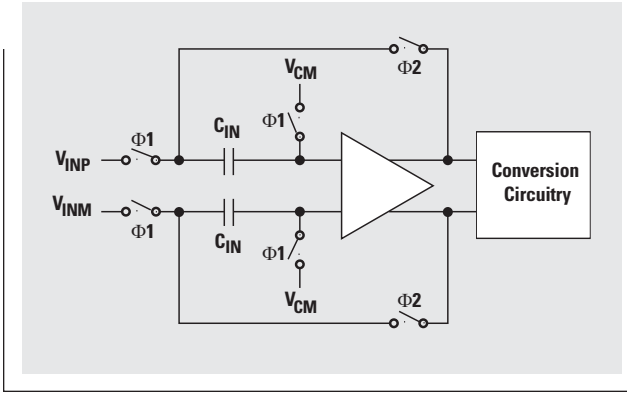


ADC input

Figure 5 shows a functional diagram of a high-performance ADC input. During **Φ**1, the input capacitors are charged to the difference between the input and V_{CM} (this is the sampling period—typically half the clock period). During **Φ**2, the charge is transferred to the conversion circuitry, where it is converted into the digital output.

It is almost universally recommended that a resistor and capacitor be used between the op amp's output and the ADC's input, as shown in Figure 4.

Figure 5. High-performance ADC input



This resistor-capacitor (RC) combination has multiple functions:

- The capacitor is a local charge reservoir for the ADC.
- The resistor isolates the amplifier from the ADC.
- In conjunction, they form a low-pass noise filter.

Charge reservoir

During the sampling phase, current is required to charge the ADC's input sampling capacitors. If external capacitors are placed directly at the input pins, most of the current is drawn from them. They are seen as a very low-impedance source. They can be thought of as serving much the same purpose as a power-supply bypass capacitor—to supply transient current, with the amplifier then providing the bulk charge.

Typically, a low-value capacitor in the range of 10 to 100 pF should provide the required transient charge reservoir.

Isolation

All this capacitance and the switched-capacitor input nature of the ADC is one of the worst loading scenarios that a high-speed amplifier will encounter. The resistor provides a simple means of isolating the associated phase shift from the feedback network and maintaining the phase margin of the amplifier.

Typically, a low-value resistor in the range of 10 to 100 Ω should provide the required isolation.

Noise filter

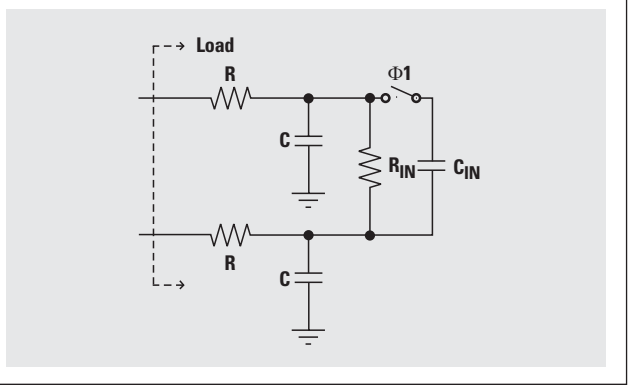
Together, R and C form a real pole in the s-plane located at the frequency

$$f_P = \frac{1}{2\pi RC}.$$

Placing this pole at about 10× the highest frequency of interest ensures that it has no impact on the signal.

Since the resistor is typically a small value, it is very bad practice to place the pole at (or very near) frequencies of interest. At the pole frequency, the amplifiers drive a load whose magnitude is $\sqrt{2} \times R$. If R is only 10 Ω or so, the amplifier is very heavily loaded above the pole frequency and will generate excessive distortion.

Figure 6. ADC input load model



Amplifier loading

With the RC combination at the input of the ADC, the amplifier drives a load that can be modeled as shown in Figure 6. Sometimes the input impedance of the ADC is such that $R_{IN} >> R$ and $C_{IN} << C$. In such cases the internal values can be ignored, and the input model is simply the external RC combination. For proper performance analysis, the amplifier should be tested with this load.

The output impedance of the op amp is important in considering the effect of output loading. Due to negative feedback, the output impedance of the op amp is very low over most of its bandwidth.

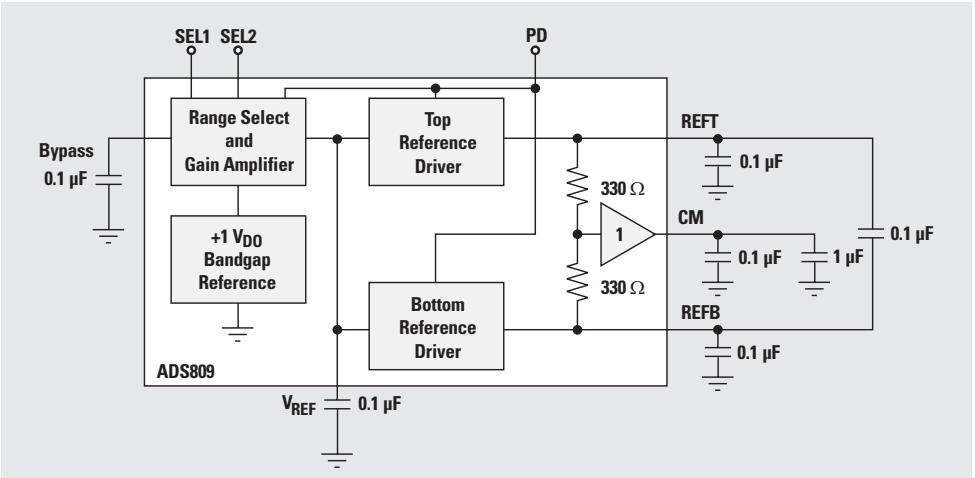
$$Z_O = \frac{z_O}{1 + A_F\beta},$$

where Z_O is the closed-loop output impedance; z_O is the open-loop output impedance; A_F is the frequency-dependent, open-loop gain of the amplifier; and β is the feedback factor

$$\beta = \left(1 + \frac{R_F}{R_G}\right).$$

At low frequencies the product $A_F\beta$ is very large and the output impedance → 0. The open-loop gain falls in proportion to the frequency. It is important, therefore, to use an amplifier at frequencies where $A_F\beta$ is very large to minimize the effect of the voltage divider between the output impedance and the load.

Figure 7. ADS809 internal reference circuit and recommended bypass scheme



ADC reference and input common-mode voltages

Figure 7 shows the internal reference circuit that is published in Reference 1. The reference voltages, REFT and REFB, determine the input voltage range of the converter. The voltage CM is

at the midpoint between REFT and REFB. The input signal to the ADC must swing symmetrically about CM to utilize the full dynamic range of the converter. This means that the output common-mode voltage of the amplifier must match this voltage.

The V_{OCM} input on the THS45xx is provided specifically for this purpose. Internal circuitry forces the output common-mode voltage to equal the voltage applied to V_{OCM}. Thus, V_{OUT+} and V_{OUT-} swing symmetrically about V_{OCM}. In many cases, all that is required is to tie CM to V_{OCM} with bypass capacitor(s) to ground (typically 0.1 µF to 10 µF).

Figure 8 shows a simplified schematic of the V_{OCM} input on the THS45xx. With V_{OCM} unconnected, the resistor divider sets the voltage halfway between the power-supply voltages. The equation

$$I_{Ext} = \frac{2V_{OCM} - (V_{CC+} + V_{CC-})}{50\ k\Omega}$$

shows how to calculate the current required from an external source to overdrive this voltage. Internal circuitry is used to cancel the bias current (I_{EA}) drawn by the V_{OCM} error amplifier. It is easy to see that, if the desired V_{OCM} is halfway between the power-supply voltages (as in a single +5-V-supply application), no external current is required. On the other hand, if the amplifier is being powered from ±5 V and the desired V_{OCM} is +2.5 V, the external source will need to supply 100 µA. Depending on the CM output drive from the ADC, a buffer may be required to supply this current.

Most high-performance ADCs using differential inputs have an output for setting the common-mode voltage of the drive circuit. Different manufacturers use different names for it—CM, REF, V_{REF}, V_{CM}, or V_{OCM}. Whatever it is called, there are two important things to remember: (1) Make sure it has enough output drive current if V_{OCM} is not at midrail; and (2) use bypass capacitors to reduce common-mode noise.

Figure 8. V_{OCM}

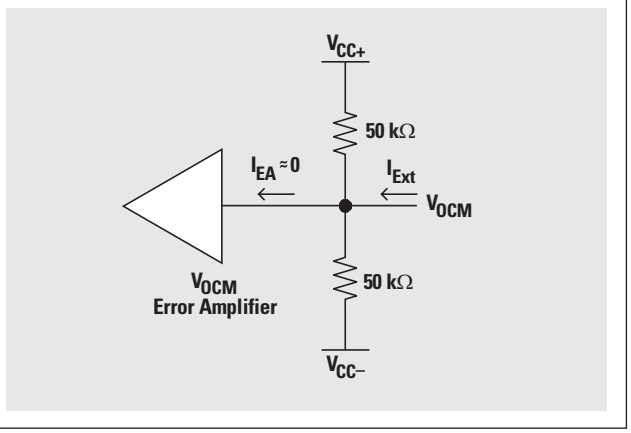


Figure 9. Single real-pole low-pass filter

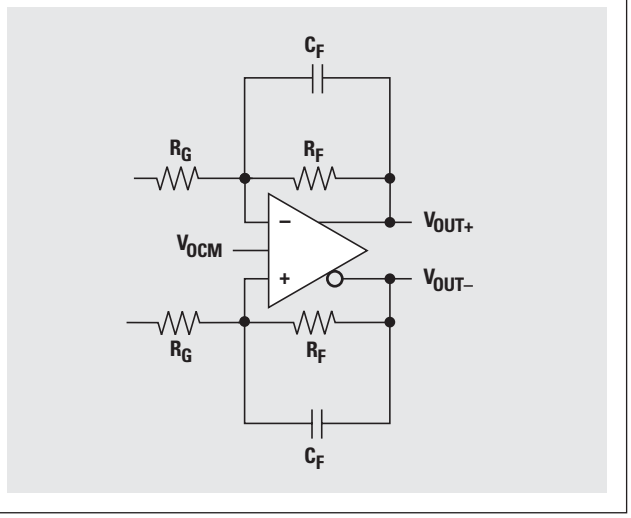
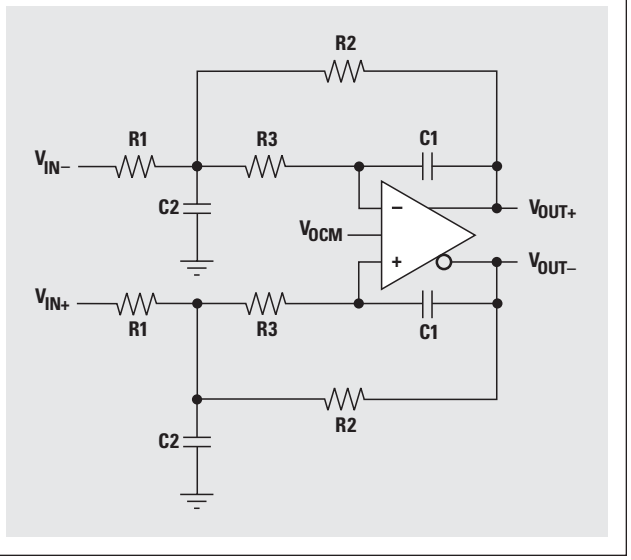


Figure 10. Second-order low-pass filter



Amplifier function

We have already discussed important amplifier design issues like setting the gain when interfacing to the source, and level shifting when interfacing to the ADC. Another common function the amplifier performs is filtering out-of-band signals. The following considers active low-pass filter design with fully differential op amps.

Single real pole

An active low-pass filter is made by adding capacitors of equal value across each feedback resistor, as shown in Figure 9. In this configuration, the op amp will attenuate frequencies above

$$f_P = \frac{1}{2\pi R_F C_F}.$$

The pole is a real pole in the s-plane.

Complex pole pairs

The classic filter types like Butterworth, Bessel, Chebyshev, etc. (second-order and greater), cannot be realized by real poles; they require complex poles. The multiple feedback (MFB) topology is used to create a complex pole pair and is easily adapted to fully differential op amps, as shown in Figure 10.

This is an active second-order low-pass filter, and the transfer function is

$$\frac{V_{OUT}}{V_{IN}} = \left[\frac{K}{-\left(\frac{f}{FSF \times f_C}\right)^2 + \frac{1}{Q}\left(\frac{jf}{FSF \times f_C}\right) + 1} \right],$$

where $V_{OUT} = (V_{OUT+}) - (V_{OUT-})$ and $V_{IN} = (V_{IN+}) - (V_{IN-})$,

$$K = \frac{R2}{R1}, \; FSF \times f_C = \frac{1}{2\pi\sqrt{R2R3C1C2}}, \text{ and}$$

$$Q = \frac{\sqrt{R2R3C1C2}}{R3C1 + R2C1 + KR3C1}.$$

K sets the pass band gain, f_C is the cut-off frequency of the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2}, \text{ and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2 \times Re},$$

where Re is the real part and Im is the imaginary part of the complex pole pair.

For design purposes, setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in

$$FSF \times f_C = \frac{1}{2\pi RC\sqrt{n \times m}} \text{ and } Q = \frac{\sqrt{mn}}{1 + m(1 + K)}.$$

The corner frequency, gain, and filter type set FSF, f_C, K, and Q. With these goals in mind, the designer can design the filter most easily in the following sequence:

1. Choose a capacitor ratio, n, that corresponds to common capacitor values for C1 and C2.
2. Use the ratio n determined in Step 1 and the equation

$$Q = \frac{\sqrt{mn}}{1 + m(1 + K)}$$

to see if there is a value for m that results in the desired Q of the filter. If the desired Q is not attainable, go back to Step 1 and choose a different capacitor ratio.

3. When suitable ratios for m and n are found, calculate R2 with the equation

$$R2 = \frac{1}{FSF \times f \times 2\pi C\sqrt{n \times m}},$$

and find the nearest standard resistor value.

4. Pick the nearest standard resistor value for R3 = mR2.
5. R1 is determined from

$$R1 = \frac{R2}{K}.$$

Pick the nearest standard resistor value.

6. Double check that the standard resistor values result in the desired gain and filter response. If not, some "tweaking" of the values may have better results.

A spreadsheet is an invaluable tool for doing these calculations.

System requirements

In the past, traditional amplifier specifications like signal-to-noise ratio, harmonic distortion, spurious free dynamic range, etc., have been used to define the quality of a system. These specifications were derived from system requirements like resolution, sensitivity, bit error rate, and the like.

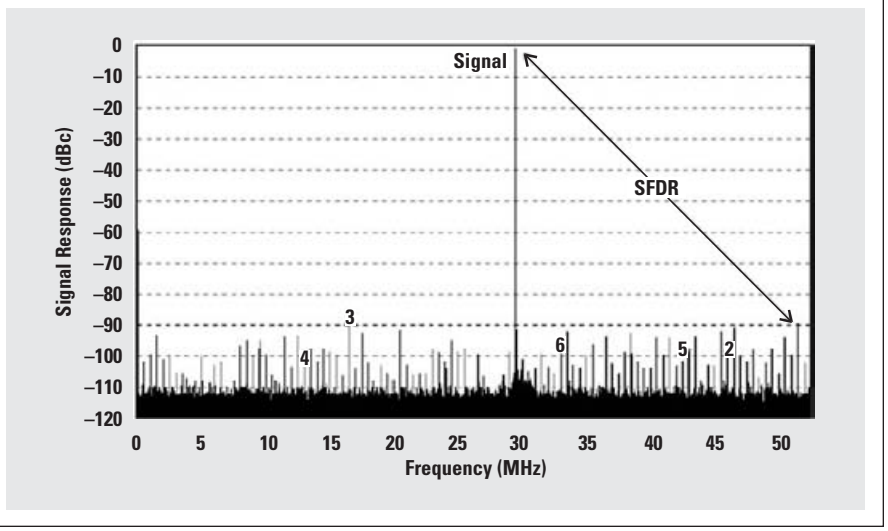
In the design of data acquisition systems today, the focus is on choosing the data converter. In high-speed, high-performance data acquisition systems, ac performance factors such as spurious free dynamic range (SFDR), effective number of bits (ENOB), and sampling rate drive the decision-making process, with dc errors being less important.

To determine the overall ac performance, the designer must analyze the system as a whole. The following discussion shows how to combine SFDR and ENOB to analyze the overall system performance.

SFDR

Spurious free dynamic range (SFDR) is the difference between the signal and the strongest spur, and is usually given in dBc. Figure 11 shows a fast Fourier transform (FFT) for a high-performance ADC. The spurious responses that are harmonics of the input signal are noted with their harmonic order (2–6). These harmonics are attributed to the nonlinearities in the input track-and-hold amplifier. In Figure 11 there is also a large number of spurs that are not harmonics of the input signal. These are attributed to the sampling process. Note that in Figure 11 the SFDR of the ADC is set by a spur that is not a harmonic of the signal.

Figure 11. FFT of a high-performance ADC



To determine the SFDR of the amplifier and ADC as a system, the output spectrum of the amplifier is overlaid on that of the ADC. The fully differential amplifier driving the ADC will have only spurs that are harmonics of the signal; so only harmonics of the signal will align and need to be added together.

How do we go about adding the harmonic spurs from two different sources? Since the electrical distances are not the same, resulting in random phase differences, the sources are added by their powers.

The FFT of the ADC's output is taken at a specified level, typically –1 dBFS. The amplifier's harmonics should also be measured at this level. Then the harmonic amplitudes of the amplifier and the ADC are converted from dBc to scalar quantities and added together. The result is converted back to dBc. The equation form is

$$HDx_{Combined}(dBc) = 10 \times \log_{10}\left[10^{\left(\frac{HDx\_Amp}{10}\right)} + 10^{\left(\frac{HDx\_ADC}{10}\right)}\right],$$

where HDx_Amp and HDx_ADC are the harmonic spurs in dBc from the amplifier and ADC.

Remembering some simple relationships helps to analyze the system quickly without doing any math. If the harmonics are equal, add 3.01 dB. If there is more than a 10-dB difference between the harmonic levels, ignoring the smaller one results in only a small error.

In a linear amplifier, the second and third harmonics normally are the most significant spurs and most likely will be the only points that need to be evaluated in this manner.

ENOB

Effective number of bits (ENOB) is not a traditional amplifier specification, but amplifiers can be attributed with an ENOB specification to compare them more directly with ADC specifications.

In an ADC, quantization noise sets a theoretical limit on the dynamic range that can be attained with a given number of bits. ENOB is a means of quantifying the effect of distortion and other noise sources within real ADCs that limit their dynamic range.

$$ENOB = \frac{SINAD(dBc) - 1.76}{6.02}.$$

The signal-to-noise ratio and total harmonic distortion added together (SINAD) is expressed as a positive number. To specify ENOB for an amplifier, measure the signal-to-noise ratio and harmonics at the ADC's specified input level, typically –1 dBFS. To get SINAD, add the signal-to-noise and harmonic levels by their powers in dBc. The procedure is the same as previously described for adding harmonics; convert from dBc to scalar quantities, add together, and convert the result back to dBc.

The ENOB of the combined system can be calculated by adding the SINAD of the amplifier and ADC together by their powers.

If the ENOB of the amplifier equals that of the ADC, the SINAD numbers are also equal. In this case, the combined SINAD is 3.01 dB lower, and the combined ENOB is 0.5 bit less.

Conclusion

We have considered the design of fully differential op amps in high-speed data acquisition systems, including the source/amplifier interface, amplifier/ADC interface, amplifier function, and overall system requirements.

Following are the key points to remember.

Source interface

- Input impedance:
  - With a single-ended source, $Z_{IN} = \frac{R_{G1}}{1 - \frac{K}{2 \times (1+K)}}$.
  - With a differential source, $Z_{IN} = R_{G1} + R_{G2}$.
- Include source impedance in the gain calculation.
- Ensure that the amplifier has the required input common-mode voltage range.

ADC interface

- Output impedance of the amplifier at low frequency is very low, $\rightarrow 0$, but can become a concern at higher frequencies.
- The RC combination between amplifier and ADC
  - provides isolation,
  - serves as a local charge reservoir, and
  - acts as a low-pass noise filter.
- The V_{OCM} pin allows an easy means of setting the output common-mode voltage. Ensure that the source has the required drive if V_{OCM} is not set to midrail.

Amplifier function

- Include source impedance in the gain calculation.
- Level shifting is accomplished via the V_{OCM} pin.
- The design can easily accommodate active first- or second-order low-pass filter function.

System requirements

- Add common spurs by their powers.
- If the largest spurs are equal and they align, then SFDR is degraded by 3.01 dB.
- If the ENOBs are equal, then ENOB is degraded by 0.5 bit.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "12-Bit, 80-MHz Sampling Analog-to-Digital Converter," ADS809 Data Sheet	sbas170

Related Web sites

www.ti.com/sc/device/ADS809
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