Worst-case design of op amp circuits

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Introduction

Building reliable hardware requires all component tolerances to be accounted for during the design stage. Worst-case design techniques do not change the basic transfer equations for an op amp circuit; rather, the components assume a wide range of values that lead to a corresponding range of output voltages. This becomes complicated because active and passive components have different error sources and tolerances.

The sample design used as a teaching aid is a single-stage op amp configured as an amplifier: the circuit is designed, the effects of passive components are calculated, the effects of steady state versus drift errors are discussed, and methods of eliminating errors are discussed. Op amps have internal error sources, but they are left as the subject of another article because component drift tolerances almost always overshadow op amp internal error sources. Circuit equations not developed here are taken from Reference 1.

Passive component and reference tolerances

Resistors are the fundamental component in all circuits, so we consider their tolerances in detail. Resistors are specified with a purchase tolerance (P) expressed as a percentage; for example, 0.5%, 1%, 2%, 5%, and 10% are popular purchase tolerances. The purchase tolerance guarantees that the resistor is within its nominal value when you receive it. As soon as the resistor is used in an assembly, it starts to change value; and, because the resistor value usually is close to the limit of the purchase tolerance, its value changes beyond the purchase tolerance. External stresses like temperature, aging, pressure, humidity, mounting, sunlight, dust, and soldering force component values to change over time.

Resistor tolerances are estimated in Table 1. Notice that the purchase tolerance is kept separate from the drift tolerance; this is because the purchase tolerance can be adjusted, but the drift tolerance occurs during normal operation and causes errors unless calibration before measurement (CBM) is done.

The resistor manufacturing process determines the drift tolerance. The tighter-tolerance resistors are manufactured with more stable, controlled methods and with materials that resist drift. Excessive drift results in manufacturing rejects, and the tight process/material control techniques that minimize drift in the factory also minimize drift in the field.

It is common to represent a resistor as R_1 or R_2; and, keeping this nomenclature, we calculate the purchase and/or drift tolerance as $(1 \pm 0.01P \pm 0.01D)R_1$ to obtain the worst-case resistor value. The purchase and drift tolerances are given as percentages, and the ±0.01 factor converts them to actual values. Purchase and drift tolerances are positive or negative depending on external conditions, manufacturing methods, materials, and internal stresses. Individual resistor tolerances must be represented as positive or negative (whichever yields the worst-case calculation), unless the data sheet specifically states that all resistors drift in a prescribed direction. When calculating the absolute worst-case maximum value for a 5% $R_1 = 10\ k\Omega$, use $(1 + 0.01P + 0.01D)R_1 = (1 + 0.05 + 0.05)R_1 = 1.1R_1 = 11\ k\Omega$. The absolute worst-case minimum value for this resistor is $(1 - 0.01P - 0.01D)R_1 = (1 - 0.05 - 0.05)R_1 = 0.9R_1 = 9\ k\Omega$.

Capacitor tolerances, while not discussed in detail here, are handled in the same manner. Capacitor tolerances vary much more than resistor tolerances because of the radically different methods used to manufacture capacitors. Electrolytic capacitors often have purchase tolerances of +80, –20%; but some glass and NPO ceramic capacitors have purchase tolerances of 1%. In general, it is best to triple all capacitor tolerances unless you check the manufacturer's data sheets and determine otherwise. This errs on the conservative side but is good judgment when you haven't done your homework.

Reference voltages can be derived from reference ICs, zener diodes, signal diodes, or power supplies. The reference voltage has four errors: initial tolerance, temperature drift, load sensitivity, and noise. Initial tolerance is comparable to purchase tolerance in a resistor and is treated in

Table 1. Resistor tolerances

PURCHASE TOLERANCE (P) (%)	DRIFT TOLERANCE (D) (%)	TOTAL TOLERANCE (T) (%)
0.5	0.25	0.75
1	2	3
2	2	4
5	5	10
10	15	25

the same manner. Temperature drift, load sensitivity, and noise must be calculated for the environmental conditions to which the finished product will be exposed; furthermore, you must assume that these worst-case conditions exist simultaneously. Obviously, these three error sources are cumulative drift errors. Remember, the reference voltage acts like the command input to a servo and, if the circuit functions correctly, follows command input to the best of its ability.

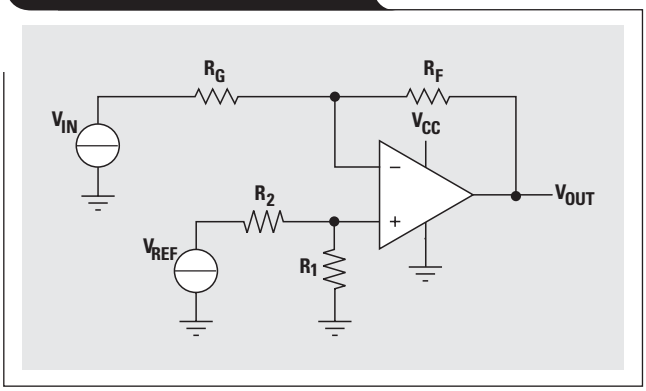
Design of the nominal circuit and resistor selection

The equation for the amplifier required by this design is

$$V_{OUT} = -16\,V_{IN} + 10.4. \quad \textbf{(1)}$$

The circuit that conforms to this equation is shown in Figure 1.

Figure 1. Amplifier circuit



Equation 1 is the general form of a transfer function; it is repeated with the op amp resistors as parameters in Equation 2.

$$V_{OUT} = -\left(\frac{R_F}{R_G}\right)V_{IN} + V_{REF}\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) \quad \textbf{(2)}$$

Comparing terms in Equations 1 and 2 yields Equations 3 and 4.

$$|16| = \frac{R_F}{R_G} \quad \textbf{(3)}$$

$$b = V_{REF}\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{R_F+R_G}{R_G}\right) \quad \textbf{(4)}$$

All resistors used in this sample design are 1%, and the reference voltage is 2.5 V with P = 1% and D = 2%. Equation 3 establishes the ratio of R_F to R_G as 16:1; and this ratio is satisfied by a large number of discrete resistor values like 16 Ω and 1 Ω, 160 Ω and 10 Ω, 1600 Ω and 100 Ω, or 160 kΩ and 10 kΩ. The designer establishes the impedance of the design by picking a resistor value that scales the remaining values. Low-value resistors draw more current, have better frequency response, and load the op amp; while high-value resistors are noisy and susceptible to printed circuit board leakage. Let us pick 10 kΩ for R_G, and then R_F = 160 kΩ. These resistor values are a good compromise because they are in the middle of the impedance range; if another resistor selection must be made later they can be selected higher or lower to satisfy network interactions. Equation 4 is algebraically manipulated to yield Equation 5.

$$R_2 = \left[\frac{V_{REF}(R_F+R_G)}{bR_G} - 1\right]R_1 = 3.086R_1 \quad \textbf{(5)}$$

Let R_1 = 12.4 kΩ and R_2 = 38.3 kΩ. R_1 is selected such that the parallel value of $R_1 \| R_2$ equals the parallel value of $R_F \| R_G$. Equal parallel resistor network values inserted in each amp lead create equal common-mode voltages from the bias currents, and the op amp rejects common-mode voltage very well. Also, the 1% purchase tolerance and the flexibility of two different scaling resistors (R_1 and R_G) enables the choice of exact resistor ratios, so recalculating the transfer equation using the selected resistor values yields $V_{OUT} = -16\,V_{IN} + 10.39$.

Worst-case analysis

Equation 2 is rewritten as Equation 6 (see below), which includes the total tolerance and has been written to obtain the maximum value of the transfer equation.

The purchase tolerance can be adjusted with a potentiometer or a DAC/variable gain amplifier combination. It is useful to know how much adjustment is required to account for the purchase tolerance, so the purchase tolerance is substituted for the total tolerance in Equation 7 (see below).

Calculation of the tolerances and potentiometer values

The maximum and minimum transfer functions (for P = 1%) are

$V_{OUT(MAXP)} = -16.32\,V_{IN} + 10.86$ and **(8)**

$V_{OUT(MINP)} = -15.68\,V_{IN} + 9.947$. **(9)**

$$V_{OUT(MAXT)} = -V_{IN}\left[\frac{(1+T)R_F}{(1-T)R_G}\right] + (1+T)V_{REF}\left[\frac{(1+T)R_1}{(1+T)R_1+(1-T)R_2}\right]\left[\frac{(1+T)R_F+(1-T)R_G}{(1-T)R_G}\right] \quad \textbf{(6)}$$

$$V_{OUT(MAXP)} = -V_{IN}\left[\frac{(1+P)R_F}{(1-P)R_G}\right] + (1+P)V_{REF}\left[\frac{(1+P)R_1}{(1+P)R_1+(1-P)R_2}\right]\left[\frac{(1+P)R_F+(1-P)R_G}{(1-P)R_G}\right] \quad \textbf{(7)}$$

Notice that the slope tolerance is 2%, double the resistor purchase tolerance. This doubling occurs because the tolerances occur in a pure resistor ratio (no addition or subtraction). The intercept has two resistor ratios multiplied by a reference tolerance. The intercept resistor error is 3.36% rather than 4% for two reasons: (1) The resistors are not in a pure ratio; and (2) there are two resistor ratios multiplied times the reference voltage. You can never assume that x% resistors yield a 2x% tolerance unless they are used in a pure ratio.

The purchase tolerance error can be plus or minus, so the prudent designer doubles the error tolerance when calculating the value of a potentiometer to account for a double tolerance; and, because potentiometers have large errors, he usually triples the error tolerance. The slope error is now 6%. The potentiometer is in the R_G circuit, so its value is calculated as 0.06(10 kΩ) = 600 Ω. Since this potentiometer value is hard to find, a 1-kΩ potentiometer is used in the design. The value of R_G is reduced by half the potentiometer value to 9.53 kΩ. When the potentiometer is at zero value, the slope is –16.79 V; and when the potentiometer is at full value, the slope is –15.19 V. The full range of required values is therefore available with this adjustment.

The combined intercept tolerance (reference and resistors) is 4.4%, and tripling that tolerance yields 13.2%. The potentiometer is in the R_1 circuit, so its value is calculated as 0.132(12.4 kΩ) = 1.64 kΩ. Since this potentiometer value is hard to find, a 2-kΩ potentiometer is used in the design. The value of R1 is reduced by half the potentiometer value to 11.3 kΩ. When the potentiometer is at zero value, the intercept is 9.68 V; and when the potentiometer is at full value, the intercept is 10.95 V. The full range of required values is therefore available in the adjustment. The final circuit is shown in Figure 2.

The potentiometer selection procedure described here is adequate for the vast majority of design work. Tripling the purchase tolerance insures that the adjustment has adequate range to satisfy worst-case conditions with a good margin. This shortcut sacrifices resolution because an adjustment cannot have simultaneous wide range and wide resolution. Usually, resolution is not a problem; but when increased resolution is required, it can be obtained by using a multiturn potentiometer. When this trick fails to provide adequate resolution, the designer must go back to Equations 8 and 9, solve them for the limit resistor values, and insure that the potentiometer is just large enough to yield the limits.

Drift tolerances and their elimination

The resistor and reference drift tolerance is 2%. A large portion of the resistor drift tolerance results from temperature variations caused by ambient temperature fluctuations and self-heating; thus, when the resistor current is small and the ambient temperature is controlled, smaller drift tolerances are appropriate. Use the reference specifications to calculate the reference drift tolerance for each application, and don't neglect manufacturing and end-of-life stresses. Normally, purchase tolerances can be adjusted, but drift tolerances usually limit the circuit's accuracy. The worst-case analysis equations are used to calculate the effects of the drift tolerances.

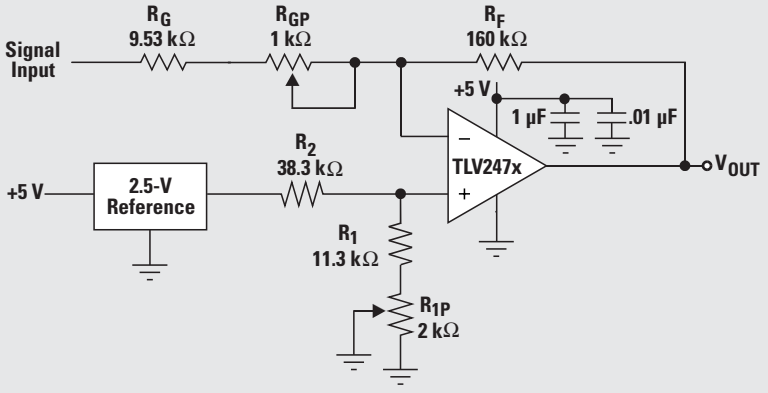
The maximum and minimum transfer functions (for D = 2%) are

$$V_{OUT(MAXD)} = -16.64\ V_{IN} + 11.34 \text{ and} \quad \textbf{(10)}$$

$$V_{OUT(MIND)} = -15.37\ V_{IN} + 9.514. \quad \textbf{(11)}$$

The transfer function varies approximately 15% because of the drift tolerances, and the best accuracy that the circuit can guarantee is 3 bits. Choosing more accurate resistors lowers the drift tolerance, and choosing resistors with a guaranteed temperature coefficient dramatically lowers the drift tolerance because all resistors must drift in the same direction. Careful evaluation of the ambient and life conditions might lower the drift tolerance, and you may choose to assume the risk that the components never drift to worst-case values. When the manufacturing volume of these circuits is large, statistics guarantee that some circuits will drift to the extreme; and it may be

Figure 2. Final circuit schematic



cost-efficient to accept those failures. Drift problems are the hardest for field people to identify and solve, so you might want to err on the cautious side.

The drift can be virtually eliminated by using CBM techniques. A DAC can be used to set the reference voltage, and a variable gain amplifier can be used as the gain stage (refer to Figure 3). The reference DAC is set to the nominal reference voltage. A known input voltage is applied, and the gain DAC increases the gain till the proper output voltage is achieved. A second known voltage is applied to the input, and the reference DAC is adjusted till the output voltage is correct. Rocking these two adjustments quickly yields better than 0.1% precision. If the measurement is taken shortly after the CBM process, it is very accurate.

Summary

Passive components have purchase and drift tolerances, and the drift tolerance may be larger than the purchase tolerance. The purchase tolerance can be adjusted at the end of the manufacturing process, but the drift tolerance can be adjusted only just prior to making a measurement. A circuit's output voltage can drift 15% if 1% resistors are used. Drift tolerances can be drastically reduced with CBM techniques.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "Op Amps for Everyone," Design Reference	. . .slod006

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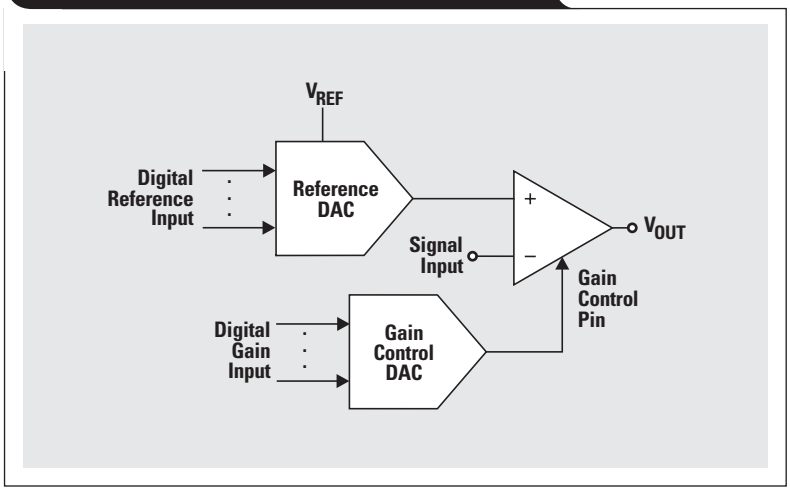
Figure 3. Block diagram of a CBM circuit



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