Skew definition and jitter analysis

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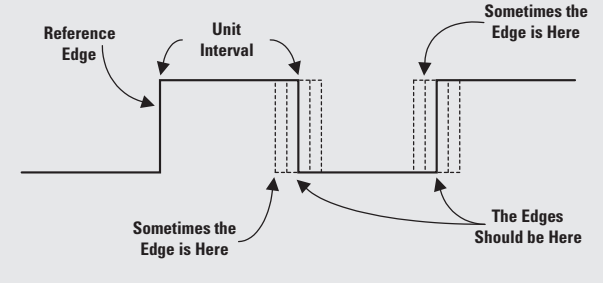
Over the past few years, jitter has become a signal property that many engineers take very seriously. Signal rise times are getting much shorter in high-speed digital systems, and slight variations in the timing of a rising or falling edge are more important with each additional Mbps. The phenomena of signal skew and data jitter in a waveform not only affect data integrity and set-up and hold times but magnify the signaling rate vs. transmission distance tradeoff, ultimately leaving a designer with a degraded system.

Although several standards clearly define various skews and jitters, no one definition can clarify the origins and contents of jitter in a measurement. JEDEC Standard 65 (EIA/JESD65) defines skew as "the magnitude of the time difference between two events that ideally would occur simultaneously" and explains jitter as the time deviation of a controlled edge from its nominal position. IEEE and the International Telecommunications Union (ITU) reinforce this time variation definition with similar discussions (see Figure 1). A more appropriate jitter definition would seem to be one for something called "jitter stew."

Jitter stew

Jitter can best be defined as the sum total of skews, reflections, pattern-dependent interference, propagation delays, and coupled noise that degrade signal quality. Jitter stew basically represents the portion of a unit interval (UI) during which a logic state should be considered indeterminate. The eye pattern is a useful tool for measuring overall signal quality. It includes all of the effects of systemic and random distortion and shows the time during which the signal may be considered valid. A typical eye pattern is illustrated in Figure 2 with the significant attributes identified.

Figure 1. Skewed edges



Several characteristics of the eye pattern indicate the quality of a signal. The height of the eye above or below the receiver threshold voltage level at the sampling instant is the noise margin of the system. Although jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal, jitter present at the receiver threshold voltage level measures the absolute jitter of the signal and is considered by some to be a more effective representation of the jitter applied to the input of a receiver. Jitter is typically given either in time as picoseconds or as a percentage of the UI. The UI or bit-length is the reciprocal value of the signaling rate; therefore, the time a logic state is valid is simply the UI minus the jitter. Percent jitter, which is the jitter time divided by the time of the UI and multiplied by 100, is more commonly used. Note how noise riding the signal levels in Figure 3 not only reduces the noise margin but

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Figure 2. Standard jitter measurement

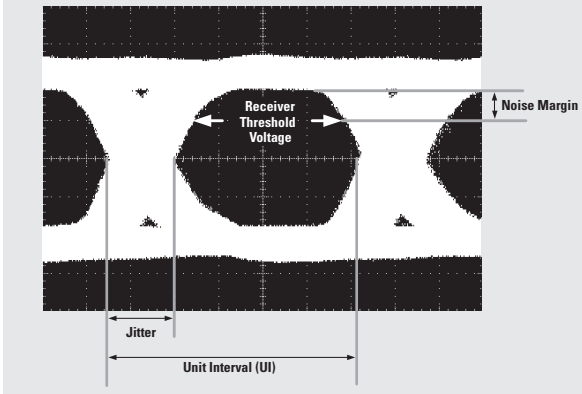
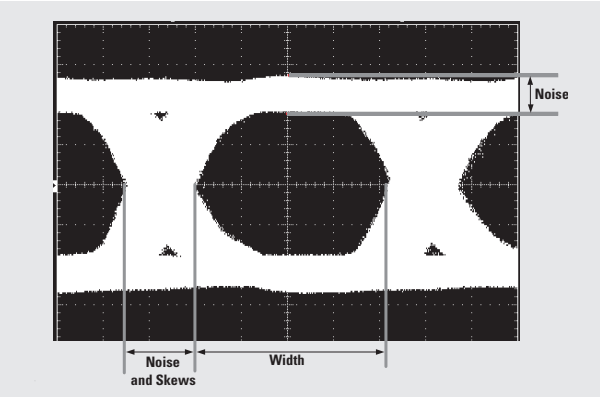


Figure 3. Noise and skews



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also becomes a primary ingredient of the jitter stew present in the eye pattern.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate reception, and lowering the height enters the input voltage threshold of a receiver.

Jitter ingredients

Noise may be coupled onto a signal from several sources and is not uniform at all frequencies. The more obvious noise sources are the components of a transmission circuit that include the signal transmitter, traces, cables, connectors, and receiver. Beyond that, there is a termination dependency, crosstalk, pattern-dependent inter-symbol interference, and V_{CC} and ground bounce.

Inter-symbol interference (ISI)

ISI is a leading cause of signal degradation. Signal attenuation and variations of signal rise and fall times combine to ultimately limit signaling rate and cable length. Figure 4 displays these effects on a signal caused just by the interplay of data patterns, rise times, and circuit impedance.

Typically referred to as pattern-dependent skew, these one-to-zero and zero-to-one voltage attenuation and propagation delays are only a few of the several jitter sources associated with a circuit component's frequency-dependent impedance. Line resistance, capacitance (mutual and ground), conductance, and inductance (series and mutual) interplay with a signal and adjacent signals at different frequencies depending on matters like slew rate, electrical environment, board layout, board composition, and connector and cable quality.

Reflections

Another of the major jitter ingredients results from signal reflections that radiate back and forth on a transmission line due to termination impedance mismatches that also exhibit frequency dependence. Even when a line is properly terminated with a value matching the characteristic impedance of the line, the "real" part of the impedance

Figure 5. Skew from unsymmetrical input-voltage levels

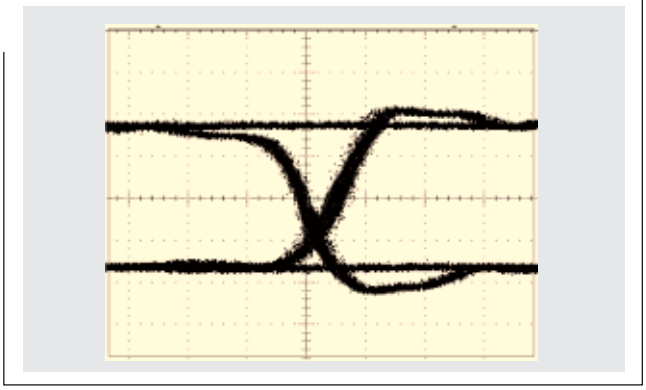
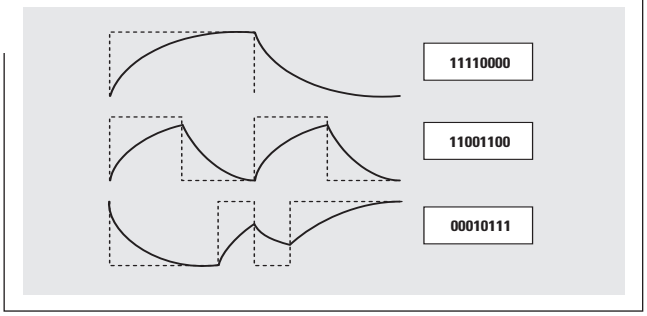


Figure 4. Pattern-dependent skew



actually changes with frequency as frequency-dependent parameters rise and fall in value.

Crosstalk

Crosstalk is jitter induced from the magnetic fields generated by nearby signals. It produces impedance changes in components, connectors, and transmission lines. If an adjacent signal is synchronous and in phase, these frequency-dependent effects may be greatly amplified. Once it is understood that the effective impedance of a circuit changes dramatically with frequency, the causes of jitter and skew are more readily understood. Aside from noise emanating from power supplies and ground, changes in circuit impedance are responsible for most of the jitter in data transmission circuits. The effective impedance of a circuit is a dynamic property not based solely on the physical properties of circuit components. Although skewed signals can result from something as simple as different transmission line lengths, many are the result of circuit component quality. For instance, adjoining signals in a multi-pair cable can arrive at the end of the cable at different times even if the lengths are equal. This time difference is defined as a cable's worst-case delay skew and is used as one of the indicators of cable quality.

Cycle-to-cycle jitter, $t_{jit(cc)}$

An extremely high skew condition occurs in any type of differential connection when the logic levels applied to a differential driver are not symmetrical about the driver's input-voltage trigger threshold—that is, an equal voltage magnitude above and below the trigger voltage. This threshold varies with frequency; therefore, a circuit designed for operation at a particular signaling rate may suffer a severe jitter increase if the signaling rate is changed.

If an input signal is biased equally above and below a driver's triggering threshold, the transition time of the signal to the trigger level is equal; therefore, the differential outputs trigger at the same time with each cycle. However, if the magnitude of the input signal is greater, either above or below the threshold, one cycle triggers earlier than the following cycle ($t_{cycle1} \neq t_{cycle2}$) and appears differentially as displayed in Figure 5. Therefore, $t_{jit(cc)} = | t_{cycle1} - t_{cycle2} |$.

Figure 6. Bank skew

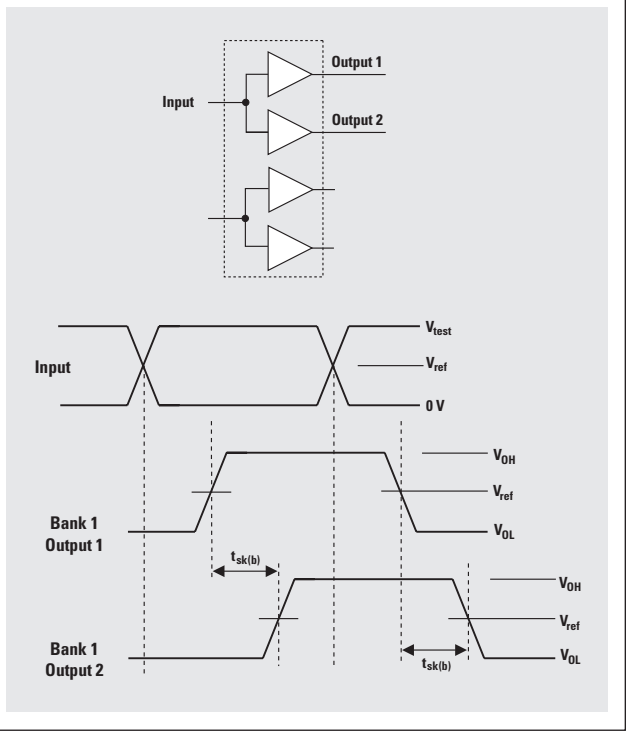
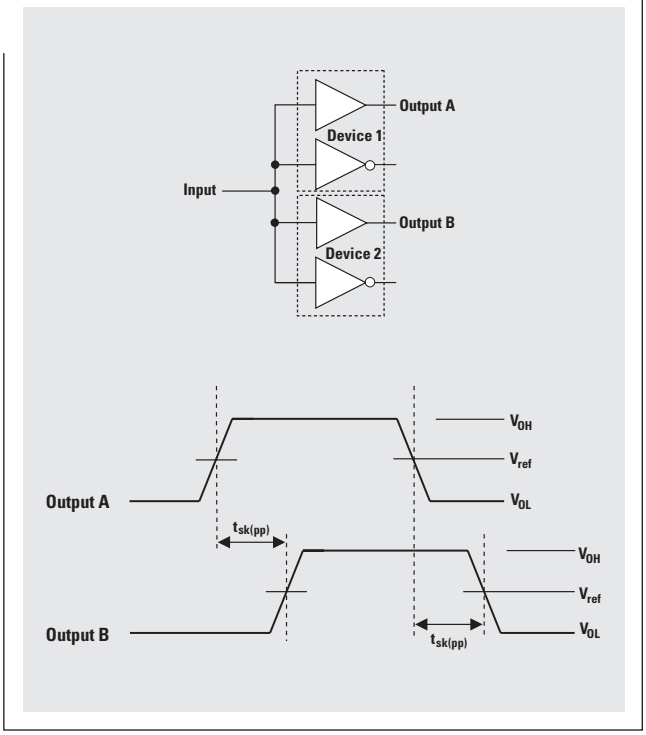


Figure 7. Part-to-part skew



Bank skew, $t_{sk(b)}$

Bank skew is the magnitude of the time difference between the outputs of a single device with a single driving input terminal.

Part-to-part skew, $t_{sk(pp)}$

Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two separate devices when both devices operate at the same temperature with the same input signals and supply voltages, and have identical packages and test circuits.

Pulse skew, $t_{sk(p)}$

Pulse skew is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

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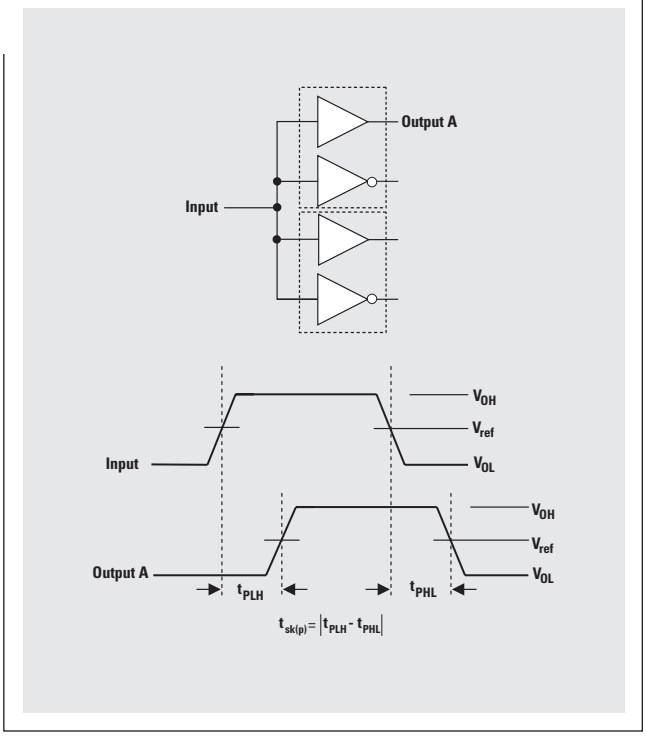
Figure 8. Pulse skew



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Output skew, $t_{sk(o)}$

Output skew is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

Jitter measurement test set-up

Figure 10 shows the circuit under consideration with the transmission line being probed at the output of both driver and receiver. First, the output of the HFS 9003 is applied directly to the input of the oscilloscope, and background noise is measured. This noise measurement, a function of the electrical environment that varies with each application, is subtracted from the overall jitter measurement. The Tektronix 784D is a digital phosphor oscilloscope (DPO), and its "infinite persistence" in DPO mode is employed for jitter measurement. Jitter is then easily measured with the cursors.

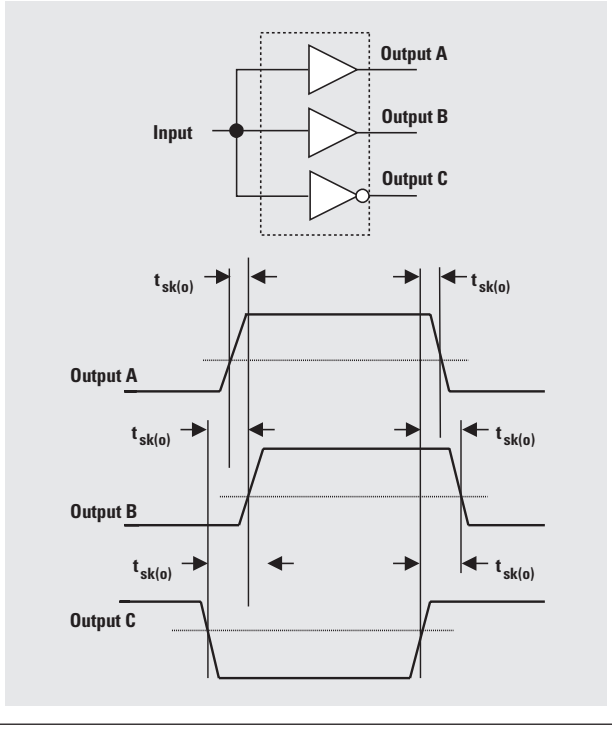
Test equipment

HP E3516A and HP 6236B DC power supplies provide the required supply voltage for the differential driver and receiver in the circuit. For the eye pattern jitter measurements, a Tektronix HFS9003 signal generator is employed as a non-return-to-zero (NRZ), pseudo-random binary sequence (PRBS) signal source for the driver and is adjusted as follows:

- Pattern: NRZ, PRBS
- Transition time: 800 ps
- Input voltage: Balance equally above and below driver threshold

At high signaling rates, the influence of equipment used to measure a signal of concern should be minimized. For differential tests, a Tektronix 784D oscilloscope and Tektronix P6247 differential probes are used. Each has a bandwidth of 1 GHz and a probe capacitance of less than 1 pF.

Figure 9. Output skew



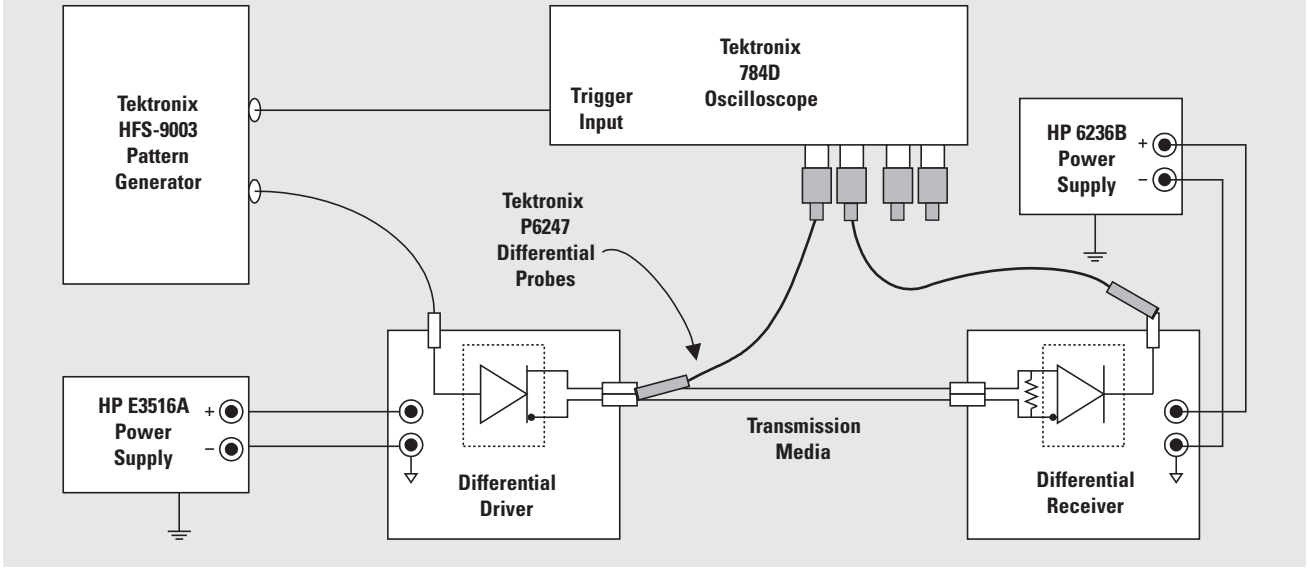
References

1. "EIA/JESD65, JEDEC Standard No. 65"
2. "IEEE Std 1596.3-1996"

Related Web site

www.ti.com/sc/docs/products/msp/intrface/index.htm

Figure 10. Jitter measurement set-up



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