LVDS receivers solve problems in non-LVDS applications

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Introduction

This article describes how some of TI's customers have solved simple problems using LVDS receivers. They're just not using them with LVDS drivers!

Problem 1: "I don't want to put 5-V PECL in my box."

This customer was designing a small 3.3-VDC battery-powered subsystem. Unfortunately, he had to receive data being sent from a 5-VDC differential PECL driver. He did not want to have 5-VDC in his subsystem and was already looking for ways to reduce the 3.3-V power consumption to extend battery life. The subsystem used a "multi-drop" configuration with 8 loads.

The solution was remarkably simple. He installed 220-ohm series resistors on the differential PECL input lines and terminated the last receiver with 110 ohms. The PECL data was being received at 50 Mbps through 2 meters of CAT5 cable.

LVDS is often thought of as a high-speed device, but this customer knew it also consumed little power. He wasn't going fast, or far, but he needed to get as much done as possible on a single battery charge. He estimates that he doubled the "on" time using LVDS receivers.

Another customer presented a similar application that he had optimized for low power at 100 Mbps. He used the LVDS32A (the operative letter here is "A"), which has an increased input common-mode voltage (V_{ICM}) range. Using this feature allows the transmission line to be terminated "line-to-line" into 100 ohms and not referenced to ground. The '32A handles the 4.4-VDC PECL V_{ICM}, making a resistor divider unnecessary.

TI built up this second circuit in the lab and examined the eye pattern. As shown in Figure 3, the circuit performs extremely well at 100 Mbps. The top trace is the LVDS input to the receiver, and the bottom trace is the receiver output signal.

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Figure 1. 5-V PECL-to-3.3-V LVDS multi-drop data transmission system

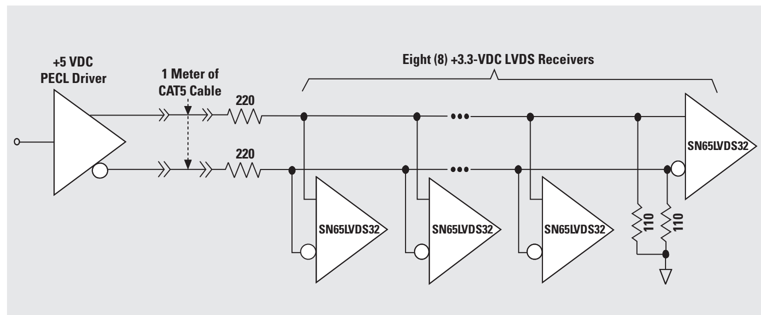


Figure 2. Optimized PECL-to-LVDS using an LVDS32A

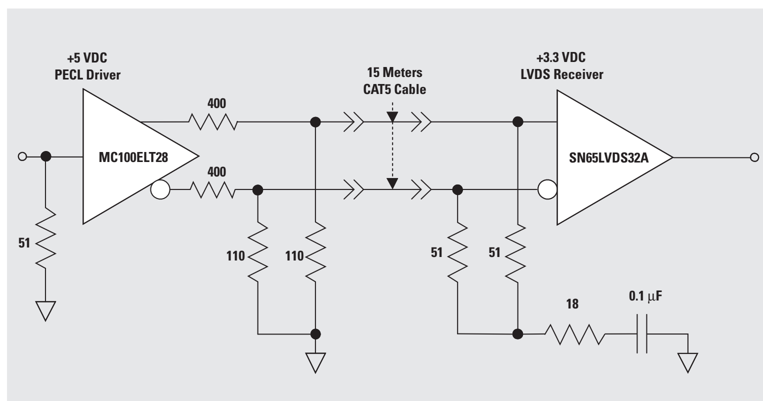
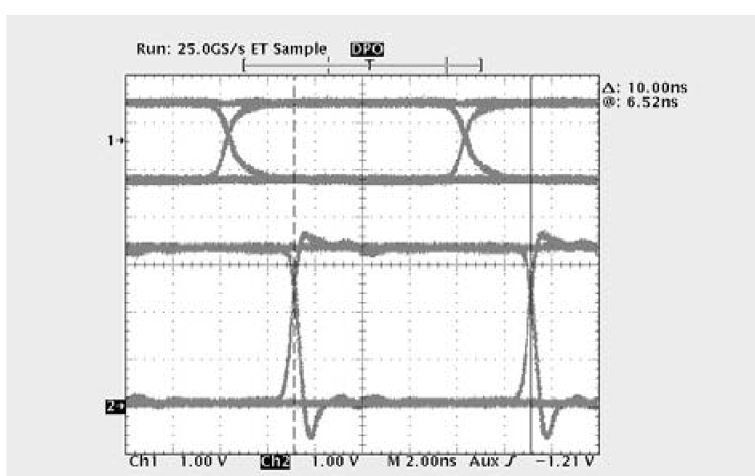


Figure 3. 5-V PECL-to-3.3-V LVDS at 100 Mbps across 15 meters of CAT5 cable



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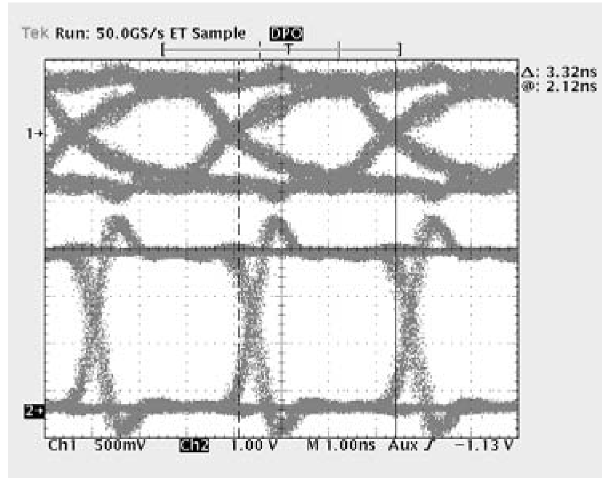
It was obvious that the signaling rate could be increased, so this was run at 200 Mbps and 300 Mbps. The waveforms at 300 Mbps are presented in Figure 4. The top trace in Figure 4 is the input signal to the LVDS receiver. The bottom trace is the output of the LVDS32A receiver. The cable effects become evident at the higher signaling rates, and the signal degrades rapidly after 330 Mbps.

LVDS is used not only for high-speed but often for low-power applications as well.

Figure 4. 5-V PECL-to-3.3-V LVDS32A at 300 Mbps across 15 meters of CAT5 cable



Problem 2: "The output from my crystal doesn't look very good!" (or "My processor board seems to work better when the clock has edges.")

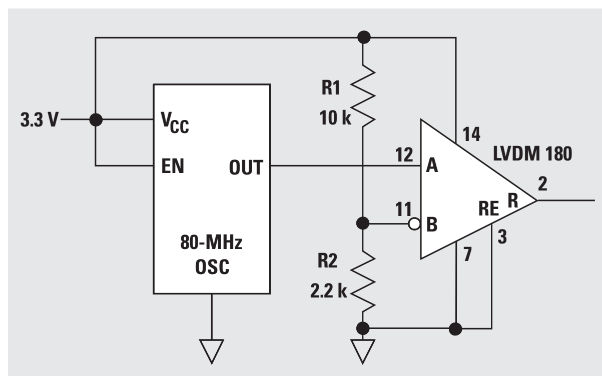
Another customer found that the output signal from his crystal oscillator needed to be "cleaned up" and distributed across a processor motherboard. His prior solutions had used a Schmitt trigger. Depending upon which oscillator he used, he sometimes used a transformer before the Schmitt trigger to boost and shift the input level to the Schmitt trigger. He had an unused receiver in a LVDM180 transceiver and now uses it to "clean up his clock," as shown in Figure 5.

This customer has several interesting LVDS applications on his processor board. This one caught the author's eye because it's so simple. The customer realized that an LVDS receiver is a very high-speed comparator, and that's exactly what he wanted. He said that this circuit gives him faster edges, uses less power, reduces his parts count, and is less expensive.

This circuit was tried in the lab with several different crystals (the author even tried it with an LC tank circuit). We found that R2 had to be replaced with a 10-kohm potentiometer because different oscillators had different output waveforms. Adjusting R2 made the duty cycle variable over a very wide range. Results obtained from a 100-MHz crystal are shown in Figure 6. The circuit was constructed with the crystal output connected to the inverting input pin on the LVDM180 (pin 11) instead of to the non-inverting input (pin 12).

If your CLK looks a little like a sine wave, give this a try. The author was impressed.

Figure 5. Using an LVDS receiver as a high-speed comparator

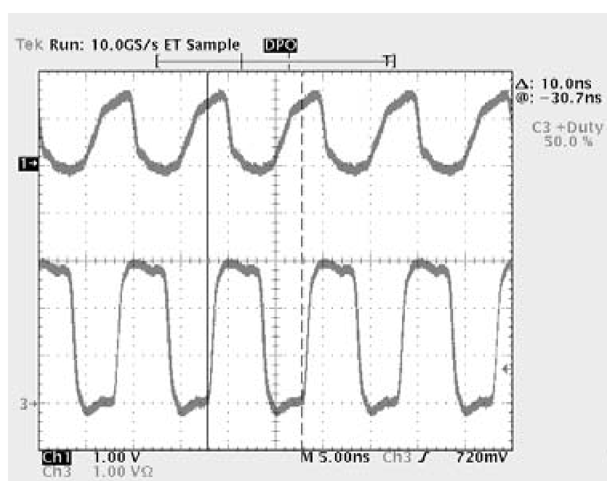


Problem 3: "Can I use LVDS to receive high-speed 5-V CMOS data?"

A customer asked if he could use LVDS to receive high-speed digital video through 10 meters of CAT5 cable. The driver was a single-ended, high-speed 5-V CMOS driver. He mentioned that the video was streaming at 300 Mbps. He did not know the specific part number of the driver, and he said he "could live with a few errors" since it was video.

One solution was to provide him with the schematic shown in Figure 7. The SN54AHC04 hex inverter was selected as the 5-V CMOS driver along with Belden's Mediatwist™ cable (because that's what was on hand). At 300 Mbps, impedances have to be matched, so the termination scheme was optimized to 100 ohms, and values were selected that would divide the input signal down to the nominal input range (V_{ICM} approximately 1.2 VDC) of the LVDS receiver. Note that this scheme creates the differential input at the receiver by bringing the driver

Figure 6. Using an LVDS receiver to improve the edges of an oscillator



ground through the cable. In the actual application, a system ground would be required between the driver supply and receiver supply to minimize any ground potential difference (V_{GPD}) between driver and receiver.

The waveforms shown in Figure 8 verify that the customer could use an LVDS receiver to receive his video data. The top waveform is the digital video signal at the input pin of the LVDS32. The bottom waveform is the output signal from the receiver.

The customer said he "could live with a few errors," so a bit-error-rate (BER) test was performed to see how fast this circuit would go before serious errors occurred. . The test set pattern generator in the BER tester can output only a maximum V_{IH} of 2.0 VDC, which would cause errors if the AHC04 V_{CC} remained at 5.0 V. Fortunately, the AHC04 inverter operates with V_{CC} = 2.5 V to 5 V, so V_{CC} was adjusted to 3.3 VDC, and the BER test was run with V_{IH} = 2.0 VDC and V_{IL} = 1.2 VDC. The test started at 400 Mbps, and the BER was recorded. The signaling rate was decreased in 10-Mbps steps, and the test was repeated. This process was continued until no errors were received at 340 Mbps. The BER results are shown in Figure 9.

The test continued to run, but at 350 Mbps the error rate was 10^{-13}, which equates to 1 bit error in every 10 trillion bits. This would be great since "it's just video." Also, the test time increases as the errors decrease. For example, at 300 Mbps it takes 9.25 hours to transmit 10 trillion (10^{13}) bits, so testing for error rates of 10^{-15} or 10^{-16} takes days to complete. But it's better now than it was—before LVDS, these BER tests were run at 50 Mbps and would take 23 days!

Conclusion

This article has demonstrated that an LVDS driver does not always have to be connected to an LVDS receiver. The latter works quite well with other types of drivers, as these customers have demonstrated.

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Figure 7. 5-V high-speed CMOS-to-LVDS receiver

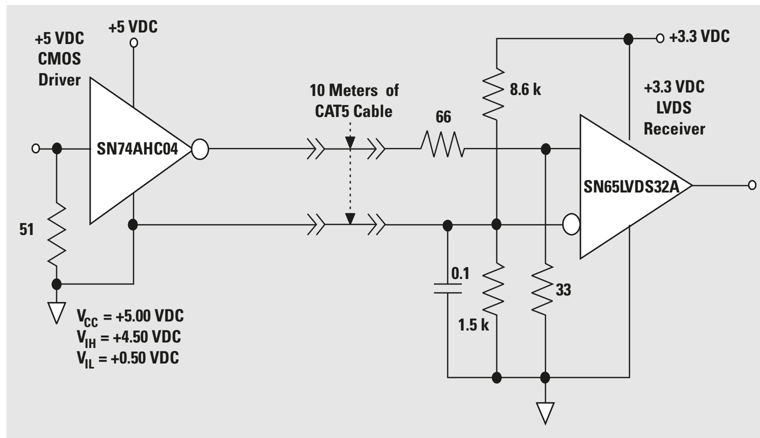


Figure 8. Single-ended 5-V CMOS driver into an LVDS receiver through 10 meters of CAT5 cable at 300 Mbps

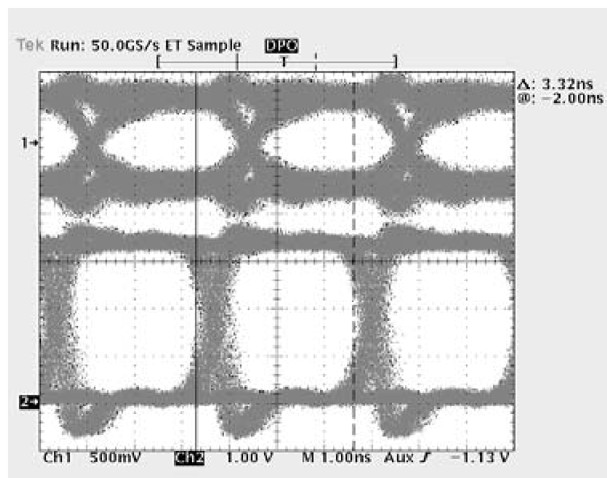
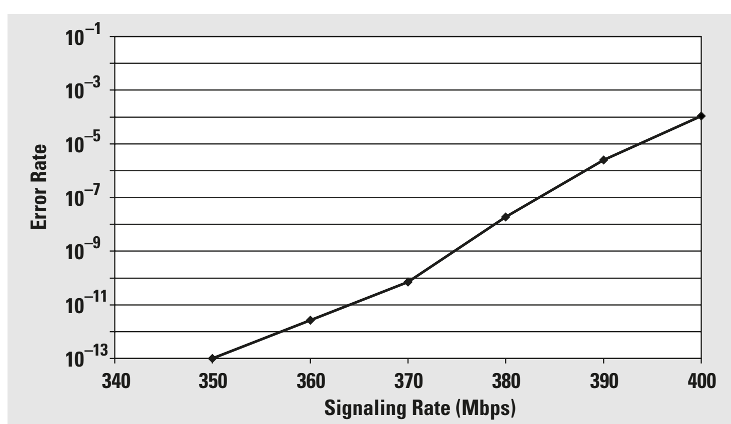


Figure 9. Bit error rate vs. signaling rate



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