Understanding the stable range of equivalent series resistance of an LDO regulator

By Bang S. Lee
Application Specialist, Power Management

This application note explores the stable range of equivalent series resistance (ESR) values for LDO regulators. An ac model of an LDO regulator is presented to discuss the LDO frequency response. Both stable and unstable ESR ranges are examined.

An ac model of an LDO regulator

Figure 1 shows the essential elements of a PMOS LDO regulator. The LDO regulator can be partitioned into four separate and distinct functional blocks—the pass element, the reference, the sampling resistor, and the error amplifier. The error amplifier is modeled by a transconductor (g_a) with a load comprised of capacitor C_{par} and resistor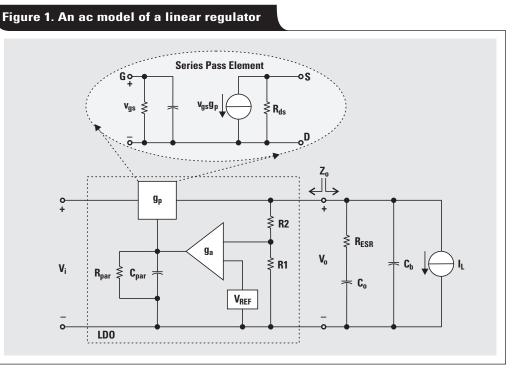 R_{par}. The parasitic parameters (C_{par}, R_{par}) represent both the output impedance of the error amplifier and the input impedance of the series pass element. The series pass element (PMOS transistor) is modeled by a small signal model with transconductance g_p. An output capacitor C_o with an equivalent series resistor (R_{ESR}) and a bypass capacitor C_b are added.

From Figure 1, the output impedance is given by

$$Z_o = R_{12p} \left\| \left(R_{ESR} + \frac{1}{SC_o} \right) \right\| \frac{1}{SC_b} \tag{1}$$

$$= \frac{R_{12p}(1 + SR_{ESR}C_o)}{S^2 R_{12p}R_{ESR}C_o C_b + S[(R_{12p} + R_{ESR})C_o + R_{12p}C_b] + 1},$$

where $R_{12p} = R_{ds} \| (R1 + R2) \approx R_{ds}$. $\qquad$ **(2)**

Typically, the output capacitor value C_o is considerably larger than the bypass capacitor C_b. Thus, the output

Figure 1. An ac model of a linear regulator

impedance Z_o approximates to

$$Z_o \approx \frac{R_{ds}(1 + SR_{ESR}C_o)}{[1 + S(R_{ds} + R_{ESR})C_o] \times [1 + S(R_{ds} \| R_{ESR})C_b]}. \tag{3}$$

From Equation 3, a part of the overall open-loop transfer function for the regulator is obtained, and the zero and poles can be found. The first pole is

$$P_o; \quad S(R_{ds} + R_{ESR})C_o = -1 \tag{4}$$

$$\therefore f_{po} = \frac{-1}{2\pi(R_{ds} + R_{ESR})C_o} \approx \frac{-1}{2\pi R_{ds}C_o} \ (\because R_{ds} \gg R_{ESR}). \tag{5}$$

The second pole is obtained from Equation 3 again:

$$P_b; \quad S(R_{ds} \| R_{ESR})C_b = -1 \tag{6}$$

$$\therefore f_{pb} = \frac{-1}{2\pi(R_{ds} \| R_{ESR})C_b} \approx \frac{-1}{2\pi R_{ESR}C_b}. \tag{7}$$

The zero is

$$Z_{ESR}; \quad SR_{ESR}C_o = -1 \tag{8}$$

$$\therefore f_{Z(ESR)} = \frac{-1}{2\pi R_{ESR}C_o}. \tag{9}$$

In addition, another pole exists from the input impedance of the pass element (i.e., the output impedance of the amplifier, R_{par}, C_{par}). The approximated poles and the zero of the LDO regulator are then given by
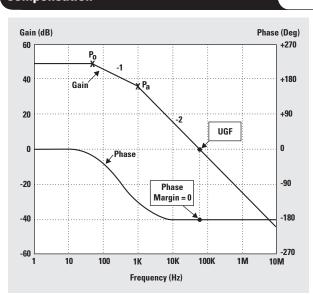
$$P_o \approx \frac{1}{2\pi R_{ds}C_o} \approx \frac{I_L}{2\pi V_A C_o}, \tag{10}$$

$$P_b \approx \frac{1}{2\pi R_{ESR}C_b}, \tag{11}$$

$$P_a \approx \frac{1}{2\pi R_{par}C_{par}}, \text{ and} \tag{12}$$

$$Z_{ESR} \approx \frac{1}{2\pi R_{ESR}C_o}, \tag{13}$$

where $R_{ds} \approx V_A/I_L$, $V_A = 1/\lambda$ for MOS device, and λ is the channel-length modulation parameter. Pole P_a is the only one introduced at the input of the pass device, not at the output of the device. Based upon the derived poles and zero, the typical frequency response of the LDO regulator is obtained and is shown in Figure 2. Pole P_o depends on the load current. When load current is low, a pole response occurs at relatively low frequencies, thereby degrading phase margin. Worst-case of stability arises at the extreme values of the ESR and at low load currents.
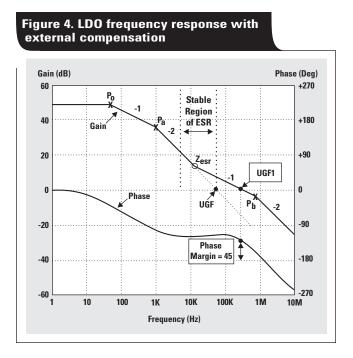
Figure 2. Typical frequency response of the LDO voltage regulator

Range of stable ESR

An LDO regulator would require an output capacitor with an output equivalent series resistor (ESR) to stabilize the control loop. As shown in Figure 3, an LDO has two poles that cause instability if it is not compensated. It is obvious that the linear regulator is unstable because the phase shift at unity gain frequency (UGF) is –180° (i.e., phase margin = 0°) due to the effects of two poles (P_o, P_a) at low

Figure 3. LDO frequency response without compensation

Figure 4. LDO frequency response with external compensation

Continued from previous page

frequencies. To make the regulator stable, a zero must be added, which will cancel out the phase effect of one of two poles.
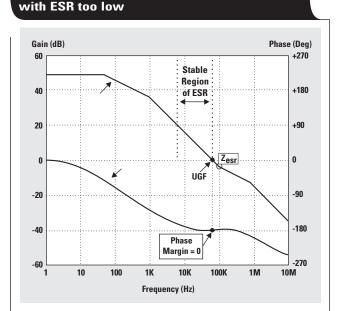
The ESR of an output capacitor or a compensated series resistor (CSR) is used for the zero. Figure 4 shows how the ESR (or CSR) zero stabilizes the control loop. The zero produced by the ESR locates before UGF so that the phase margin at UGF_1 will be higher than 0°. Thus, the linear regulator becomes stable. The phase margin of the control loop at UGF always should be more than 0° for the system stability.

The ESR value should be maintained in the range that determines the loop stability. In most cases, LDO regulators have the minimum/maximum ESR values. Figures 5 and 6 show that the loop responses are unstable even though a zero is added. From Equations 11 and 13, the zero Z_{esr} and the pole P_b are determined by the ESR. When the ESR changes, Z_{esr} and P_b are shifted upward/downward and the loop stability is affected.

Figure 5 illustrates the unstable frequency response of LDO when the ESR is too high, and Figure 6 illustrates the LDO frequency response when the ESR is too low. For both cases, the phase margin at UGF is less than or equal to 0°, resulting in system instability. Figures 5 and 6 show the stable range of Z_{esr}.
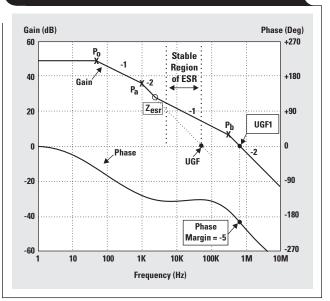
Since ESR can cause instability, LDO manufacturers typically provide a graph showing the stable range of ESR values. Figure 7 shows a typical range of ESR values with respect to the output currents (TI TPS76933, 3.3-V LDO regulator). This curve is called the "Tunnel of Death." The curve shows that ESR must be between 0.1 Ω and 8 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the ESR requirements.

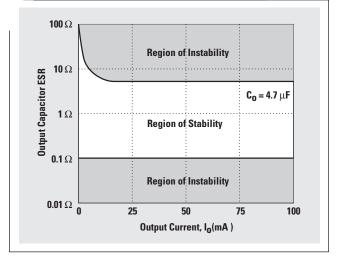**Figure 5. Unstable frequency response of LDO with ESR too high**

References

1. Thomas Kugelstadt, "Fundamental Theory of PMOS Low-Dropout Linear Regulators," Application Report, Texas Instruments Inc., literature number SLVA068.

2. Bang S. Lee, "Technical Review of Low Dropout Voltage Regulator Operation and Performance," Application Report, Texas Instruments Inc., literature number SLVA072.

3. Abraham I. Pressman, *Switching and Linear Power Supply, Power Converter Design* (Rochelle Park, NJ: Hayden Book Company, Inc., 1977).

4. Gabriel Alfonso Rincon-Mora, "Current Efficient, Low Voltage, Low Drop-Out Regulators," PhD Thesis, Georgia Institute of Technology, November 1996.

Figure 6. Unstable frequency response of LDO with ESR too low

Figure 7. Range of stable ESR values

Products

Amplifiers	**amplifier.ti.com**
Data Converters	**dataconverter.ti.com**
DSP	**dsp.ti.com**
Interface	**interface.ti.com**
Logic	**logic.ti.com**
Power Mgmt	**power.ti.com**
Microcontrollers	**microcontroller.ti.com**

Applications

Audio	**www.ti.com/audio**
Automotive	**www.ti.com/automotive**
Broadband	**www.ti.com/broadband**
Digital control	**www.ti.com/digitalcontrol**
Military	**www.ti.com/military**
Optical Networking	**www.ti.com/opticalnetwork**
Security	**www.ti.com/security**
Telephony	**www.ti.com/telephony**
Video & Imaging	**www.ti.com/video**
Wireless	**www.ti.com/wireless**

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI Semiconductor KnowledgeBase Home Page
support.ti.com/sc/knowledgebase

Product Information Centers

Americas

Phone	+1(972) 644-5580	Fax	+1(972) 927-6377
Internet/Email	support.ti.com/sc/pic/americas.htm		

Europe, Middle East, and Africa

Phone

Belgium (English)	+32 (0) 27 45 54 32	Netherlands (English)	+31 (0) 546 87 95 45
Finland (English)	+358 (0) 9 25173948	Russia	+7 (0) 95 7850415
France	+33 (0) 1 30 70 11 64	Spain	+34 902 35 40 28
Germany	+49 (0) 8161 80 33 11	Sweden (English)	+46 (0) 8587 555 22
Israel (English)	1800 949 0107	United Kingdom	+44 (0) 1604 66 33 99
Italy	800 79 11 37		
Fax	+(49) (0) 8161 80 2045		
Internet	support.ti.com/sc/pic/euro.htm		

Japan

Fax			
International	+81-3-3344-5317	Domestic	0120-81-0036
Internet/Email			
International	support.ti.com/sc/pic/japan.htm		
Domestic	www.tij.co.jp/pic		

Asia

Phone

International	+886-2-23786800		
Domestic	Toll-Free Number		Toll-Free Number
Australia	1-800-999-084	New Zealand	0800-446-934
China	800-820-8682	Philippines	1-800-765-7404
Hong Kong	800-96-5941	Singapore	800-886-1028
Indonesia	001-803-8861-1006	Taiwan	0800-006800
Korea	080-551-2804	Thailand	001-800-886-0010
Malaysia	1-800-80-3973		
Fax	886-2-2378-6808	Email	tiasia@ti.com
Internet	support.ti.com/sc/pic/asia.htm		ti-china@ti.com

C011905

SLYT187