TPS79918 RF LDO supports migration to StrataFlash® Embedded Memory (P30)

By Michael Day (Email: m-day@ti.com)
Power Management Products/Portable Power dc/dc Applications

Introduction

The Texas Instruments (TI) TPS79918 low dropout (LDO) linear regulator provides the performance required to power the new Intel® StrataFlash® Embedded Memory (P30). Intel is migrating from its third-generation 180-nm StrataFlash Embedded Memory (J3) to its fourth-generation 130-nm StrataFlash Embedded Memory (P30). This migration from J3 to P30 memory allows systems to operate at a lower overall current consumption because the P30 V_{CC} voltage requirement has dropped to 1.8 V. Intel Application Note 812[1] recommends using an LDO linear regulator to provide the new 1.8-V voltage rail.

TPS79918 features

The TPS79918 LDO offers exceptional electrical performance in a small package. It provides a high (greater than 66-dB) power supply rejection ratio (PSRR), low noise, fast startup, and excellent line and load transient response. It consumes only 40 µA of ground current at full load. No input capacitor is required for operation. The TPS79918 is stable with a small ceramic output capacitor and uses an advanced BiCMOS fabrication process to yield a 110-mV dropout voltage at the full 200-mA output load. Its precision voltage reference and feedback loop achieve a 2% overall accuracy over all load, line, process, and temperature variations. The addition of an optional noise-reduction capacitor provides an extremely low-noise output voltage. It is fully specified from T_J = –40°C to +125°C and is offered in three packages: ThinSOT-23, wafer chip-scale (WCSP), and 2 × 2 SON-6. The difference between the three packages is size and power dissipation. If we assume a 60°C ambient temperature, the power dissipation for the three packages is 142 mW, 156 mW, and 526 mW, respectively. That corresponds to a maximum continuous load current of 119 mA, 130 mA, and 438 mA, respectively.

Figure 1 shows the TPS79918 internal block diagram. The active-high enable signal turns the device on after the input voltage goes above the undervoltage lockout (UVLO) level. UVLO ensures that the input voltage is available, which provides a clean start-up waveform. The IC features current-limit and thermal-shutdown protection in case of a system failure. The internal 500-kΩ resistor, along with an external noise-reduction capacitor on the NR pin, provides an RC filter to reduce the bandgap noise, resulting in a low-noise output voltage. The quickstart switch initially shorts out this resistor to provide a fast 40-µs start-up time. This IC has excellent transient response enhanced by the Overshoot Detect circuit that during a heavy load actively pulls the output voltage down to a light-load transient.

Figure 1. TPS79918 internal block diagram

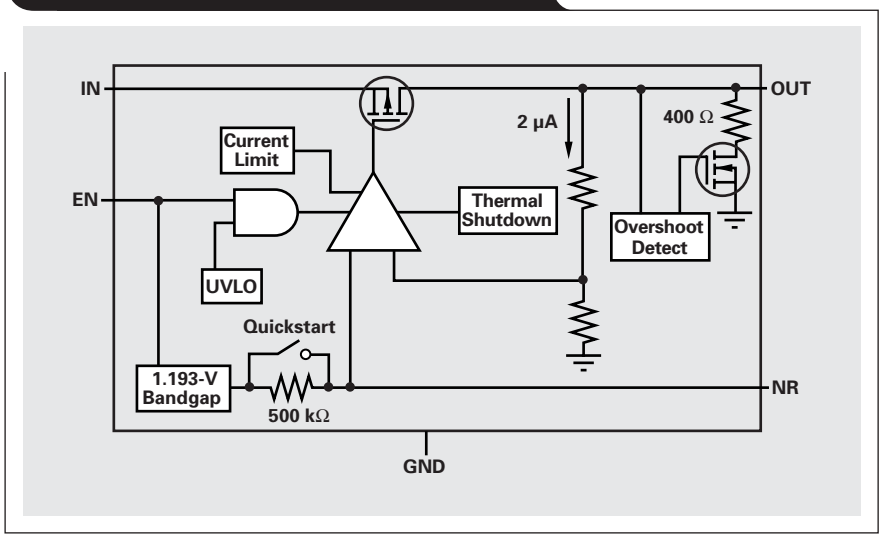
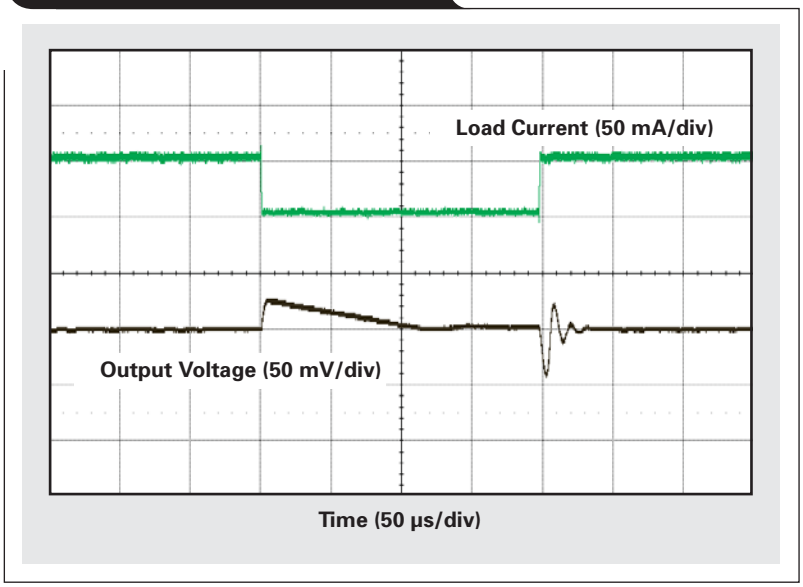


Figure 2. TPS79918 load transient



Intel StrataFlash Embedded Memory (P30) requirements

Migrating existing J3 memory systems to the new P30 memory requires regulating the existing 3.0-V core voltage down to 1.8 V. The 1.8-V core voltage requires regulation within ±0.1 V, which is met by the TPS79918's tight 2% voltage tolerance. The LDO performs well with the load transients caused by rising and falling edges of CE# and OE#. Figure 2 shows that even with a 1- to 50-mA load transient, the output voltage drops only 40 mV. This performance meets the P30 memory input voltage requirement. Taking system-level requirements into consideration, Intel's application note cautions the designer to consider both standby current and active current. Figure 3 shows that, unlike some LDOs, the TPS79918's low quiescent current is constant over changes in input voltage and load current. The low quiescent current extends battery life in portable applications.

Figure 3. TPS79918 quiescent current vs. line and load

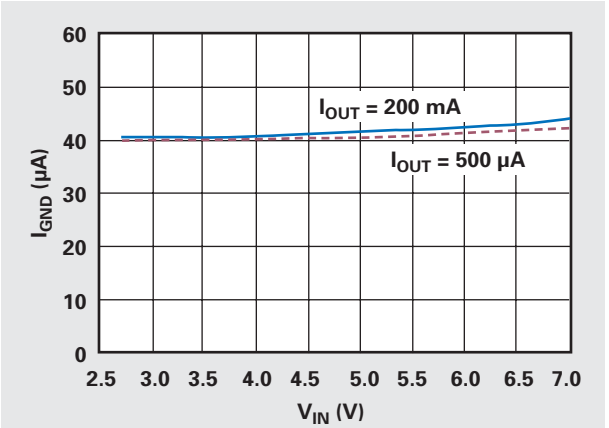


Figure 4 shows the simplicity of a TPS79918 powering a P30 memory module. The only required components are the LDO itself and its output capacitor. The input capacitor is required only if the 3.0-V output capacitor is not physically located near the LDO. The noise-reduction capacitor is needed only to power noise-sensitive applications, so it is not required in this application.

Intel specifically recommends the TI LDOs in Table 1 for its StrataFlash Embedded Memory (P30). These LDOs meet the electrical and temperature requirements for the new P30 memory.

Table 1. Recommended TI LDOs for Intel StrataFlash Embedded Memory (P30)

DEVICE	V_O (V)	I_O (mA)	I_Q (µA)	PSRR (dB)	PACKAGE	DIMENSIONS (mm)
TPS79918DDC	1.8	200	40	70	TSOT-23	2.9 x 2.8 x 1.0
TPS79918DRV	1.8	200	40	70	2 x 2 SON-6	2.0 x 2.0 x 0.75
TPS79918YZU	1.8	200	40	70	WCSP	1.36 x 1.00 x 0.62

Conclusion

The TI TPS79918 LDO is ideally suited to power Intel's next-generation StrataFlash Embedded Memory (P30). The three packaging options allow the designer to optimize the solution size while the LDO's electrical performance meets the system-level requirements for low standby current, transient response, and peak current.

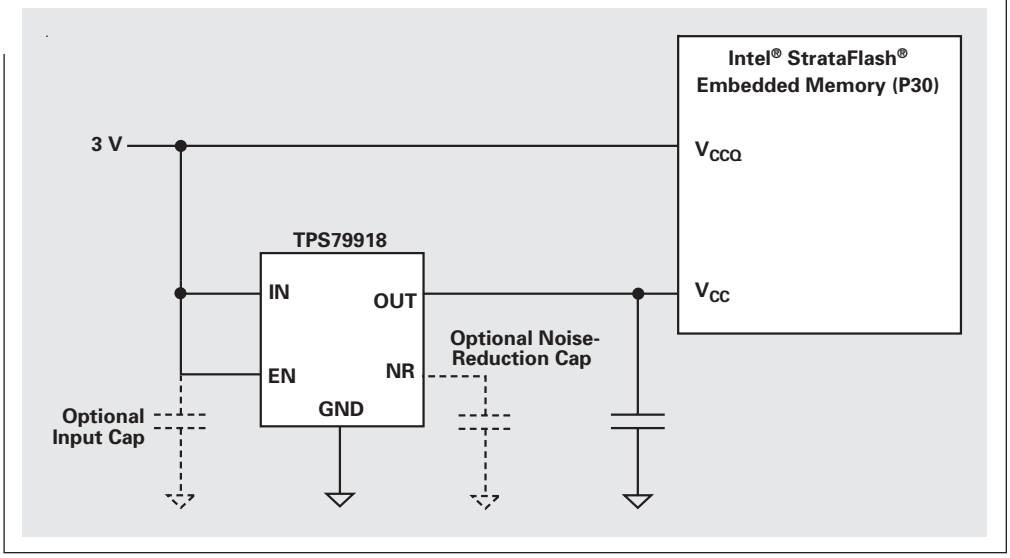
Reference

1. "Migration Guide for Intel StrataFlash® Memory (J3) to Intel StrataFlash® Embedded Memory (P30)," Intel Application Note 812, June 3, 2005, www.intel.com/design/flcomp/applnots/306667.htm

Related Web sites

power.ti.com
www.intel.com

Figure 4. Typical StrataFlash configuration with LDO



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