

Using the ADS8361 with the MSP430 USI port

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Introduction

The ADS8361 is a dual, 16-bit, 500-kSPS, analog-to-digital converter (ADC) with four fully differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differentially to the input of the ADC. This provides excellent common-mode rejection of 80 dB at 50 kHz, which is important in high-noise environments.

MSP430 devices such as the new MSP430F2013, which contain a universal serial interface (USI), can be used in a very simple and straightforward interface that requires no “glue logic” and very little software overhead. Applications that require precise timing of simultaneous data acquisition channels can use this interface to achieve desired system results.

Hardware

The hardware used to produce the timing diagrams in Figures 2 and 3 includes the eZ430-F2013 Development Tool and the ADS8361EVM.

ADS8361EVM

The ADS8361 is a member of the motor control products family of serial ADCs available from Texas Instruments (TI). The EVM provides a platform to demonstrate the functionality of the ADS8361 ADC with various TI DSPs and microcontrollers while allowing easy access to all analog and digital signals for customized end-user applications. For more information on the EVM, see Reference 1.

eZ430-F2013 Development Tool

The eZ430-F2013 is a complete MSP430 development tool including all the hardware and software necessary to evaluate the MSP430F2013. The hardware is provided in a convenient USB stick form factor. The eZ430-F2013 uses the IAR Embedded Workbench integrated development environment (IDE) to provide full emulation with the option of designing a stand-alone system or detaching the removable target board to integrate into an existing design. For more information, visit www.ti.com/ez430

Hardware interface

A simple three-wire interface is the minimum requirement to connect the eZ430-F2013 and the ADS8361EVM (see Table 1). The hardware connections are shown in Figure 1. The CLOCK, (RD + CONVST), and Serial Data A pins from the ADS8361 are connected respectively to the SCLK, MOSI, and MISO pins of the USI port. The chip select (\overline{CS}) pin is grounded because only one ADC is

Figure 1. Hardware interface block diagram

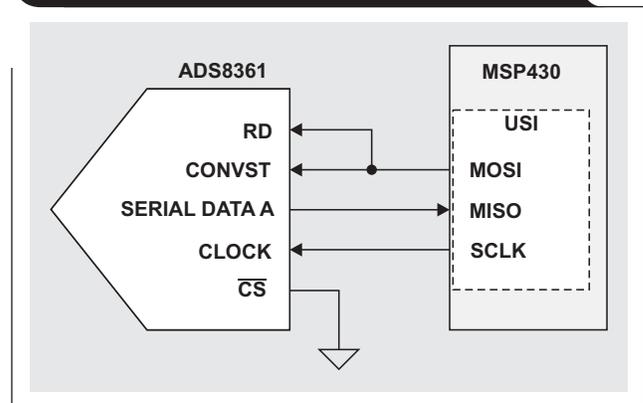


Table 1. Cable requirements

ADS8361EVM	eZ430-F2013
J2.1 — \overline{CS} *	Optional GPIO
J2.3 — CLOCK	P1.5
J2.13 — Serial Data A	P1.7
J2.7 — (RD + CONVST)**	P1.6

* \overline{CS} can be held to ground by placing a shunt jumper from J2.1 to J2.2.

** (RD + CONVST) is created by placing the shunt jumper in location W2 on pins 1 and 2.

placed on the port. If more than one device is on the bus, then chip select should be controlled by any available GPIO on the MSP430 device.

Software interface

All of the software was written and compiled using the Kickstart version of IAR Embedded Workbench for the MSP430. This software is the free version of the IDE and is available for download at www.ti.com/ez430 under “TOOL SUPPORT.” The code used in these examples is available upon request.

USI settings

The USI module provides the basic functionality to support synchronous serial communication schemes. The USI includes built-in hardware functionality to ease the implementation of SPI communication. The USI module also includes interrupts to further reduce the software overhead.

USI control registers 0 and 1 (USICTL0 and USICTL1) set up the basic operation of the serial interface. The port is configured in SPI master mode by setting bits 3, 5, 6, and 7 in USICTL0. The USI counter interrupt is set in

USICTL1 to provide an efficient means of SPI communication with minimal software overhead.

The serial clock polarity, source, and speed are controlled by settings in the USI clock control register (USICKCTL). For the purposes of this article, the polarity of the clock is set to zero (dwells low), and the clock source is the SMCLK with a division factor of one.

Bit clocking and shift register configuration are controlled in the USI port by the bit settings in the USI bit count register (USICNT). The USICNT register has 5 bits that provide up to 32 SCLK cycles per transfer. Setting the USICNT to 0×13 transmits 19 serial clocks from the MSP430 to the ADS8361 on each conversion cycle. Setting the USI16B bit in the USICNT register causes the shift register to act as a 16-bit transmit/receive buffer. Transmitted data is MSB-aligned and commences with the first SCLK cycle.

Starting a conversion

Connecting the MOSI output of the USI port to both the RD and the CONVST inputs on the ADS8361 starts a conversion cycle, and the conversion results are presented on the serial data output pins of the device.

The ADS8361 will begin to output the conversion results (MSB first) on the fourth SCLK cycle. Since the shift register holds the last 16 bits of received data, the entire 16-bit conversion result is captured for further processing. The timing diagram in Figure 2 shows the entire process.

ADS8361 operating modes

The ADS8361 has four operational modes controlled by the M0 and M1 pins. The ADS8361EVM provides jumpers to statically set the operating mode. Using GPIO output on the MSP430 permits the operating mode to be controlled by the microprocessor as well.

For two-channel operation, the EVM should be configured in Mode I or II. Depending on the MSP430 being used, the user has several options on how to receive conversion results. Devices with multiple serial ports can receive data from both the Serial Data A and Serial Data B outputs of the ADS8361. This method involves setting up one port as an SPI master and the other as an SPI slave. The master SPI port would share SCLK with the slave port, and the two serial output pins would be routed to MISO and MOSI.

Two-channel simultaneous sampling

In the case of the eZ430-F2013, there is only a single serial port, which means the ADS8361 must be set in Mode II to receive conversion results from the two simultaneously sampled input channels. This mode presents both conversion results at the Serial Data A output pin (see Figure 3).

Figure 2. Complete single-channel conversion cycle

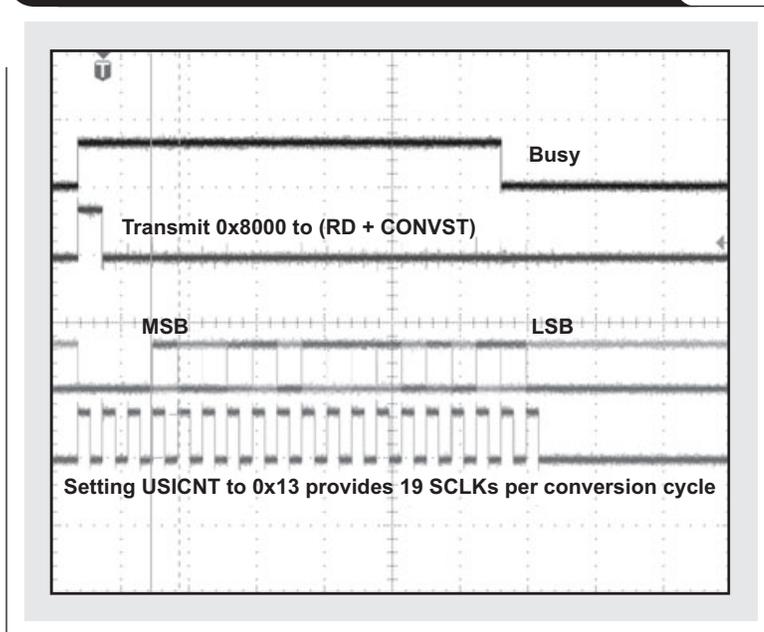
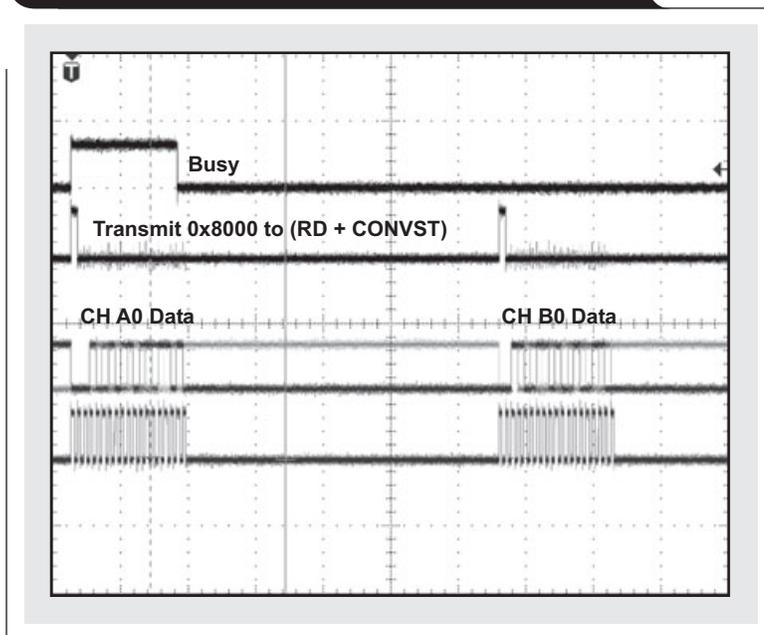


Figure 3. Complete two-channel conversion cycle



ADS8361 channel ID bits

The serial output stream of the ADS8361 also incorporates two channel ID bits so the controller can use software methods to decipher the received channel information. The first ID bit determines the channel pair, A or B. The second ID bit determines the sampled channel, 0 or 1. In Mode II operation, two of the input channels are converted and a single ID bit is included in the output data stream.

The A/B-channel ID bit is not used in this mode because the pair of inputs sampled depends on the A0 input control pin of the ADS8361. When A0 is low, the channel A0/B0 input pairs are sampled. When A0 is high, the channel A1/B1 input pairs are sampled.

The ADS8361EVM provides a jumper to statically set the input pair via the A0 pin. This too can be controlled if desired with a GPIO on the MSP430, letting the user realize up to four-channel operation—two pairs of simultaneously sampled inputs.

Four-channel sampling

Modes III and IV allow the user to realize four-channel operation of the ADS8361. Mode III provides data from the Serial Data A and B outputs. Receiving data from all four conversions in this mode would require two serial ports configured in a master/slave relationship as described previously.

Mode IV allows a single serial port to receive all four conversion results via the Serial Data A output. In this mode, both the A/B- and 0/1-channel ID bits are passed through to the conversion results. What becomes problematic in this mode when used with the eZ430-F2013 is that the ID bits are essentially lost in the shift register. It is possible to recover these bits via software, but this increases software overhead and adds unnecessary complexity.

When operating in four-channel sequential mode, the ADS8361 can be initialized in such a way that channel integrity can be maintained without the need to decipher the ID bits at all. Using available GPIO, this can be done with a simple software loop at the start of the program that actively manipulates the state of the A0, M0, and M1 inputs. An alternative is to simply ignore the first set of conversion results. The ADS8361 powers up in Mode I by default; if M0 and M1 are fixed to V_{CC} at power up, the

device will enter Mode IV operation with the second conversion cycle. This action presents channel A0 data with the third SPI transfer, followed sequentially by channels B0, A1, and B1.

Conclusion

Using the high-performance ADS8361 with the USI port of MSP430 processors is a relatively simple and straightforward task. Very little software overhead is involved; there is no need to shift or concatenate conversion results as was the case in the simple 8-bit SPI interface of the older UART port found in previous generations of the MSP430. The interface method described in this article brings a new level of flexibility to MSP430 applications that require multichannel, simultaneous data acquisition.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace “litnumber” with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. “ADS7861/8361 EVM User’s Guide”	slau094
2. “Dual, 500kSPS, 16-Bit, 2 + 2 Channel, Simultaneous Sampling Analog-to-Digital Converter,” ADS8361 Datasheet	sbas230
3. “MSP430x2xx Family User’s Guide”	slau144

Related Web sites

dataconverter.ti.com
www.ti.com/ez430
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www.ti.com/sc/device/ADS8361
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