High-Performance Analog Products

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps
- General Interest

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Conversion latency in delta-sigma converters

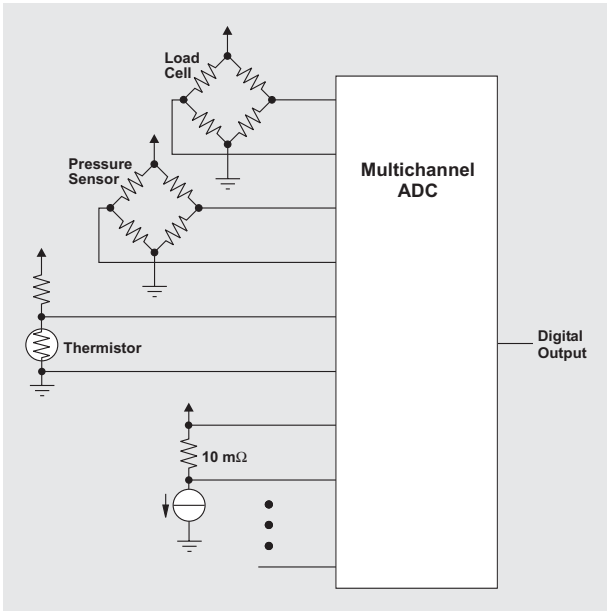
By Bonnie C. Baker (Email: bonnie@ti.com)
Senior Applications Engineer

Small-signal sensors often generate slow-moving dc signals. For these types of sensors, the delta-sigma (ΔΣ) analog-to-digital converter (ADC) eliminates most of the analog input circuitry by providing a complete high-resolution, low-noise solution. Some systems have multiple sensors generating low-frequency signals. This situation may require a high-resolution, low-noise ADC with a multiplexer at its input. An example of a multiplexed sensor system is an automotive diagnostic application where numerous small-signal sensors monitor temperature, tire pressure, air-bag readiness, etc. (see Figure 1). Examples of other sensor-input multiplexed systems are found in industrial-control, medical, avionics, and process-control applications. Even though the sensors at the input of the multiplexer in these systems present low-frequency (nearly dc) signals, switching from channel to channel creates the need for an ADC that is capable of a high-speed response.

There are two common units of measure that describe the latency of an ADC: cycles and seconds. Cycle latency is the number of complete data cycles between the conversion initiation and the availability of the corresponding output data. Latency time, measured in seconds, tells the user how fast fully settled conversions can be performed.

In the system in Figure 1, the multiple-channel ADC must have high resolution, low noise, zero-cycle latency, and low latency time. (Zero latency or 0-cycle latency is sometimes called no latency.)

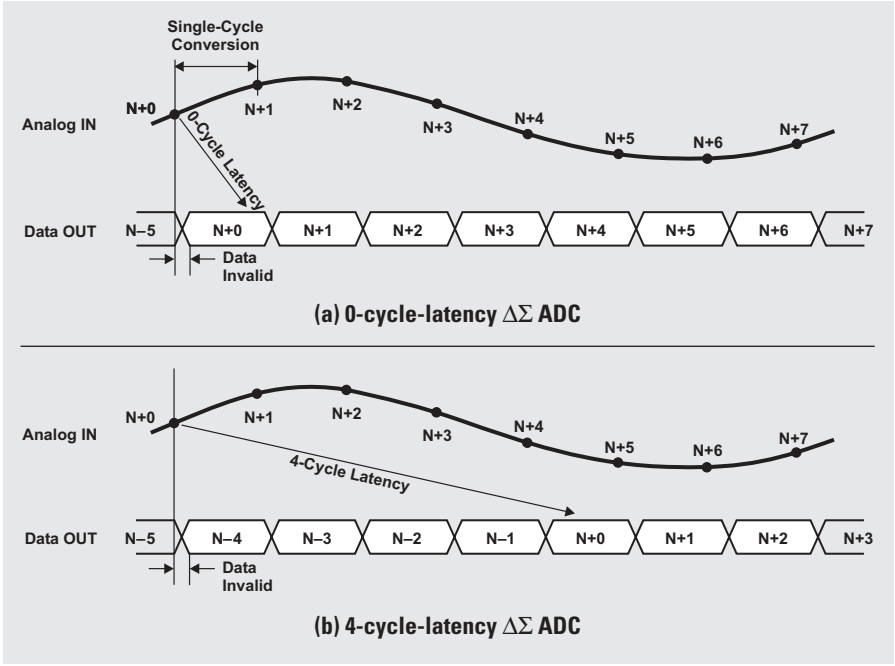
Figure 1. Example multiplexed sensor system



ADC cycle latency

For ADCs, cycle latency is the number of *complete* data cycles between the initiation of the input-signal conversion and the availability of the corresponding output data (see Figure 2). The unit of measure for this definition of latency is N-cycle latency, where N is a whole number. Figure 2 shows the timing diagrams for a 0-cycle-latency (or zero-latency) ADC and a 4-cycle-latency ADC. In Figure 2(a), with 0-cycle latency, the sampling period of N+0 is initiated. The output data of N+0 is acquired before the sampling period of N+1 is initiated. In Figure 2(b), with 4-cycle latency, the sampling period of N+0 is

Figure 2. Comparison of cycle-latency behavior of two ΔΣ ADCs



initiated. The output data of N+0 is presented after the completion of four conversion cycles.

Figure 3 shows zero-latency ADC behavior graphically. In Figure 3, the input signal is first acquired at t_0. The ΔΣ converter continues to acquire input samples through the sampling period and continually modulates the signal into a noise-shaped representation. The digital low-pass/decimation filter accumulates the noise-shaped signal and generates the output code at the end of the t_0 period. A ΔΣ converter has zero latency if data is available before a new sampling period is initiated. The output code represents the oversampled, filtered-input signal. At t_1 the converter initiates the next sampling period.

The successive approximation register (SAR) ADCs are capable of zero latency as are many ΔΣ converters. The better choice for the application shown in Figure 1 is a high-resolution, zero-latency ΔΣ ADC. Some data sheets for ΔΣ ADCs claim single-cycle conversions. This is another way of saying that a converter has zero latency.

Texas Instruments (TI) offers numerous multiplexed, zero-latency ΔΣ ADCs that provide low-noise, high-resolution solutions (see Figure 4). These ΔΣ converters are capable of masking the filter action and providing a fully settled signal before the end of one cycle. As an example, TI's 16-channel, 24-bit ADS1258 has an internal, fifth-order, sinc digital filter followed by a programmable, first-order averaging filter. When the converter is configured in its auto-scan mode, the cycle latency is zero. In the auto-scan mode, the ADS1258 scans through the selected channels automatically, with break-before-make switching.

ADC latency time

Latency time is typically viewed as the time required for an ideal step input to converge, within an error margin, to a final digital output value. This error band can be expressed as a predefined percentage of the total output-voltage step. The latency time of a conversion is the time between the beginning of the signal acquisition and the time when data is available to download from the converter. In contrast to the cycle-latency specification, the latency time (or settling time) is never equal to zero.

Figure 5 compares the latency-time performance of various multiplexed ΔΣ ADCs. The latency time of a zero-latency ΔΣ ADC varies from device to device, depending on the system clock and the order of the converter's digital filter. A requirement for larger applications is that the multiplexed ADC must quickly cycle through the channels. The latency time for these types of applications can be critical.

Figure 3. Typical input and output of zero-latency ΔΣ ADC

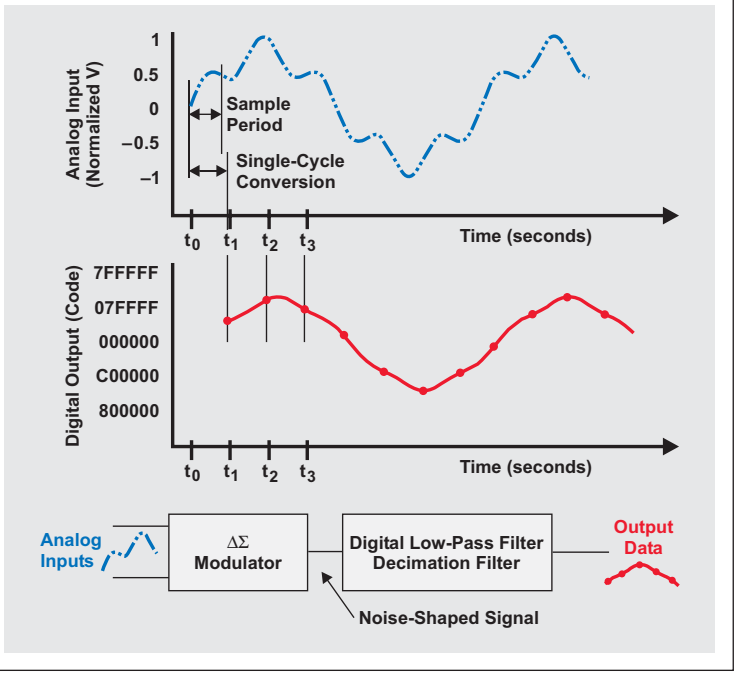


Figure 4. TI's multiplexed zero-latency ΔΣ ADCs

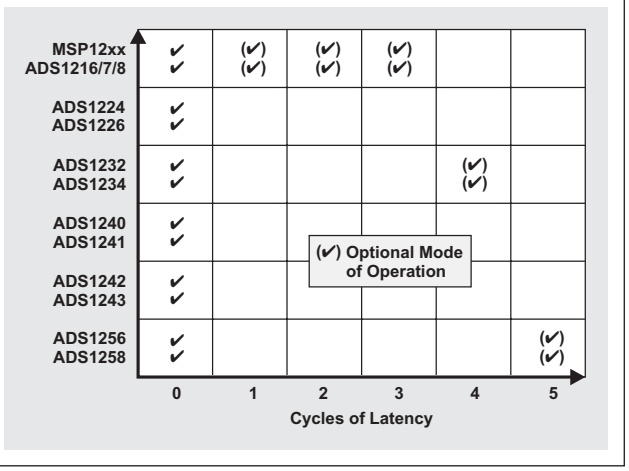
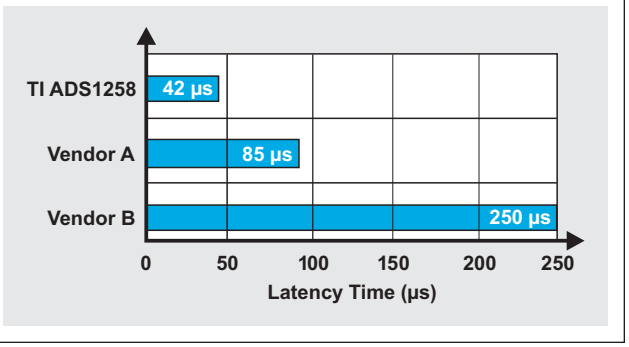


Figure 5. Latency-time comparison of ΔΣ ADCs



When the ADS1258 (Figure 6) is configured in its auto-scan mode (zero latency), the output data is fully settled at the end of each conversion. The minimum latency time in the ADS1258's auto-scan mode is 42 µs.

It is possible to reduce the throughput time of a zero-latency ΔΣ ADC if the intermediate or masked digital filter results are available. In this mode, the digital output results are not necessarily fully settled. For these devices the throughput time is always less than the latency time. Reduction of throughput time best suits sensors that produce small voltage changes at a slow rate (such as temperature sensors, pressure sensors, or load cells). With these types of sensors it might be advantageous to acquire several conversions and perform post-processing on the data.

When the ADS1258 is configured in its fixed-channel mode, the intermediate results from the fifth-order digital filter are available to the user. In the ADS1258 fixed-channel mode, the converter is no longer automatically cycling from channel to channel, and the output data may or may not be fully settled. The minimum throughput time of the ADS1258 in fixed-channel mode is 8 µs (⅛ of the fully settled latency time).

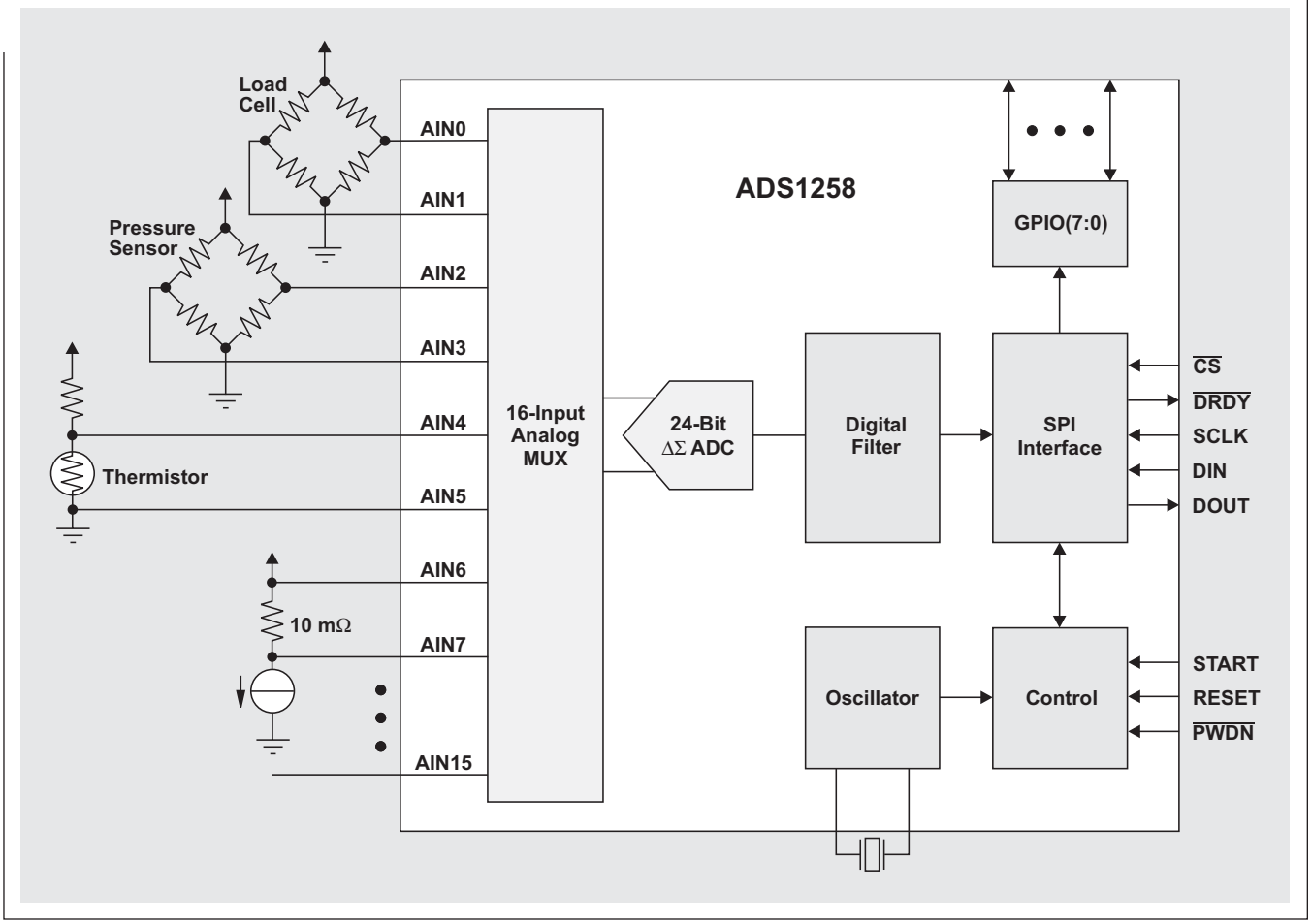
Conclusion

The economy and efficiency of using multiplexed ΔΣ ADCs for applications with multiple sensors must be weighed against possible problems caused by ADC conversion latency and any latency introduced by external processing. The TI ADS1258 offers 16-channel, 24-bit conversions with low noise and zero latency. The device's single-cycle, low-latency-time capability provides fully settled data at the end of each conversion cycle. In auto-scan mode, the ADS1258 can complete a conversion for all 16 channels in under 700 µs. Cycle latency and the total conversion time must be evaluated for each ADC considered to be sure the device will perform as intended.

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/ADS1258

Figure 6. The ADS1258, a 16-channel, zero-latency, 24-bit ΔΣ ADC



Enhanced-safety, linear Li-ion battery charger with thermal regulation and input overvoltage protection

By Jinrong Qian
Applications Manager, Battery Management Applications

The lithium-ion (Li-ion) battery is widely adopted in portable devices because of its high energy density on both a gravimetric and volumetric basis. Due to their simplicity, low cost, and small size, highly integrated linear battery chargers are widely used to charge single-cell Li-ion batteries. However, when unregulated adapters are used to power portable systems, it can be a challenge to remove or minimize the heat generated from the linear chargers and to maintain their operation within a safe thermal range. This article describes a newly developed battery charger with thermal regulation. This charger has input overvoltage protection (OVP), which alleviates thermal concerns while maximizing the charge rate and minimizing the charging time, allowing use of an unregulated adapter.

Battery-charging requirements

The charge profile widely used for charging Li-ion batteries consists of three charging phases: precharge; fast-charge constant current (CC); and constant voltage (CV). In the precharge phase, the battery is charged at a low rate when the cell voltage is below 3.0 V. Typically, when the cell voltage reaches 3.0 V, the charger enters the CC phase. The faster-charge CC is usually limited to stay below the cell's 1C rating. The cell cycle life decreases with charge rates above 1C because metallic lithium deposited on the node easily reacts with the electrolyte and is permanently lost. Finally, the charger enters the CV phase, where it maintains the peak cell voltage and then terminates charging when the charge current drops to a predefined level.

The cell capacity is a function of the cell voltage—the higher the voltage, the higher the capacity. However, higher cell voltage results in shorter cycle life. For example, charging a cell at 4.3 V can provide 10% more capacity, but cell cycle life may be 50% shorter. On the other hand, if the cell is undercharged at just 40 mV under the optimum voltage, it can have about 8% lower capacity. Therefore, a very accurate battery charge voltage is extremely important.

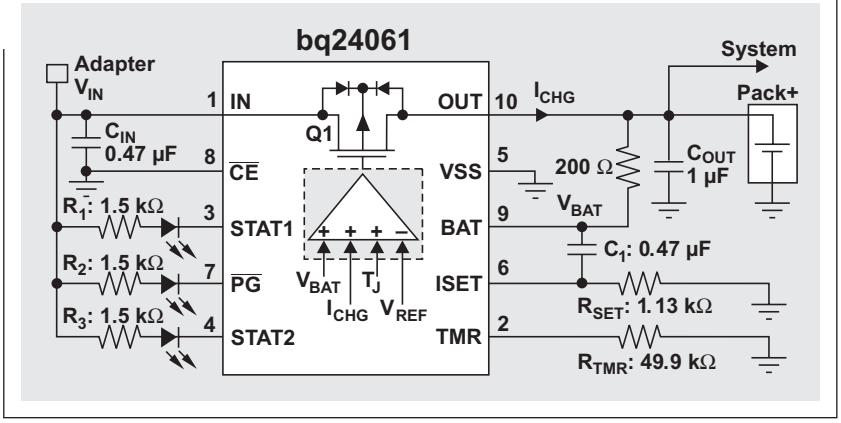
Thermal-regulated battery charger with input OVP

Figure 1 shows a low-cost, stand-alone linear battery charger circuit with thermal regulation and input OVP. The charger simply drops the adapter's DC voltage down to the battery voltage. The power dissipation in the linear charger is given by

$$P_{CHGR} = (V_{IN} - V_{BAT}) \times I_{CHG}.$$

There is a large difference between the input and battery voltages when the charger transitions from precharge to fast-charge mode, where the power dissipation reaches the maximum. For example, if a 5-V adapter is used to

Figure 1. Application circuit with thermal regulation and input OVP



charge a 1200-mAh Li-ion battery, it has a maximum power dissipation of 1.8 W with a 1-A charge current and a 3.2-V battery voltage. This power dissipation results in an 85°C temperature rise for a 3 × 3-mm QFN package with 47°C/W thermal impedance. The junction temperature exceeds the maximum allowed operating temperature of 125°C at 45°C ambient temperature. It is hard to maintain the junction temperature within a safe thermal range at the beginning of the charging. As the battery voltage rises during the charging, the power dissipation drops. After charging enters the CV mode, the power dissipation drops further as the charge current starts to taper down.

How do we improve the design to keep the charger operating in a safe thermal range? The more advanced battery chargers such as bq2406x and bq2403x have introduced a thermal regulation loop to prevent overheating of the charger. When the internal chip temperature reaches a predefined temperature threshold—for example, 110°C—any further increase of the IC temperature results in reduction of the charge current. This limits the power dissipation and provides thermal protection to the charger. The maximum power dissipation causing the IC junction temperature to reach thermal regulation depends upon the PCB layout, the number of thermal vias, and the ambient temperature. Figure 2 shows that after 1.2 seconds the thermal loop reduces the effective charging current from 1.2 A to 600 mA within 2 seconds.

Thermal regulation usually happens at the early stage of the fast charge, but if it is active during the CV mode, the charging current could prematurely reach the charge termination threshold. To prevent this false charge termination, the battery charge-termination function is disabled whenever the thermal regulation loop is active. In addition, the effective charge current is reduced, which increases the battery charging time and which, if the charge safety timer had a fixed setting, could terminate charging early. The bq2406x employs a dynamic safety-timer control circuit that effectively extends the safety time during thermal regulation and minimizes the chance of a safety-timer fault. Figure 3 shows that the safety-timer response is inversely proportional to the effective charge current in thermal-regulation mode.

When the battery-charging function is enabled, the internal circuit generates a current proportional to the real charging current set by the ISET pin. The voltage generated across resistor RSET reflects the charge current. This voltage can be monitored by the host for charge-current information.

There are several types of adapters used to charge Li-ion batteries. Less expensive adapters may not have well regulated output and have higher output voltages under no load than at the normal load. In addition, during the battery hot plug-in, the input voltage to the charger could reach as high as two times that of the adapter voltage due to resonance between the cable inductance and the input

Figure 2. Charge-current waveform under thermal regulation

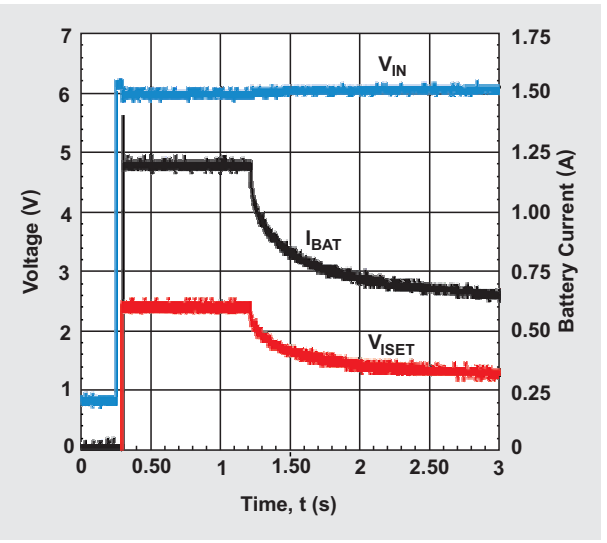
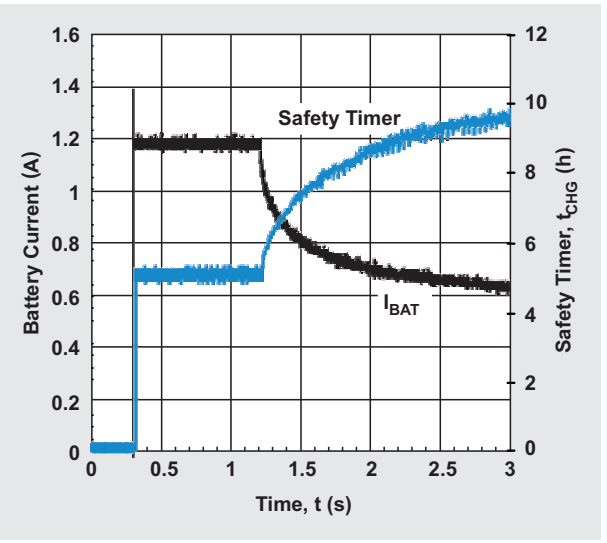


Figure 3. Dynamic safety timer in thermal regulation



capacitor of the battery charger. To increase safety when the input voltage is above the predefined threshold, the input OVP implemented in bq2406x chargers does not allow charging.

The LDO mode (with the TMR pin open) disables the charge-termination circuit and the battery-detection routine and holds the safety-timer clock in reset. This mode is often used for operation without a battery or in production testing.

Many applications require powering the system while charging the battery simultaneously. When the system is directly connected to the battery-charge output as shown in Figure 1, interaction between the system and charger may result in a false charge termination caused by the safety timer. Figure 4 shows a typical application circuit that eliminates such issues. There are two independent power paths, one to charge the battery and one to power the system. When the AC adapter is not available, the battery discharge MOSFET is turned on after a time delay set by R4 and C2 so that the battery will provide power to the system.

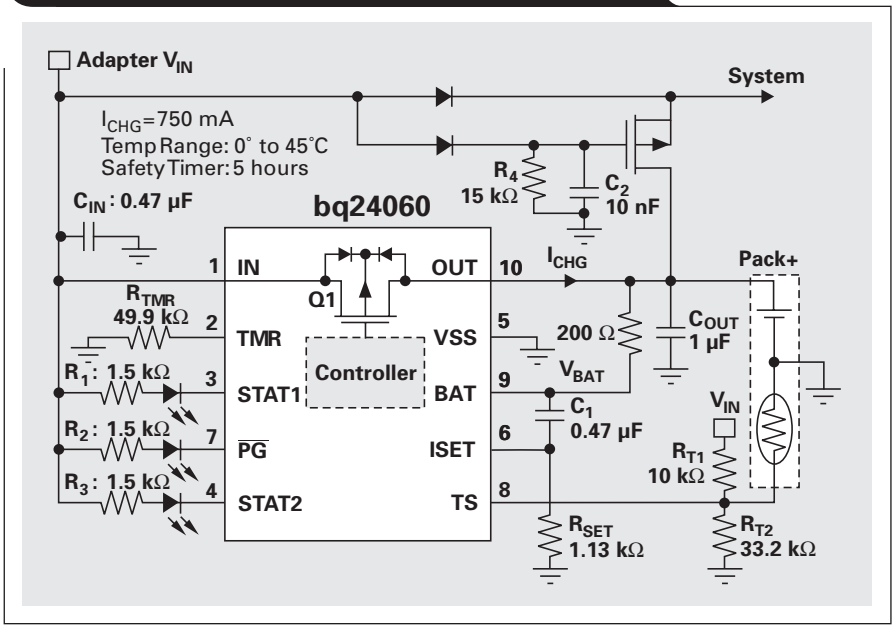
Summary

The linear battery charger with thermal regulation can significantly improve the thermal design and safety. With input OVP, it allows only authorized adapters to charge the battery, improving system safety.

Related Web sites

power.ti.com
www.ti.com/sc/device/bq24060
www.ti.com/sc/device/bq24061

Figure 4. Power-path-management battery charger



Current balancing in four-pair, high-power PoE applications

By Steven R. Tom
Systems Engineer, Power Interface Products

Introduction

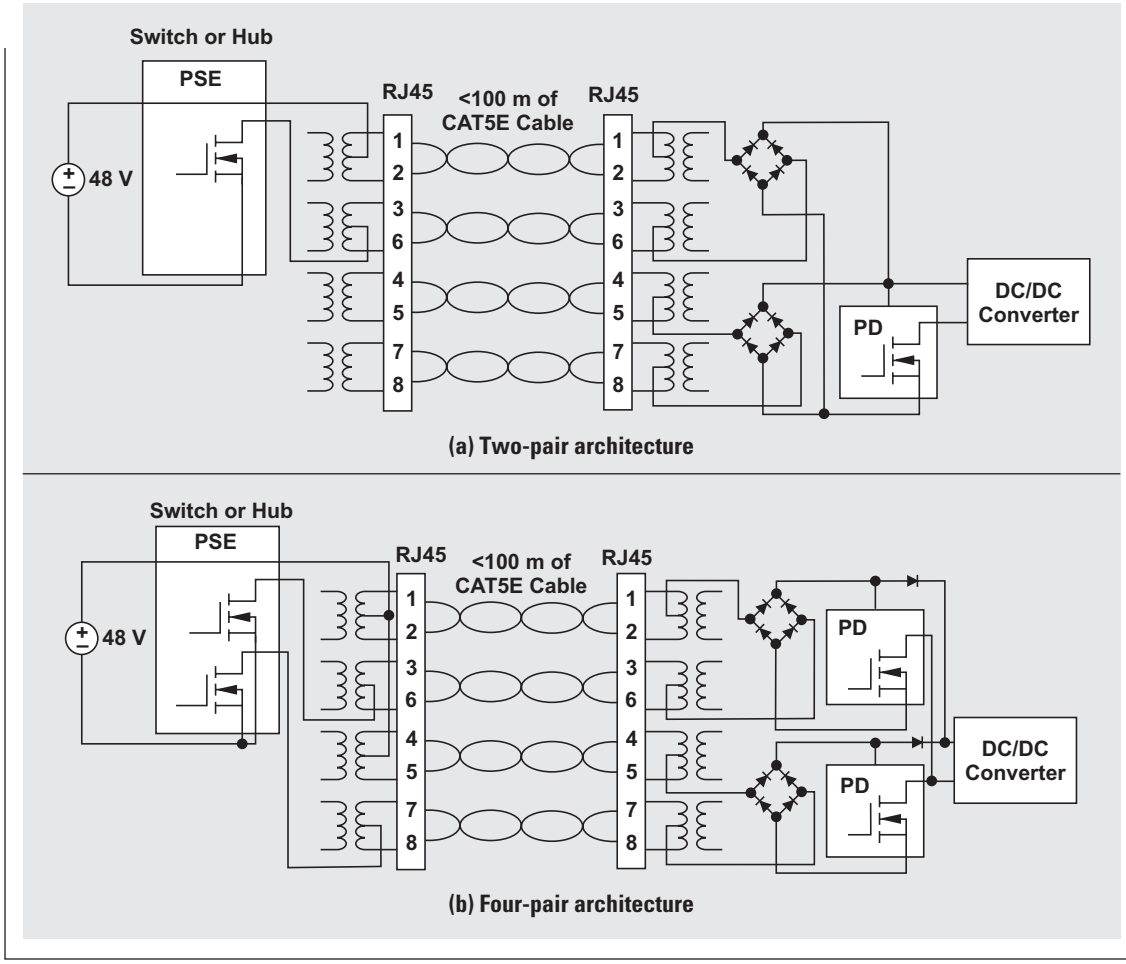
Power-over-Ethernet (PoE) parameters are specified by IEEE 802.3-2005 clause 33, which defines both the allowable architectures and the maximum deliverable power for a PoE system.[1] The present standard mandates a two-pair architecture allowing a maximum of 12.95 W at the end of the cable. As end equipment becomes more complex, it requires more power and architectures more flexible than the IEEE standard allows. This article describes a unique current-balancing technique that uses a four-pair architecture to deliver up to 50-W to the end equipment.

Review of PoE two-pair/four-pair architectures

An end-to-end PoE solution typically comprises a power source, referred to as "power sourcing equipment" (PSE), and end equipment, referred to as the "powered device" (PD). The PSE may be standalone or embedded in a router or switch. Most Ethernet cable used today is Category 5E (CAT5E) cable composed of four unshielded twisted pairs of copper.

Figure 1 shows the possible architectures that can be used to deliver power over CAT5E cable. The architecture in Figure 1a delivers power to the PD from the PSE in a single loop over two pairs of the CAT5E cable. The IEEE

Figure 1. Two possible architectures for power delivery to the PD



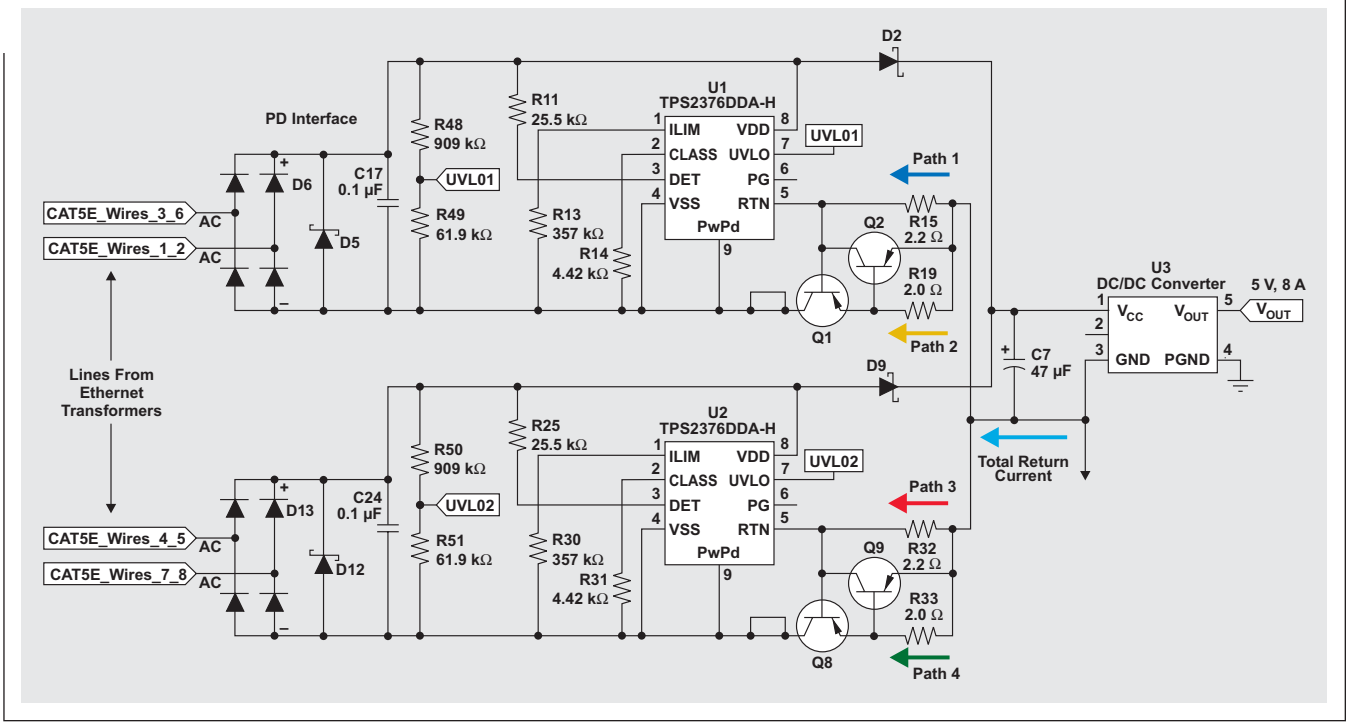
standard specifies that power may be delivered in a single loop over either of the two pairs but not over all four pairs simultaneously. Using two current loops over all four pairs, the architecture in Figure 1b increases the available power delivered to the input of the PD. The main advantage of the four-pair architecture is the increased number of conductors which decreases power loss and increases total power to the end equipment. The main disadvantages are the added cost and the increased complexity needed to ensure that the current is balanced between the two current loops.

In the four-pair architecture, both current loops feed a single DC/DC converter. If the impedances of each loop were identical, current balancing would be unnecessary and each loop would provide half of the needed input current to the DC/DC converter. However, mismatches in the wires, connectors, and components will naturally cause one loop to carry more current than the other. To ensure reliability, the series components in each current loop must be designed to handle the worst-case imbalance while maintaining data transmission. A larger imbalance implies an oversized (and thus more costly) design. Maximum power delivery can be obtained by balancing the current between the line pairs so that each path operates just below its current limit. The following design example and analysis show how the worst-case imbalance can be determined and minimized.

Design example with current-booster circuit

In a four-pair architecture, the detection and classification functions of the PD must be performed on each two-pair current loop, which necessitates the need for two PD controllers. In the design example that follows, two TPS2376-H controllers are used as the PD input source to the DC/DC power supply[2] (see Figure 2). The DC/DC power supply uses a UCC3809-2 in a single-switch flyback

Figure 2. Design example of four-pair architecture with current-booster circuit



topology to provide an isolated 5 V at 8 A to the load.

Table 1 shows the predetermined design specifications used for this design example. It is assumed that an available PSE will supply a regulated voltage between 51 and 57 V that is capable of sourcing up to 800 mA for each current loop consisting of two pairs of the CAT5E cable. A reasonable assumption for the loop impedance of each two-pair loop (maximum length of 100 m) is 12.5 Ω. The CAT5E cable will connect to the PD interface and input to the DC/DC converter that will provide an isolated 5 V at 8 A to the load. For simplicity and emphasis on the PD interface, the DC/DC power supply is shown in Figure 2 as a simple black box.

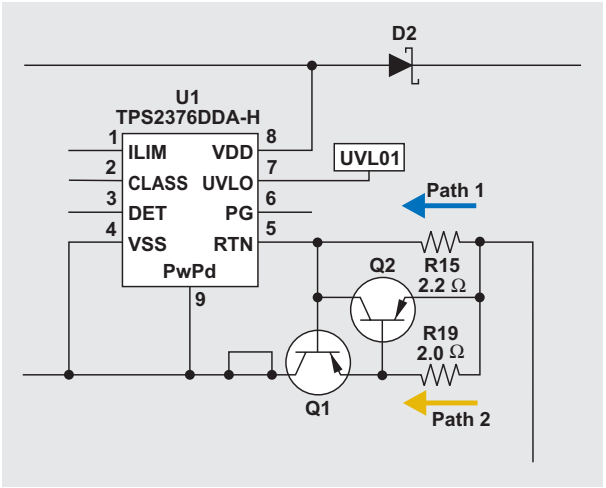
Assuming that the DC/DC converter is ~85% efficient, approximately 47 W of input power is needed. Depending on the CAT5E cable length and the PSE voltage, an input current between 0.825 and 1.2 A is required to meet the input-power specification.

The current limit of the TPS2376-H is listed in Table 1 because it is imperative that the current in either of the two current loops not exceed this value during operation to avoid unwanted shutdown. Because the minimum current limit of the TPS2376-H is 625 mA, the current-booster circuitry in Figure 3 was introduced to gain the full potential of the allowable 800 mA of input current per two-pair loop. In reality, the current is not boosted—it is merely shunted around the TPS2376-H. Figure 3 shows how the current-booster circuit works for one of the current loops. As the return current into pin 5 (RTN) on the TPS2376-H increases, the voltage drop across R15 increases, lowering the voltage between base and emitter sufficiently to turn on transistor Q1. Current through R15 will turn on Q1 when $V_{R15} > 0.7$ V. This allows Q1 to conduct and shunt a portion of the return current around the TPS2376-H. Q2 provides protection for Q1 during short-circuit and transient conditions by clamping the base of Q1 to its collector and forcing it off. Q2 will turn on when $V_{R19} > 0.7$ V, shunting some of the Q1 base current and eventually turning it off if the current continues to increase. For a more detailed explanation of this circuit, please see Reference 3.

Table 1. Design specifications

	MIN	TYP	MAX
PSE Voltage (V)	51	—	57
Impedance per Two Pairs (Ω)	—	12.5	—
Input Current per Two Pairs (A)	—	—	0.800
V_{OUT} (V)	4.95	5	5.05
I_{OUT} (A)	—	—	8.0
DC/DC Output Power to Load (W)	—	—	40
DC/DC Input Power (W)	—	—	47
DC/DC Efficiency (%)	—	85	—
DC/DC Input Current (A)	0.825	—	1.200
Current Limit (A) (TPS2376-H)	0.625	0.765	0.900

Figure 3. Current-booster circuit for one current loop



Modeling the four-pair architecture within PSPICE

To ensure that the design will current share appropriately, it is necessary to model the four-pair architecture within a simulation tool such as PSPICE. The key elements that need to be modeled are the sources of impedance in series with each current loop; i.e., the diode bridge, the CAT5E cable resistance, and the series resistances of the TPS2376-H pass FETs and booster circuitry. Table 2 correlates the actual schematic in Figure 2 with the PSPICE simulation schematic in Figure 4.

The simulation models the PSE as an ideal DC voltage source, the DC/DC power supply as an ideal DC current source, and the CAT5E cable and PD interface as the four current paths. The color-coded paths in Figure 4 correspond to those shown in Figure 2. Modeling the PSE as an ideal voltage source and the DC/DC power supply as an ideal DC current source are reasonable assumptions that simplify the simulation significantly and allow the analysis to focus on the current balancing of the CAT5E and PD circuitry.

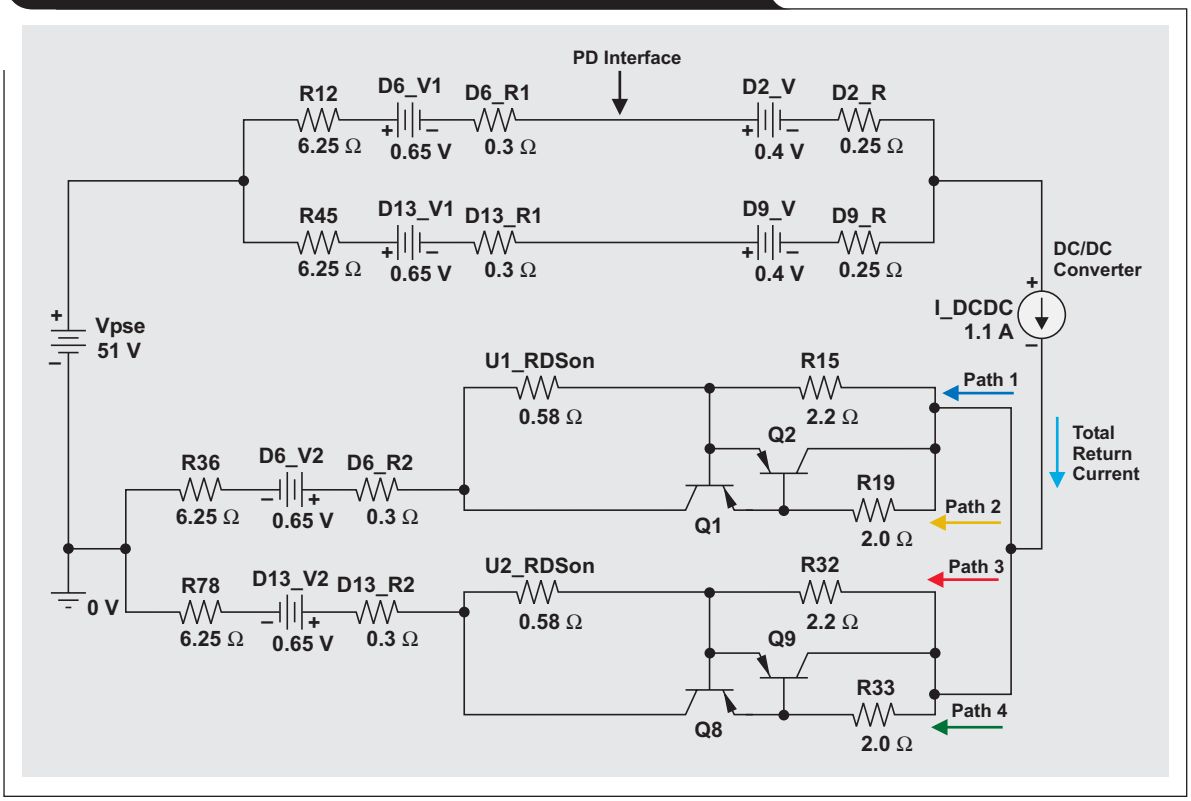
As stated earlier, in an ideal circuit the current would be equal in each current path because each path contains the same components. However, imbalances do arise because of variations in diode forward voltage drops, cable resistance, and pass FET on resistances. PSPICE allows for examination of the ideal case where matched components are used and the current in each current loop is balanced. The simulation is made by sweeping the current in the DC current source, I_DCDC, and recording the current in each of the two current loops and the power delivered to the DC current source. The power delivered to the DC current source represents the input power to the DC/DC converter. (If the efficiency of the DC/DC power supply is known, it can be multiplied by the input power to calculate the actual power to the load.) Within each current loop, it is important to make sure that the current through the pass FET of each TPS2376-H device is less than the 625-mA current-limit threshold and that the total current in either current loop does not exceed 800 mA.

A second variable that must be considered is the length of the CAT5E cable. The IEEE standard allows for a

Table 2. Modeling of four-pair architecture

ACTUAL SCHEMATIC (Figure 2)	PSPICE SIMULATION SCHEMATIC (Figure 4)
U1	U1_RDSon (pass FET on resistance)
U2	U2_RDSon (pass FET on resistance)
D6	D6_V1, D6_V2, D6_R1, D6_R2
D13	D13_V1, D13_V2, D13_R1, D13_R2
D2	D2_V, D2_R
D9	D9_V, D9_R
CAT5E cable resistance	R12, R45, R36, R78
PSE input voltage	Vpse
DC/DC power supply	I_DCDC
Q1, Q2, Q8, Q9, R15, R19, R32, R33	Q1, Q2, Q8, Q9, R15, R19, R32, R33

Figure 4. Balanced PSPICE circuit for load-share simulation



maximum of 100 m of Ethernet cable between the PD and PSE.[1] Figure 5 shows the simulation results for the corner areas of 100 m and 1 m of cable length when the model cable resistances (R12, R45, R36, R78) are modified. All simulations are done at the minimum PSE voltage of 51 V because input current is highest at this condition.

The simulation results confirm that when matched, the current loops will load share identically as Path 1 overlaps Path 3 and Path 2 overlaps Path 4. As input power increases above 25 W, the current-booster circuitry begins turning on and a portion of the current in each current loop is shunted around the TPS2376-H. The largest current handled by either TPS2376-H device is ~465 mA when the input power to the DC/DC power supply is 48 W and 100 m of cable connects the PD to the PSE. The largest current in either of the two-pair current loops is 599 mA (465 mA + 134 mA). This simulation result is acceptable because the maximum TPS2376-H current is less than the 625-mA current limit and the maximum current in either of the two-pair current loops is less than 800 mA.

Understanding sources of loop-impedance mismatch

To ensure reliable performance, it is important to understand the sources of loop-impedance mismatch so that worst-case imbalances can be entered into the simulation and analyzed. The simulation circuit in Figure 6 takes into account maximum variations in diode forward voltage, 1% resistor tolerances, and maximum pass FET on-resistance tolerances. Also, the maximum cable length resistance tolerance of 3% was used in accordance with the IEEE standard.

Figure 5. PSPICE simulation of balanced current sharing

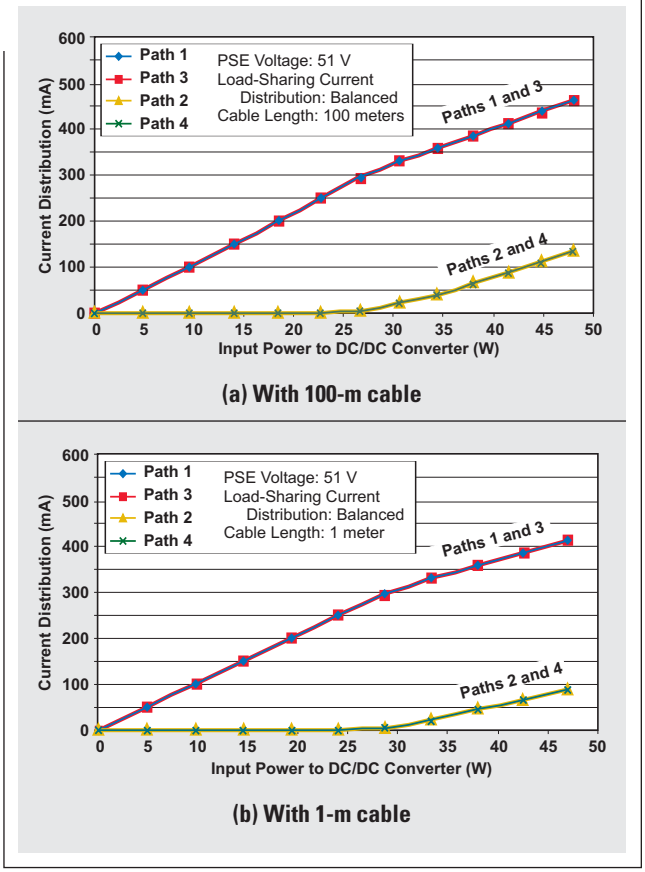
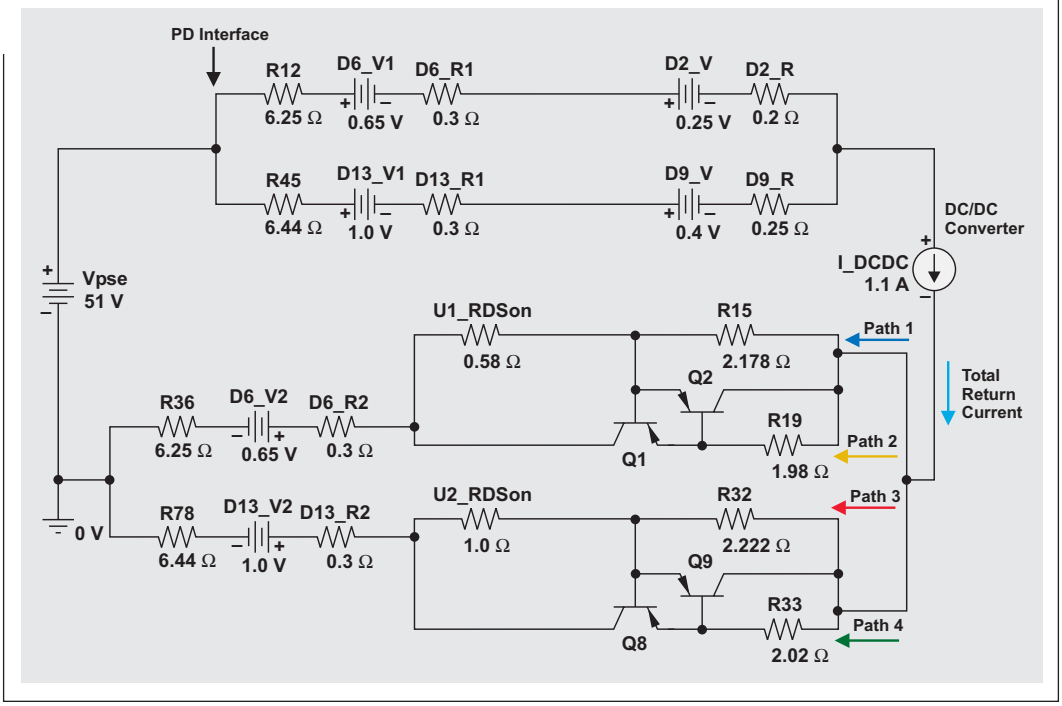


Figure 6. Unbalanced PSPICE circuit for load-share simulation



The values were adjusted so that all impedance mismatches were in one current loop, allowing for the largest imbalance. The four-pair architecture simulation previously discussed was run a second time to determine the extent of current imbalance in each current pair.

Figure 7 shows that the largest current through either of the TPS2376-H devices is 488 mA with a 100-m cable and 498 mA with a 1-m cable. The largest current available (in this example, Path 1 plus Path 2) is 640 mA with a 100-m cable and 660 mA with a 1-m cable. Because the worst-case current imbalance exceeds neither 625 mA through the TPS2376-H nor 800 mA in one current loop, the design remains within the original design specification.

Board-level results

To verify that the simulations are accurate, an evaluation board was built and tested. Figure 8 shows the current in each of the current loops when measured in an ideal lab setting at 25°C ambient temperature. These board-level results demonstrate a current imbalance through each TPS2376-H of only 10 mA (2.1%) with a 100-m cable and 1 mA (0.2%) with a 1-m cable.

To emulate worst-case conditions, the evaluation board was retested with a diode and resistor in series with the return path of the R78 current loop (Paths 3 and 4). The forward voltage drop of the diode (0.7 V) and an additional 0.5-Ω resistance were added to compensate for worst-case

Figure 7. PSPICE simulation of unbalanced current sharing

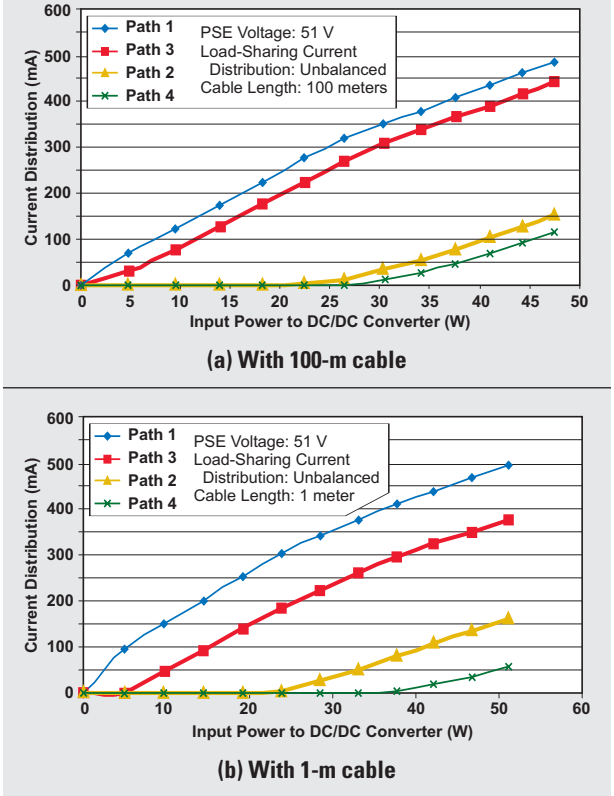
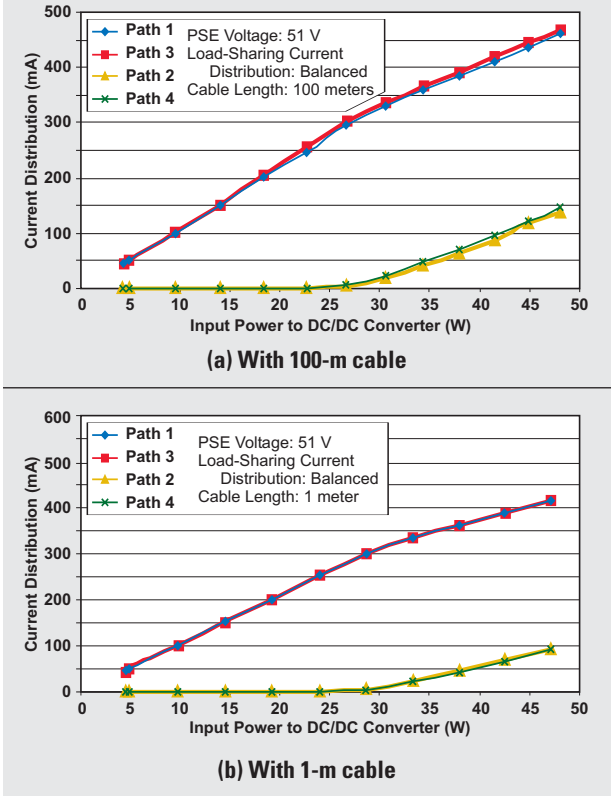


Figure 8. Board-level test results of balanced current sharing



diode forward voltage variations and system resistance tolerances. This permitted a reasonable board-level test to be conducted to measure actual current-loop imbalances.

Figure 9 shows that the largest current through either of the TPS2376-H devices is 488 mA with a 100-m cable and 484 mA with a 1-m cable. The largest current available (in this example, Path 1 plus Path 2) is 648 mA with a 100-m cable and 640 mA with a 1-m cable. Because the worst-case current imbalance exceeds neither 625 mA through the TPS2376-H nor 800 mA in one current loop, the design remains within the original design specification.

Conclusion

Overall, both simulation and board-level results confirm that the current-booster circuit will meet the initial design requirements for current balancing by keeping the return current through each TPS2376-H under its minimum current limit and under the maximum current allowable in the CAT5E Ethernet cable. The addition of the current-booster circuit improves the current balancing between the two current loops so that the wire, connector, and component tolerances do not cause the design to fall out of the design specifications.

References

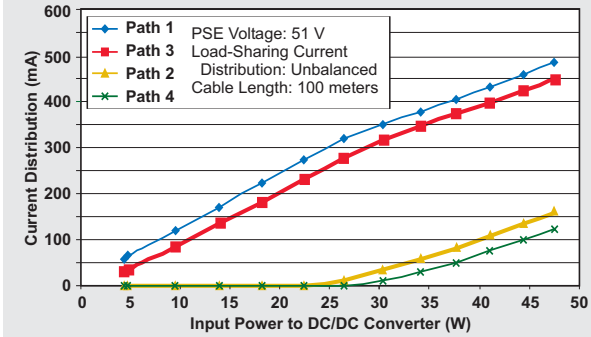
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. IEEE 802.3 standard, http://standards.ieee.org/getieee802/802.3.html	—
2. "IEEE 802.3af PoE High Power PD Controller," TPS2376-H Datasheet	slvs646
3. Martin Patoka, "High-Power PoE PD Using TPS2375/77-1," Application Report	slva225

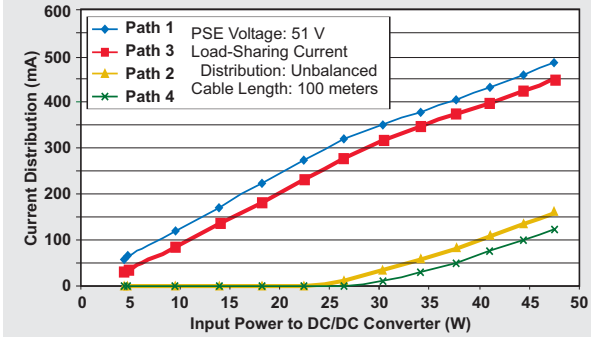
Related Web sites

power.ti.com
www.ti.com/sc/device/TPS2376-H
www.ti.com/sc/device/UCC3809-2

Figure 9. Board-level test results of unbalanced current sharing



(a) With 100-m cable



(b) With 1-m cable

Enabling high-speed USB OTG functionality on TI DSPs

By Dan Harmon
Product Line Marketing Manager, Digital Interface Products

High-speed USB On-The-Go (OTG) enables connectivity between portable consumer electronic devices over the industry's most popular peripheral interface, USB. Currently, USB devices require a PC host—laptop or desktop—to transfer data. High-speed USB OTG removes the need to find a bulky PC host to transfer pictures, music, and data to/from a cell phone, digital camera, MP3 player, memory stick, etc. Power is not much of an issue with today's PC host-centric USB, but is of increasing concern as portable devices take on more functionality and the demand for longer battery life increases. The problem of USB direct connection and power-management complexities is solved with the new USB 2.0 high-speed OTG controllers and power-management devices from Texas Instruments (TI). These devices allow developers to add full high-speed OTG capability to their platforms in small-form-factor, low-power designs. TI's OTG devices are available with a muxed NOR-flash or VLYNQ host interface for easy connectivity to TI's OMAP processors and many other DSPs.

What is USB OTG?

The terms USB 1.1, USB 2.0, USB OTG, WUSB, and OTG are all in common use today. In many cases they have created confusion among engineers and end users. The original USB 1.0 specification was released in January 1996. It defined two speeds for devices, low speed (LS) at 1.5 Mbps and full speed (FS) at 12 Mbps. The specification was revised in July 1998 and released as USB 1.1 with major clarifications/updates. In April 2000, the specification underwent a major revision and was released as USB 2.0, the current version that fully superseded USB 1.1. The beauty of USB 2.0 is that it maintains full backwards compatibility with USB 1.1 devices. However, it adds a much needed third speed node, high speed at 480 Mbps, while keeping support for both low speed and full speed. In July 2003, the USB OTG addendum was released, defining a new class of devices for portable, battery-powered products with limited host capabilities. Finally, in May 2005, the Wireless USB (WUSB) specification was released.

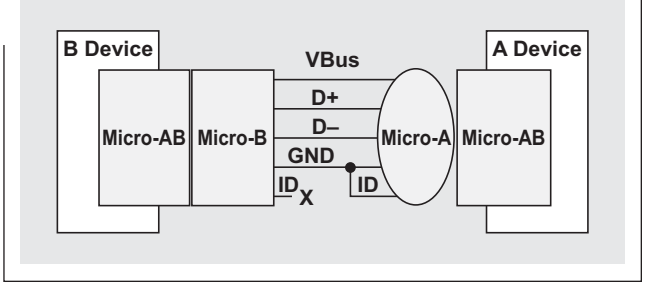
USB OTG is an addendum to the USB 2.0 specification that defines a new class of devices that extends the functionality of a peripheral product to include limited host capabilities. As the name implies, the original target of the specification was consumer portable devices with which end users may have wanted to share data when a computer was not available. Usage examples included sharing contact information between two PDAs or cell phones, sharing pictures from one digital still camera or camera phone with another, or printing directly from a digital still camera or PDA. Like standard USB, OTG is a point-to-point, host-centric bus and is not intended as a peer-to-peer networking connection. An OTG product must act as a standard peripheral when connected to a standard USB host such as a PC. The OTG addendum mainly addresses how a device must act when it is in host mode.

Just like a standard USB host port, an OTG host must supply power; but the required supply current is limited to 8 mA. Unlike a standard USB host in a PC, an OTG device may not have a simple way to add drivers for "unrecognized" devices. Therefore, an OTG device must supply what is called a Targeted Peripheral List (TPL), which allows device manufacturers to specify exactly what peripherals they will support. The specification also mandates messaging that will communicate to the end user that an unsupported device has been plugged in and will not work. This messaging can be as simple as an LED or as complex as a text display.

Since the target end products were primarily small portable consumer electronics, a standard USB connector was too large. Therefore the USB Implementers Forum introduced new mini and micro connectors. The mini-B connector has been in common use as a small-form-factor receptacle on many USB peripherals. The micro-AB receptacle is what a dual-role OTG device must use. This connector accepts either a micro-A plug or a micro-B plug. The orientation of the cable determines which device in an OTG connection acts as the host (A side) and which acts as the peripheral (B side), as shown in Figure 1. The new connector has an additional pin (ID) that is left open on the micro-B plug and is grounded in the micro-A plug to determine initial roles.

Although cable orientation determines which role, host or peripheral, each OTG device will initially assume at connection, the roles can be reversed via a dynamic switching method called Host Negotiation Protocol (HNP).

Figure 1. Cable orientation determines initial state

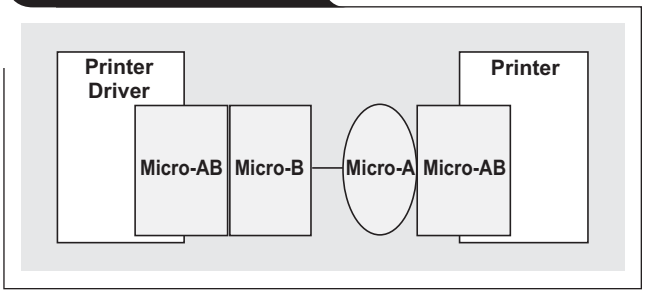


Why switch roles? The need for this can be understood if we look at Figure 2 and consider that every OTG device must include a TPL. The device on the left has the printer on its TPL, but it is *not* on the printer's TPL. If the user plugs in the cable backwards as shown in Figure 2, then communication between the two devices will not be possible without reversing the roles. HNP allows the roles to be reversed silently and automatically, thus enabling the communication and enhancing the end-user experience by eliminating the need to disconnect the cable and reverse it.

Session Request Protocol (SRP) is a method for turning bus power off/on at the discretion of the host device to save power when communication is not needed. Many of the target devices for OTG are battery-powered. Extending battery life is of utmost importance to both the manufacturer and the end user. With this in mind, the A device (as indicated by cable orientation) in an OTG connection can power off the bus and go into a sleep mode, extending battery life. This also allows the B device to go to sleep if it so desires. However, if the end user desires the communication to start up again and initiates this request on the B device, SRP allows the B device to request the A device to turn on VBus power and start a session. An OTG session is defined as the time during which the A device is furnishing VBus power. To wake up the A device, the B device pulses first the D+ wire and then the VBus wire. The A Device, which can respond to either pulsing, detects the pulse, causing it to switch on VBus and start a session.

SRP is more complex than this simple illustration. The B device, for example, must first measure VBus to ensure that a session is not in progress. It must also be able to differentiate between a classic PC or an OTG device at the other end of the cable. It does this by delivering measured amounts of current to the VBus wire and noting the resulting voltage.

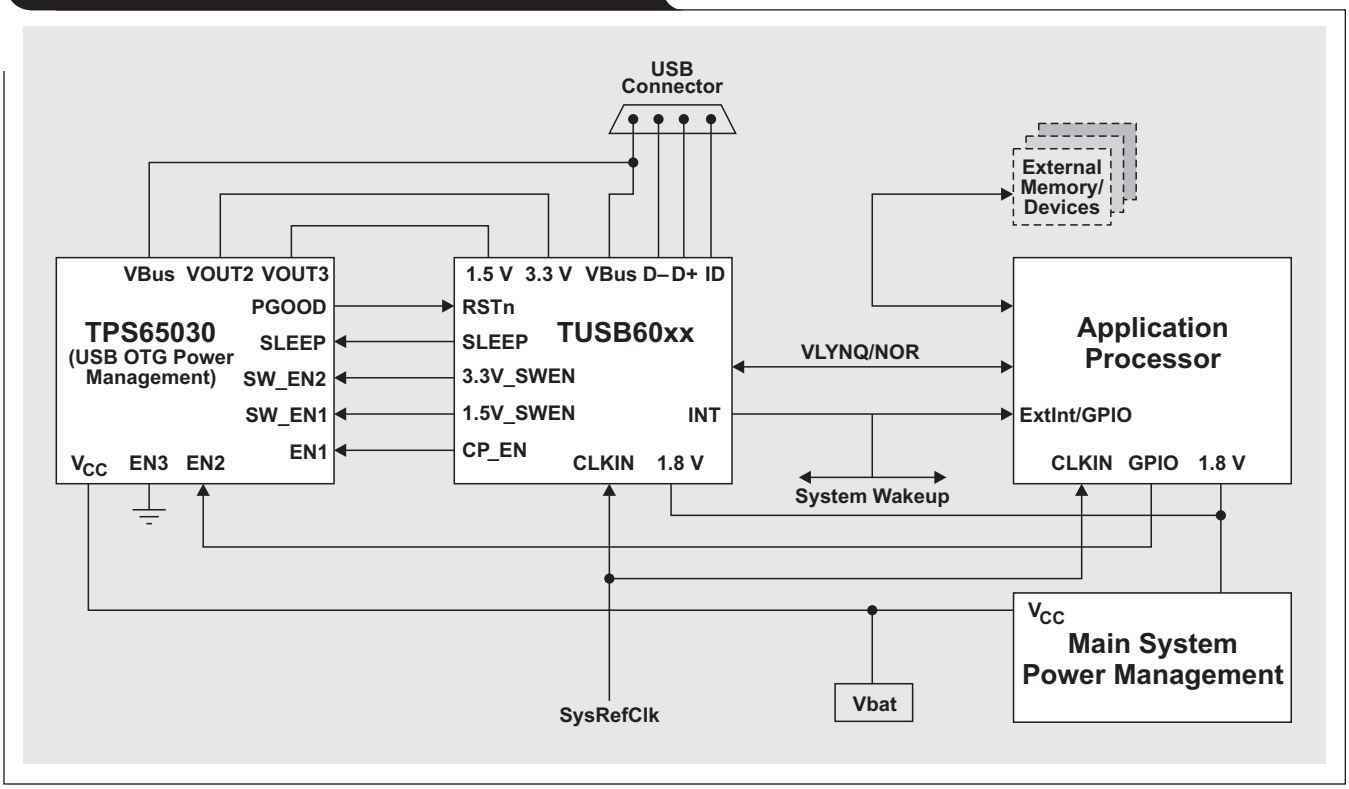
Figure 2. HNP example



TUSB60xx: The family of high-speed, OTG-interface-solution devices

This family of devices enables application processors (DSPs, OMAP™, and MCUs) that do *not* have integrated USB cores to function as either a USB 2.0 high-speed peripheral, an embedded USB 2.0 high-speed host controller, or a full USB 2.0 high-speed OTG device. The TUSB60xx devices serve as bridges between a USB 2.0 high-speed bus and a local processor host interface. Figure 3 shows a typical system implementation. The TUSB60xx family is

Figure 3. TUSB60xx typical system implementation



fully compliant with high-speed USB OTG. These devices come in a space-saving 5 × 5-mm MicroStar Junior™ BGA package and support an ultralow-power idle mode that consumes less than 100 µA. Both of these features are critical to small portable consumer devices that feature USB OTG. An application processor is required to support software needs. These include the operating system for host mode, the drivers for the TPL devices when they are in OTG host mode, and the application functionality when the TPL devices are in peripheral mode. A summary of the TUSB60xx family's features and benefits is given in Table 1.

The TPS65030 is a companion power-management device to the TUSB60xx devices. In addition to providing all of the power requirements of the TUSB60xx, it can provide 5 V at 100 mA on the VBus line when a TUSB60xx device is in OTG host mode.

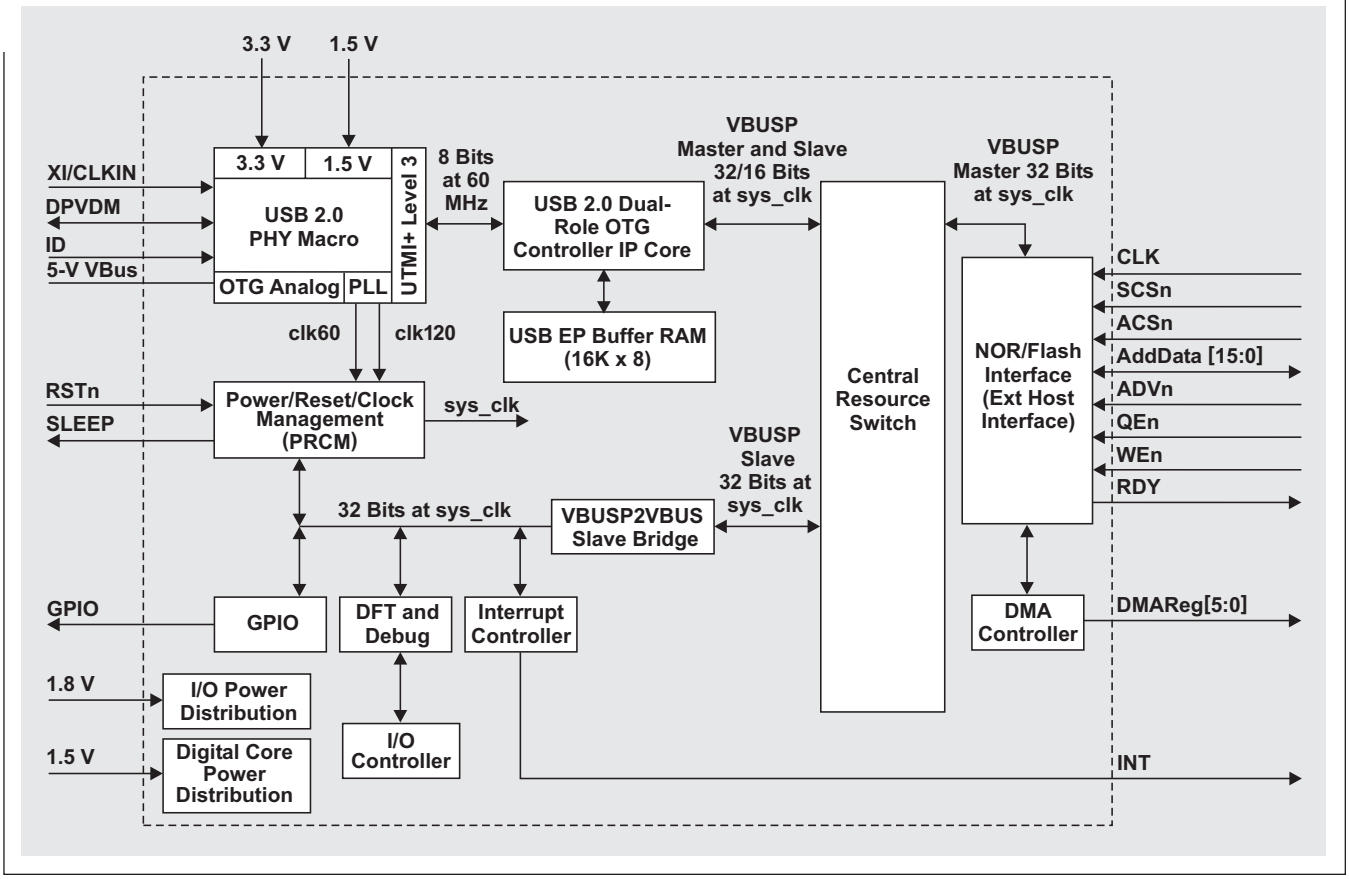
The first two members of the TUSB60xx family are the TUSB6010B and the TUSB6020. The only difference between the two devices is the external processor interface.

The TUSB6010B (Figure 4) features a 16-bit muxed NOR-flash interface that supports both synchronous and asynchronous transfers. The TUSB6010B supports single and burst read/write access with a programmable burst size of up to 16 half words. It can also support 6 external direct-memory-access (DMA) requests. The TUSB6010B will gluelessly interface to the OMAP1710 and the OMAP2420 processors. When the device is used with the OMAP2420 with the GPMC running at 55 MHz, the throughput measures a sustained 250-Mbps bulk input and bulk output with DMA. When the TUSB6010B is connected to the OMAP1710 with the external memory interface running at 55 MHz, the throughput measures a sustained 250-Mbps

Table 1. TUSB60xx family

Features	Benefits
• USB 2.0 high-speed, OTG-compliant device	• Certified compliance and interoperability
• Multiple external processor interface options	• Flexible architectures to interface to multiple processors
• Ultralow-power (<100-µA) idle mode; small form factor = 5 x 5-mm MicroStar Junior™ BGA	• Designed to meet the critical demands of portable, battery-powered target devices

Figure 4. TUSB6010B block diagram



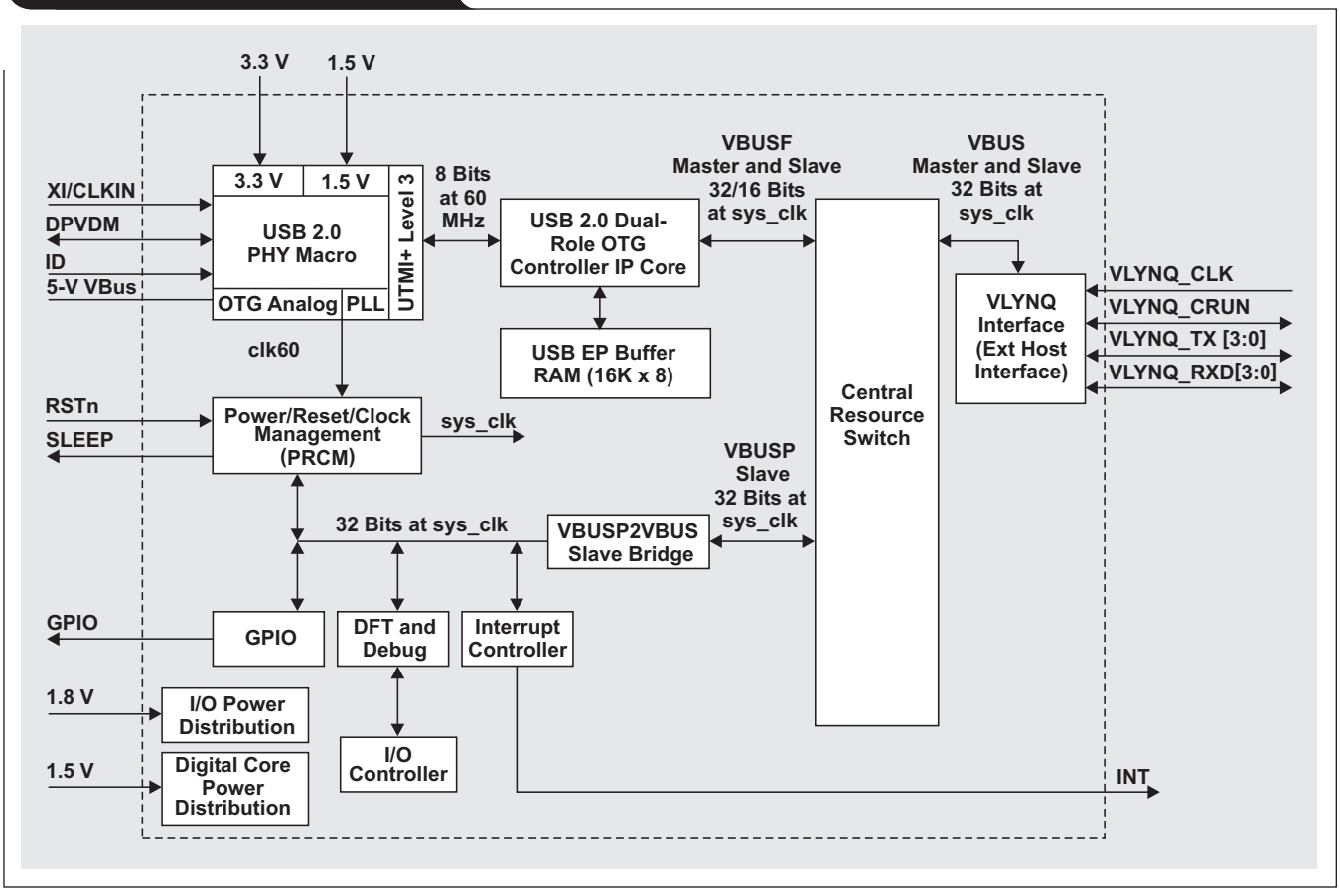
bulk output with synchronous DMA and a sustained 100-Mbps bulk input with asynchronous DMA.

The TUSB6020 (Figure 5) features a VLYNQ interface, which is a high-speed, low-pin-count, point-to-point serial specification developed by TI. The TUSB6020 features a 10-pin interface supporting 4 receive lines and 4 transmit lines that run at 150 MHz. It works as a memory-mapped master/slave interface with a multichannel DMA controller. The integrated list processor is capable of parsing CPPI 3.0-compliant buffer descriptors. The TUSB6020 will gluelessly interface to any TI processor that supports a VLYNQ interface. These processors include (but are not limited to) the DaVinci™ family, the DM320, and the OMAP5912. Utilizing an 8-pin VLYNQ interface running at 125 MHz, the TUSB6020 will enable a sustained 267-Mbps bulk input and bulk output.

Related Web sites

interface.ti.com
www.ti.com/davinci
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with OMAP5912, TUSB6020, or TPS65030

Figure 5. TUSB6020 block diagram



New zero-drift amplifier has an I_Q of 17 µA

By Thomas Kugelstadt
Senior Systems Engineer, Industrial Systems

Micropower applications require not only a very small offset and offset drift but also very low noise. Such applications include instrumentation front ends in biomedical electronics, conditioning stages in CO_2 detectors, and electronic sensor interfaces in precision metrology equipment. A front-end, low-noise amplifier combined with signal-conditioning circuits and a sensor forms a microsystem that often has to either be portable or stand alone and is therefore battery-powered. Hence, the power consumption has to be small. It is therefore crucial to eliminate the 1/f (flicker) noise and to reduce the overall noise down to the fundamental thermal noise, which is mainly determined by the allowable current consumption of the input stage.

While an auto-zero amplifier (AZA) removes its offset and 1/f noise at the cost of a raised white-noise level in the baseband, a chopper-stabilized amplifier reduces its baseband noise to the initial white-noise level but generates large output ripple instead. Because the input-stage noise is inversely proportional to its quiescent current, $e_n^2 \approx 1/I_Q$, an AZA often requires a significant increase in I_Q to achieve the desired noise levels after noise folding. Since this increase counteracts the requirements of a micropower amplifier, it is desirable to use a chopper-stabilized amplifier in micropower applications and to find some way to filter the output ripple.

This article describes a new, micropower, low-noise, chopper-stabilized operational amplifier, the OPA333, which operates from a 1.8-V supply, requiring a quiescent current of only 17 µA.

Overview

The OPA333 consists of a high-precision path (g_{m1}, g_{m2}, and g_{m3}) in parallel with a wideband path (g_{m4} and g_{m3}) (see Figure 1). The precision path ensures a high open-loop gain, A_{OL}, of 130 dB, while the wideband path provides a 350-kHz gain bandwidth at a phase margin of 60° (Figure 2). An internal, patent-pending notch filter removes chopper noise by a factor of more than 500, yielding a voltage-noise spectral density of 55 nV/√Hz across a 20-kHz bandwidth (Figure 3).

Figure 1. Internal block diagram

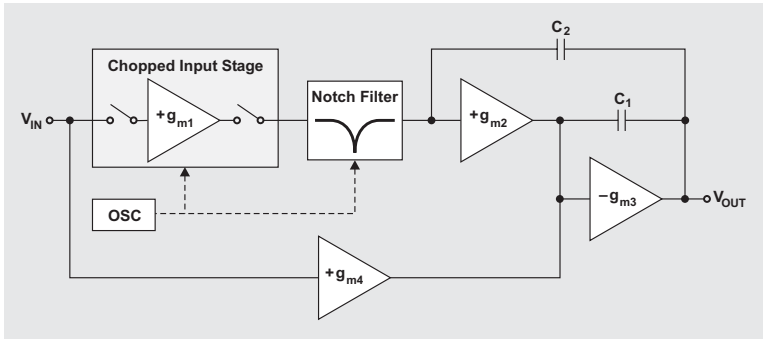


Figure 2. Open-loop gain and phase versus frequency

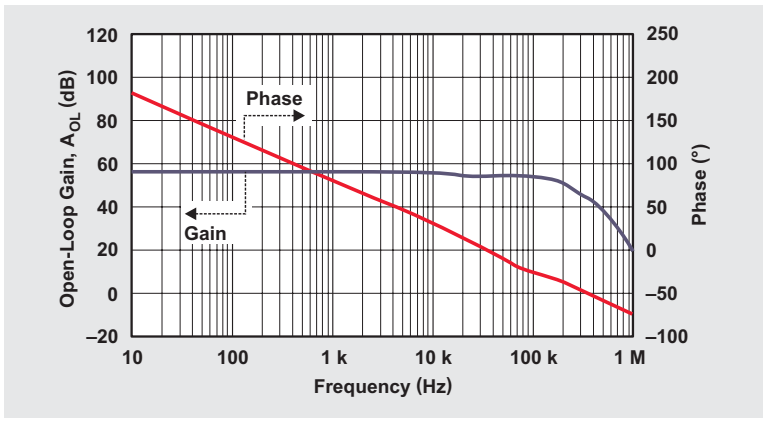
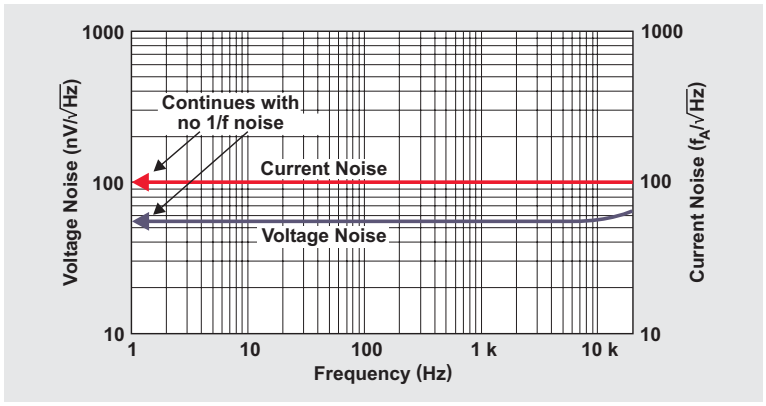


Figure 3. Noise densities versus frequency



With typical values for offset and drift of V_{OS} = 2 µV and dV_{OS}/dT = 20 nV/°C, respectively, the OPA333 also generates only 1.1 μV_{pp} of instantaneous noise in the 0.01- to 10-Hz band. The device offers rail-to-rail input and output and is available in SC70 and SOT23 packaging. Operation is specified from –40°C to 125°C.

OPA333 design rationale

The remainder of this article explains the underlying principles of the OPA333 design, describing the functional blocks and their individual contributions to the overall performance of this remarkable amplifier.

Offset cancellation of a wideband amplifier in general

Reducing the input offset voltage of a wideband amplifier, A_W, typically requires the support of an additional stabilizing or nulling amplifier, A_N, which is connected in parallel to the main amplifier (Figure 4). The stabilizing amplifier must be able to cancel its own offset, thus resembling an ideal amplifier. In addition, its open-loop gain has to be significantly larger than $A_N >> A_W$. This is usually achieved by using a multistage amplifier whose input gain is identical to A_W and whose output gain is G, with G >> 1. Note that the nulling amplifier can use chopping or auto-zeroing to null its own offset.

The output voltage of the circuit in Figure 4 is given by

$$V_{OUT} = V_W + V_N = A_W \times (G+1) \times \frac{V_{IN} + V_{OSW}}{G+1}.$$

Assuming G >> 1 and substituting $A_W G$ with A_N yields the effective open-loop gain and input offset for the amplifier model in Figure 5:

$$V_{OUT} = A_N \times \frac{V_{IN} + V_{OSW}}{G}.$$

Figure 4. Offset cancellation principle

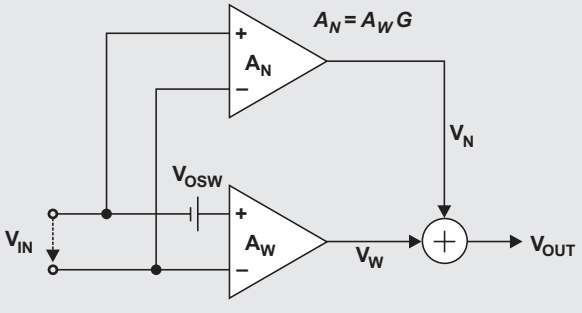
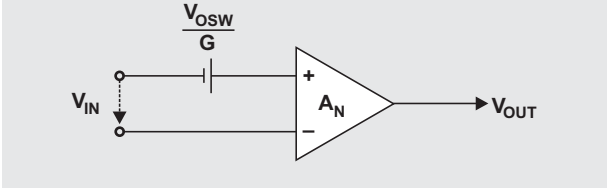


Figure 5. Effective amplifier model



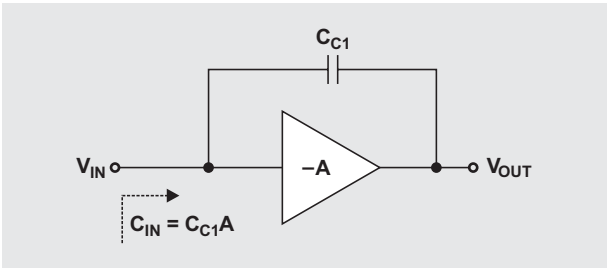
Thus, the DC gain has increased by factor G, from A_W to A_N, while the input offset of the wideband amplifier is reduced by G (typically 60 dB).

Multistage stabilizing amplifier

Large capacitance values are required to achieve low dominant pole frequencies. We recall that Miller compensation is used in op amp design to reduce these large values down to a size feasible for on-chip integration. Miller compensation relies on the effect that the input capacitance of an amplifier, C_{IN}, appears to be A times larger than the actual capacitance in the feedback loop, C_{C1}, with A being the amplifier gain (see Figure 6).

Because the precision path requires significantly higher gain than the wideband path, a three-stage cascade structure is used to provide that gain while allowing operation from very low supply voltages. If we neglect the chopper mechanism and the notch filter in Figure 1, the stabilizing

Figure 6. Miller effect: $C_{IN} = C_{C1}(A + 1)$. For A >> 1: $C_{IN} \approx C_{C1}A$.



amplifier that remains is a three-stage, nested Miller-compensated (NMC) cascade amplifier as shown in Figure 7.

Miller compensation provides the additional valuable feature of frequency-response shaping through a process known as *pole-splitting*. Figure 8 shows the frequency response of an uncompensated three-stage amplifier with its pole frequencies f_{p1}, f_{p2}, and f_{p3}. Through careful design of the g_m stages and appropriate selection of the Miller compensation capacitances, it is possible to shift f_{p1} down to a very low frequency, f_{p1}', making it the dominant pole of the precision path. At the same time, f_{p2} is pushed to higher frequencies, f_{p2}', expanding the 20-dB/dec slope and thus the range of stable operation.

In the case of a stand-alone amplifier, f_{p2} is usually located beyond the unity-gain frequency, allowing a three-stage NMC structure to achieve high bandwidth beyond 10 MHz while maintaining phase margins of up to 70°.

In the OPA333 design, however, the NMC amplifier operates in parallel with the wideband stages, g_{m4} and g_{m3}. Because this wideband forward path is responsible for providing the necessary bandwidth and phase margin of the overall amplifier, the stability requirements of the NMC amplifier are relaxed, allowing its second pole, f_{p2}, to occur before the unity-gain crossover.

Where do we apply the actual offset cancellation?

To answer this question we can, for convenience, replace the g_m stages with actual op amps, where the precision path comprising A_1 to A_3 is in parallel with the wideband path comprising A_4 and A_3 (Figure 9). For further simplification, the switching network and the notch filter have been left out, and the amplifier circuit is shown in a feedback configuration.

Figure 7. Three-stage NMC cascade amplifier

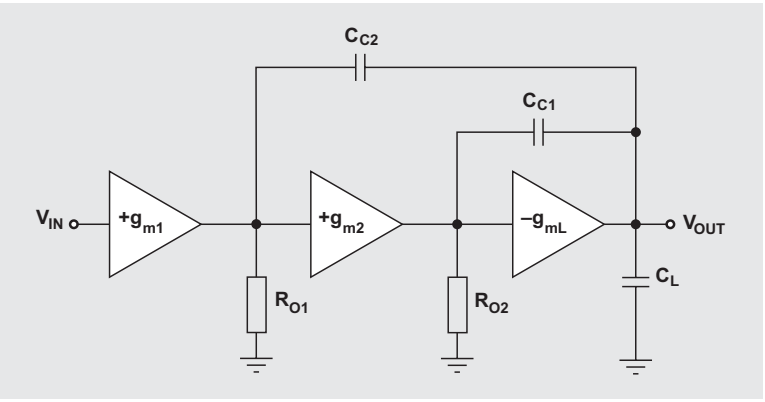


Figure 8. Pole splitting of the three-stage NMC amplifier

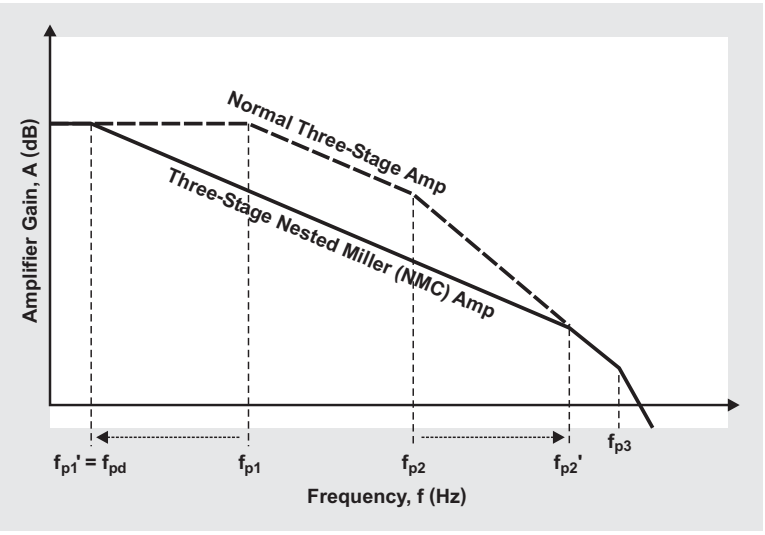
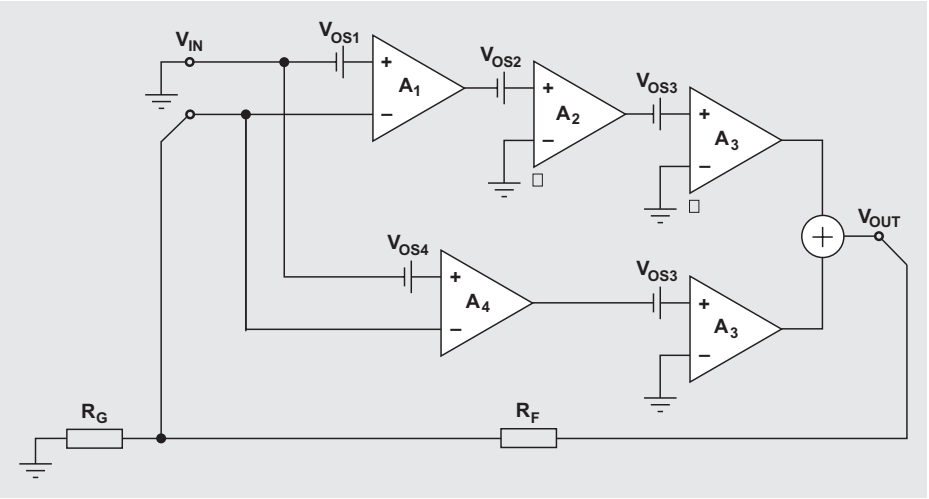


Figure 9. Deriving V_{OUT} as a function of individual offset voltages, V_{OSi}



Providing each amplifier with its individual input offset voltage and setting V_{IN} to zero yields an output of

$$V_{OUT} = A_3\left\{V_{OS3} + A_2\left[V_{OS2} + A_1\left(V_{OS1} - V_{OUT}\,\beta\right)\right]\right\} + A_3\left[V_{OS3} + A_4\left(V_{OS4} - V_{OUT}\,\beta\right)\right],$$

where

$$\beta = \frac{R_F}{R_F + R_G}.$$

Separating the V_{OUT} terms and solving for V_{OUT} gives

$$V_{OUT} = \frac{1}{\beta}\left(\frac{2V_{OS3} + V_{OS2}A_2 + V_{OS4}A_4 + V_{OS1}A_1A_2}{A_1A_2 + A_4}\right).$$

Assuming that the DC gains of A_4 and A_1 are matched,

$$V_{OUT} = \frac{1}{\beta}\left(\frac{2V_{OS3}}{A_1A_2} + \frac{V_{OS2}}{A_1} + \frac{V_{OS4}}{A_2} + V_{OS1}\right).$$

We see that, except for V_{OS1}, all offsets are strongly suppressed by the open-loop gains of at least one, if not two, preceding amplifiers. The nonattenuated V_{OS1}, however, requires active cancellation through either chopping or auto-zeroing.

Auto-zeroing versus chopping

Figures 10 and 11 show the simplified principles of both offset cancellation methods. Auto-zeroing consists of two phases, a nulling phase with switches in position 1 and an amplification phase with switches in position 2. In the nulling phase, the amplifier measures its own offset and stores it on capacitor C_1. In the amplification phase, the amplifier measures the input voltage plus the offset and subtracts the previously stored offset from the contaminated input. The resulting, offset-free output signal is stored on C_2 and operates as correcting voltage for the main amplifier.

The function of sampling and holding the offset voltage makes the AZA a data-sampling system prone to aliasing and folding effects. For DC and low frequencies, the noise properties in the time domain change slowly, and the subtraction of two consecutive noise samples results in a true cancellation. At higher frequencies this correlation diminishes, and subtraction errors translate into wideband foldover components in the baseband, where they make up the lion's share of baseband noise.

Figure 12 shows that the AZA removes offset and 1/f noise, but at the cost of a significantly raised noise floor in the baseband.

Because the noise power density of an amplifier's input stage is inversely proportional to its transconductance

Figure 10. Auto-zero principle

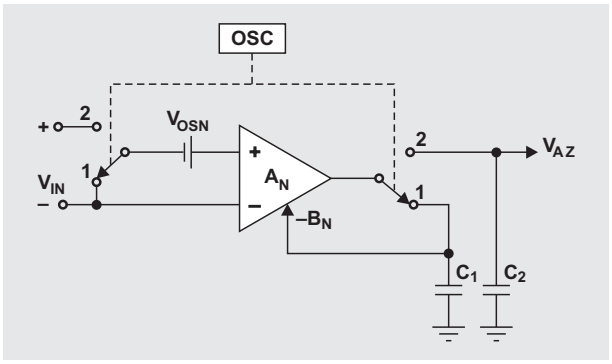


Figure 11. Chopper principle

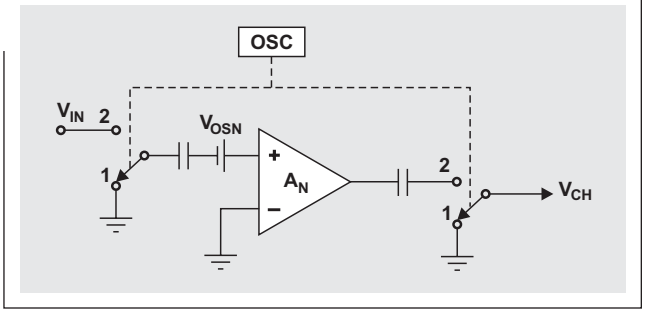


Figure 12. Auto-zeroing and chopping effects on baseband noise

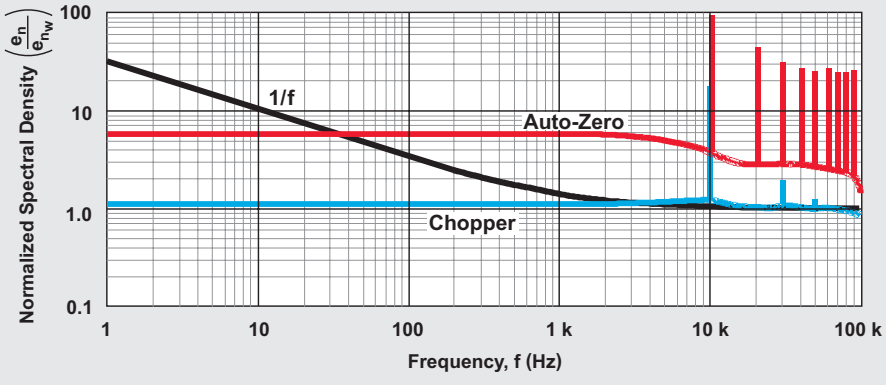
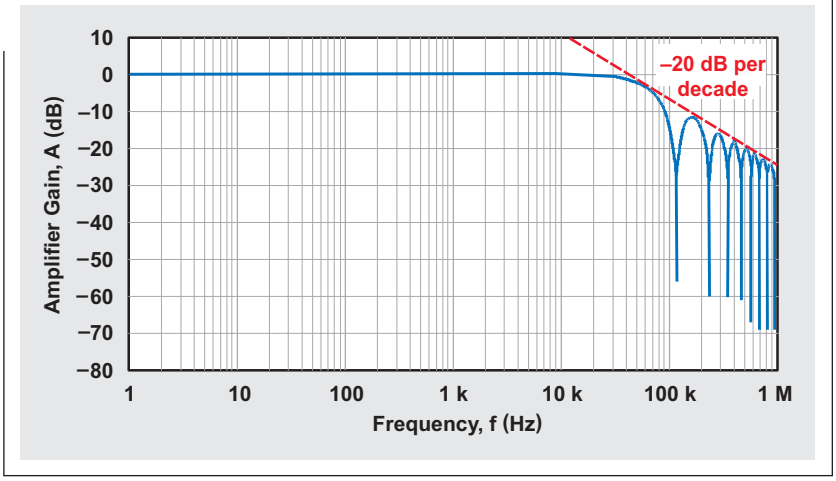


Figure 13. Filter transfer function



($e_n^2 = 2/3 \times 4KT/g_m$), and g_m is proportional to the stage quiescent current ($g_m \approx I_Q$), the power density is inversely proportional to the quiescent current ($e_n^2 \approx 1/I_Q$). Therefore, to reduce the baseband noise of an AZA to the desired level, the initial input noise must be lowered through a significant increase in quiescent current, which counteracts the intrinsic requirements of a micropower amplifier.

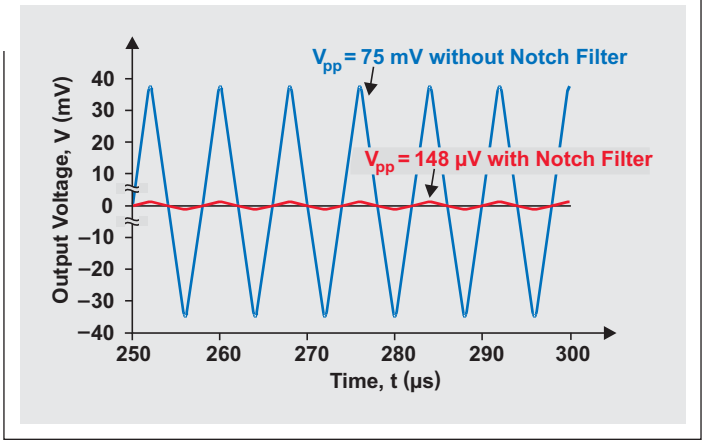
In strong contrast to the AZA, the chopper amplifier does not introduce aliasing fold-over components. As shown in Figure 11, a chopper simply modulates its offset and low-frequency noise to higher frequencies. Here the noise is neither sampled nor held, just periodically inverted without changing the general properties of the noise in the time domain. Although the power density of the chopper output noise results from a summation in the chopper modulation, as is the case for the sample-and-hold process in the AZA, the replicas (odd harmonics only) vary rapidly via a $1/n^2$ function, making their contribution to the baseband negligible.

As shown in Figure 12, for chopper frequencies larger than the noise-corner frequencies, the baseband white noise in the output is only slightly larger than the initial white-noise floor, which eliminates increases in quiescent current and makes the chopper amplifier suitable for micropower applications.

Output noise filter

While the chopper does not introduce wideband folding components into the baseband, the process of chopping does modulate the offset, or DC noise, into the higher frequency range where no noise existed before, thus creating large output ripples. The OPA333 therefore possesses a switched-capacitor (SC), low-pass notch filter in the offset cancellation path with filter notches at the chopper frequency and its harmonics. The filter's transfer function, shown in Figure 13, reduces the output ripple by a factor of more than 500. Figure 14 shows the difference in output ripple with and without the notch filter.

Figure 14. Output ripple with and without filter



The final amplifier system

Figure 15 shows the actual implementation of the chopper-stabilized amplifier, revealing a differential signal-path structure for g_{m1} and the SC notch filter. Note that, for signal symmetry, the implementation of a third capacitor, C_3, is required.

During phases 1 and 2, the input signal is modulated. During phases 3 and 4, the capacitors C_5 and C_6 work in tandem. While C_5 is charged with g_{m1}'s output current, the charge of C_6 is transferred to the integrator, g_{m2}, and vice versa.

Note that the input signal is modulated twice, once by the input switches of g_{m1} and a second time by the output switches. Relative to V_{IN}, the polarity or direction of g_{m1}'s output current remains the same during phases 1 and 2. However, the offset voltage, or offset current, is modulated only once by the output switches. Its polarity changes from phase 1 to phase 2.

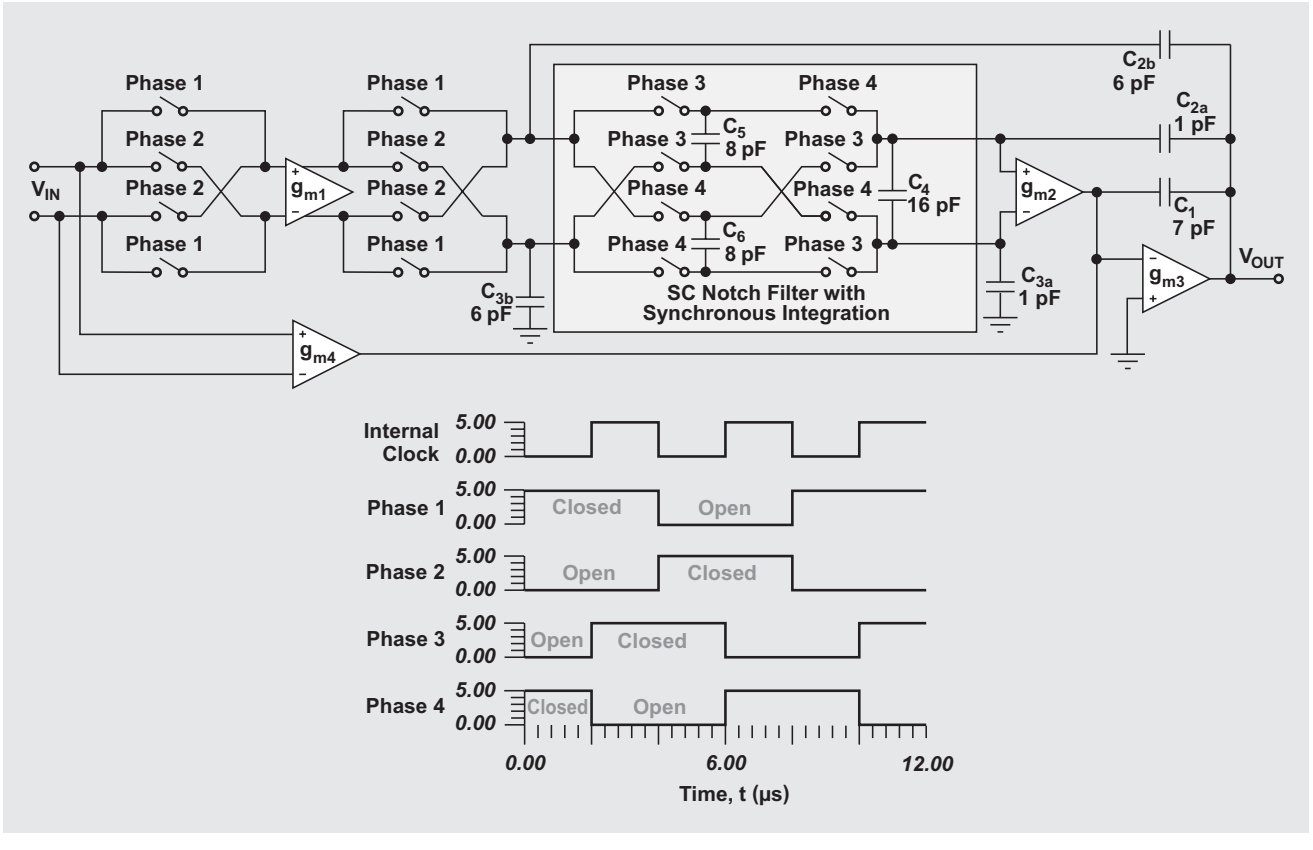
During the first half of phase 3 (that is, $t_{CK}/2$ of the clock period), the phase 1 switches are active and C_5 is charged with g_{m1}'s output current, $I_{SIG} + I_{OS}$. During the second half of phase 3, the phase 2 switches are active, the direction of the offset current changes, and C_5 is charged with $I_{SIG} - I_{OS}$.

The capacitor charge is given by $Q = I_C \times t$, with $t = t_{CK}/2$, $I_{C1} = I_{SIG} + I_{OS}$, and $I_{C2} = I_{SIG} - I_{OS}$. Thus, after phase 3 is completed, C_5 has the charge of $Q_{C5} = (I_{SIG} + I_{OS}) \times t_{CK}/2 + (I_{SIG} - I_{OS}) \times t_{CK}/2 = I_{SIG} \times t_{CK}$. The offset-free charge is then transferred to the next stage during phase 4, where the same procedure is applied to C_6.

While the large attenuation of the notch filter removes the output ripple, it may also filter the signal to some degree. A signal delay is created by the integrate-and-transfer action, which affects the circuit differently depending on how the compensation capacitors are connected.

Notice that C_2 and C_3 have been split into "a" and "b" portions (Figure 15). The "b" portion returns most of the compensation to the filter input, C_{2b} = 6 pF, maintaining good continuous-time characteristics for the signal path. The smaller "a" portion, C_{2a} = 1 pF, connects to the filter output, providing sufficient local-loop stability. The complex compensation scheme is responsible for a slight rise in the

Figure 15. Internal block diagram and timing sequence



noise floor beyond 20 kHz, which is visible in Figure 16.

Summary

This article elaborates on the technical implementations of the OPA333, the industry's superior, zero-drift micropower amplifier. Chopper stabilization ensures low baseband noise at very low supply currents. An integrated, patent-pending notch filter removes the output ripple created by the chopper modulation of the input offset.

Because an amplifier's noise power density is inversely proportional to its quiescent current, the product ($e_n^2 \times I_Q$) represents a figure of merit, revealing how much additional tail current was necessary to reduce the remaining baseband noise to the desired level after the process of offset cancellation. A more familiar figure is the ratio of gain bandwidth to quiescent current, GBW/I_Q, disclosing how much bandwidth per microampere was achieved. In both figures of merit, the OPA333 demonstrates far superior performance versus even its closest competitor (see Table 1).

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/OPA333

Figure 16. DC to 20-kHz and 200-kHz noise spectra

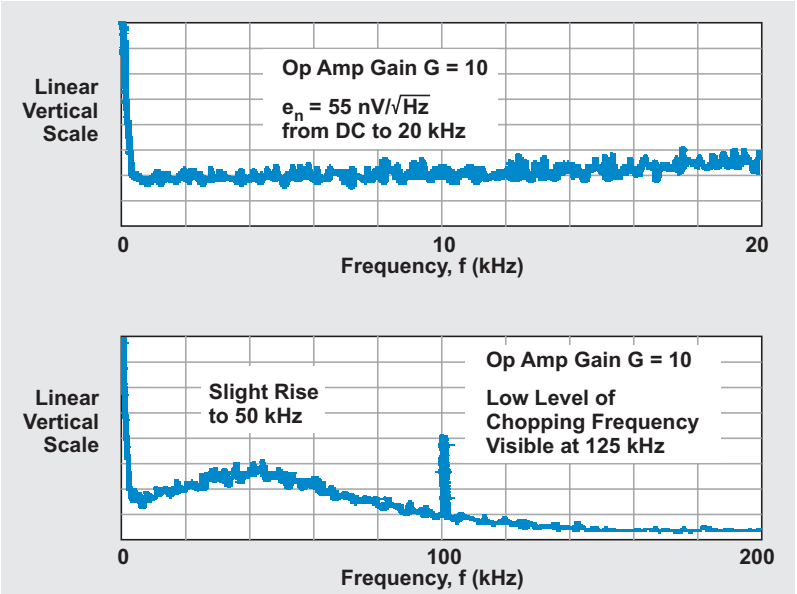


Table 1. Comparison of the OPA333 versus previous zero-drift amplifiers

	TI	COMPETITOR				
DEVICE	OPA333	(1) AD8628	(2) ICL7650	(3) LTC2054	(4) OPA335	(5) AD8551
Year	2006	2005	2005	2004	2002	2002
f_{CH} (kHz)	125	15	—	—	—	—
f_{AZ} (kHz)	—	15	0.25	1	10	4
V_{OS} (µV)	2	1	1	3	1	1
I_B (pA)	70	30	5	1	70	10
GBW (kHz)	350	2500	2000	500	2000	1500
e_n (nV/√Hz)	55	22	25	85	55	42
I_Q (µA)	15	1100	2000	150	285	975
$e_n^2 \times I_Q$ (nV² × µA)*	45	532	1250	1084	862	1720
GBW/I_Q (kHz/µA)*	23	2	1	3	7	2

*Figure of merit

Spreadsheet modeling tool helps analyze power- and ground-plane voltage drops to keep core voltages within tolerance

By Steve Widener
Analog Field Applications Engineer

Introduction

The trend toward smaller geometries in processor cores drives requirements for lower-voltage power supplies. For example, DSPs from Texas Instruments (TI) such as the TMS320TCI648x series require a 1-V core. As processor-core voltages drop, clock frequencies are typically increased to match the thermal capabilities of the packaging and of the overall cooling systems. That means higher currents in the power structures of printed circuit boards (PCBs). It is not uncommon to see 50- to 100-A current requirements for a 1-V rail when multiple processors are distributed on a single PCB. This article addresses the impact of these higher currents on the power- and ground-plane design and on the core-voltage-tolerance budget and describes a spreadsheet model that may be used to calculate voltage gradients.

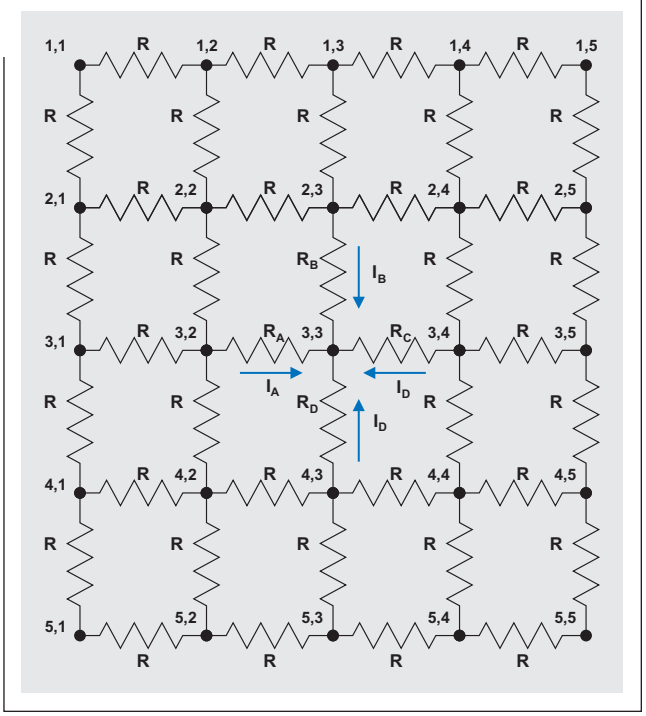
Requirements for processor-core voltage

The typical voltage-tolerance budget for the processor core is 3% for a 1-V rail, which equates to 30 mV for the total static and dynamic response of the power supply. TI's new power devices such as the PTH TurboTrans™ series (T2) modules, and new synchronous buck controllers such as the TPS40140, have been designed with internal references that allow for 1.5% tolerance under static line, load, and temperature conditions. The current guidance allocates the remaining 1.5% tolerance for the transient response of the supply. This, in combination with the bandwidth of the switching power supply, determines the amount of capacitance required to meet the core-voltage requirements. Local bypassing counteracts the inductive nature of large ground planes. Little attention is typically paid to the DC voltage drop in the power planes. As currents continue to increase and core voltages decrease, power- and ground-plane DC voltage drops will become a more significant portion of the total tolerance budget.

Power- and ground-plane voltage-drop considerations

Power- and ground-plane copper thickness is the primary attribute that impacts the voltage drop. Another major factor is the placement of the processor loads relative to the power-supply output pins. Power converters such as the PTH series allow for remote sensing to mitigate board voltage drops, but there are few tools to aid the designer in the placement of these remote sensing lines. Most designers use an ohms-per-square figure for different copper thicknesses to calculate an equivalent resistance and to determine the required copper weight. This technique works well for simple configurations; but when multiple processors or significant plane discontinuities are present (due to vias or other features), the simple ohms-per-square method may not be adequate to model the voltage drop in the power and ground planes.

Figure 1. Resistor sheet



Commercial software

Commercial software for finite-element analysis may be used to compute the plane voltage drops for arbitrary geometries, but the software is expensive and requires a developed expertise. There is no simple tool to generate a PCB model and quickly assess the plane voltage drops.

SPICE modeling

A model of the PCB may be constructed with an equivalent sheet resistance model (see Figure 1), with sources and loads connected to the appropriate nodes. The PCB

model can then be solved with a SPICE-based simulator. The difficulty in the SPICE method is that the schematic is unwieldy and the results are difficult to visualize.

A spreadsheet-based model

This article details a method that uses Microsoft® Excel® spreadsheet software to determine plane voltage distribution on a PCB with arbitrary geometry and source/load placement. A little-used feature of Excel, circular references and iteration, is used to solve the network matrix. The method may also be used with other mathematical software. This article also develops the necessary equations and provides step-by-step instructions to calculate power/ground-plane voltage drop for arbitrary source and load conditions.

Node equations for sheet resistance

Figure 1 is a schematic model of PCB node voltages interconnected by equivalent sheet resistances, R, with nodes expressed as *row, column*. This model divides the PCB into 25 nodes. Increasing the number of squares will provide more resolution. This array is sufficient to illustrate the general node equations applicable to larger models. The voltage at any node is determined by using Kirkoff's current law, which states that the sum of all currents into a node must equal zero. One of three equations is required to determine node voltage, which depends on the node location—central, edge, or corner.

Central-node equations

For central node 3,3 in Figure 1, the current equation is

$$I_A + I_B + I_C + I_D = 0. \quad (1)$$

Using Ohm's law yields

$$\frac{V_{3,2} - V_{3,3}}{R_A} + \frac{V_{2,3} - V_{3,3}}{R_B} + \frac{V_{3,4} - V_{3,3}}{R_C} + \frac{V_{4,3} - V_{3,3}}{R_D} = 0. \quad (2)$$

Solving Equation 2 for $V_{3,3}$ yields

$$V_{3,3} = \frac{R_B R_C R_D V_{3,2} + R_A R_C R_D V_{2,3} + R_A R_B R_D V_{3,4} + R_A R_B R_C V_{4,3}}{R_B R_C R_D + R_A R_C R_D + R_A R_B R_D + R_A R_B R_C}. \quad (3)$$

Equation 3 is the general form of the equation for a central node with arbitrary sheet resistance. This equation accommodates variations in square resistance that are due to localized heating or other nonuniformities. In the case of uniform sheet resistance, Equation 3 simplifies to

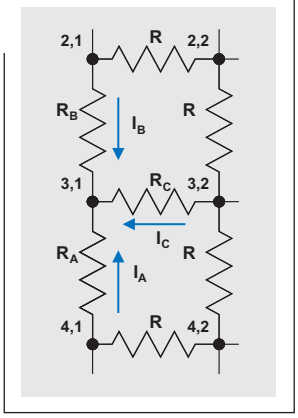
$$V_{3,3} = \frac{V_{3,2} + V_{2,3} + V_{3,4} + V_{4,3}}{4}. \quad (4)$$

Edge-node equations

For edge node 3,1, Figure 2 depicts the currents flowing from the three adjacent nodes. The current equation for an edge node is

$$I_A + I_B + I_C = 0. \quad (5)$$

Figure 2. Edge node



Using Ohm's law yields

$$\frac{V_{4,1} - V_{3,1}}{R_A} + \frac{V_{2,1} - V_{3,1}}{R_B} + \frac{V_{3,2} - V_{3,1}}{R_C} = 0. \quad (6)$$

Solving for $V_{3,1}$ yields

$$V_{3,1} = \frac{R_B R_C V_{4,1} + R_A R_C V_{2,1} + R_A R_B V_{3,2}}{R_B R_C + R_A R_C + R_A R_B}. \quad (7)$$

Equation 7 is the general form of the equation for an edge node with arbitrary sheet resistance. In the case of uniform sheet resistance, Equation 7 simplifies to

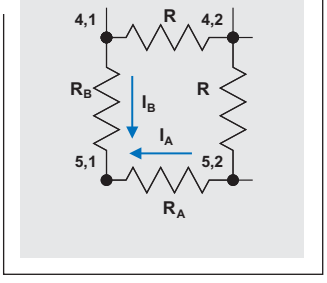
$$V_{3,1} = \frac{V_{4,1} + V_{2,1} + V_{3,2}}{3}. \quad (8)$$

Corner-node equations

For corner node 5,1, Figure 3 depicts the currents flowing from the two adjacent nodes. The current equation for a corner node is

$$I_A + I_B = 0. \quad (9)$$

Figure 3. Corner node



Using Ohm's law yields

$$\frac{V_{5,2}-V_{5,1}}{R_A}+\frac{V_{4,1}-V_{5,1}}{R_B}=0. \quad (10)$$

Solving for $V_{5,1}$ yields

$$V_{5,1}=\frac{R_B V_{5,2}+R_A V_{4,1}}{R_B+R_A}. \quad (11)$$

Equation 11 is the general form of the equation for a corner node with arbitrary sheet resistance. In the case of uniform sheet resistance, Equation 11 simplifies to

$$V_{5,1}=\frac{V_{5,2}+V_{4,1}}{2}. \quad (12)$$

Source nodes

The outputs of power supplies are modeled as fixed values (voltages) at the geometrically relevant nodes. Many power supplies utilize differential remote sensing. In the model, the fixed-voltage nodes may represent the local sense points, and the power-supply output is varied to set the desired voltage at those remote sensing points.

The remaining equations solve for node voltages where a load is present at the node.

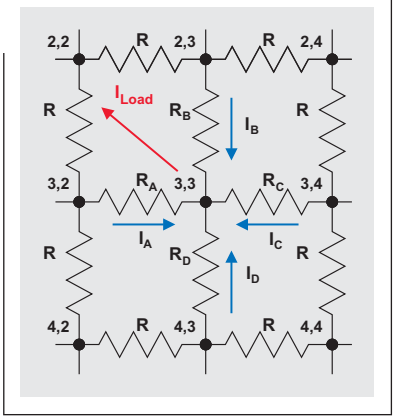
Load equations

Central-node equations

In the case of a central node with a load (Figure 4), the current equation is

$$I_A+I_B+I_C+I_D=I_{Load}. \quad (13)$$

Figure 4. Central load node



Using Ohm's law yields

$$\frac{V_{3,2}-V_{3,3}}{R_A}+\frac{V_{2,3}-V_{3,3}}{R_B}+\frac{V_{3,4}-V_{3,3}}{R_C}+\frac{V_{4,3}-V_{3,3}}{R_D}=I_{Load}. \quad (14)$$

Solving Equation 14 for $V_{3,3}$ yields

$$V_{3,3}=\frac{R_B R_C R_D V_{3,2}+R_A R_C R_D V_{2,3}+R_A R_B R_D V_{3,4}+R_A R_B R_C V_{4,3}-R_A R_B R_C R_D I_{Load}}{R_B R_C R_D+R_A R_C R_D+R_A R_B R_D+R_A R_B R_C}. \quad (15)$$

Equation 15 is the general form of the equation for a central node with arbitrary sheet resistance and a load current. In the case of uniform sheet resistance, Equation 15 simplifies to

$$V_{3,3}=\frac{V_{3,2}+V_{2,3}+V_{3,4}+V_{4,3}-RI_{Load}}{4}. \quad (16)$$

Edge-node equations

For the case where load current is sourced from an edge node (node 3,1 in Figure 2), the node voltage equation is

$$V_{3,1}=\frac{R_B R_C V_{4,1}+R_A R_C V_{2,1}+R_A R_B V_{3,2}-R_A R_B R_C I_{Load}}{R_B R_C+R_A R_C+R_A R_B}. \quad (17)$$

For uniform sheet resistance, Equation 17 simplifies to

$$V_{3,1}=\frac{V_{4,1}+V_{2,1}+V_{3,2}-RI_{Load}}{3}. \quad (18)$$

Corner-node equations

For the case where load current is sourced from a corner node (node 5,1 in Figure 3), the node voltage equation is

$$V_{5,1}=\frac{R_B V_{5,2}+R_A V_{4,1}-R_A R_B I_{Load}}{R_B+R_A}. \quad (19)$$

For uniform sheet resistance, Equation 19 simplifies to

$$V_{5,1}=\frac{V_{5,2}+V_{4,1}-RI_{Load}}{2}. \quad (20)$$

The previous equations may be used to model the power- or ground-plane voltage map of a PCB with arbitrary source, resistance, and load arrangements.

Example problem

PCB voltage-drop modeling presents two challenges. The first is to build the representative model with a number of voltage sources, path resistances, and loads distributed across the PCB; the second is to solve the simultaneous equations. Excel spreadsheet software provides a convenient means to quickly build a model and solve the nodal equations. Following is a simple example that illustrates this. A PCB power plane with uniform sheet resistance is modeled and the voltage at every node is calculated for a given set of load conditions.

For this example, a 10 × 15-cm copper board with a 1-V/1-oz power plane and a 1-oz ground return plane is assumed. A single power supply with 1 output pin provides the voltage source, and distributed across the PCB are 10 loads drawing 5 A each. The goal is to determine the steady-state voltage at each load with a 65°C board temperature.

Worksheet model construction step-by-step

To model the PCB, a worksheet is used where a range of cells is assigned to represent the node voltages on the PCB. Each cell corresponds to a square of copper on the PCB. The size of each square is chosen for a desired geometric resolution. For instance, if 1-mm geometries (such as slots or via holes) are desired, then 100 × 150 squares (cells) would be required to model a 10 × 15-cm PCB. For this simple example, 5-mm squares are selected to model a 10 × 7.5-cm PCB, so an array of 20 × 15 cells is used in the spreadsheet (see Figure 5). The 300 cells are highlighted green to identify the PCB outline.

Circular references

To build this model, a few non-intuitive steps must be followed, because circular references are required to solve the nodal equations. "Circular reference" refers to the condition where the value of a cell is a function of its own value in some way. This situation may be resolved by allowing Excel to iterate the value in the cell (by increasing or decreasing the value) until some tolerance level is met and the interrelated equations converge. There are instances when Excel will not be able to resolve circular references—particularly evident when the model is being built or is undergoing major changes. For this reason, manual calculation is used in the spreadsheet model.

Initialization

To build the model, it is first assumed that the voltage distribution is ideal; that is, there is 1 V in every cell. A "1" is entered in each cell to start (see Figure 6). Note that it is convenient to label the boundaries of the PCB model with an index grid to aid in placing the sources and loads.

Figure 5. Model of 10 x 7.5-cm PCB with 5-mm squares

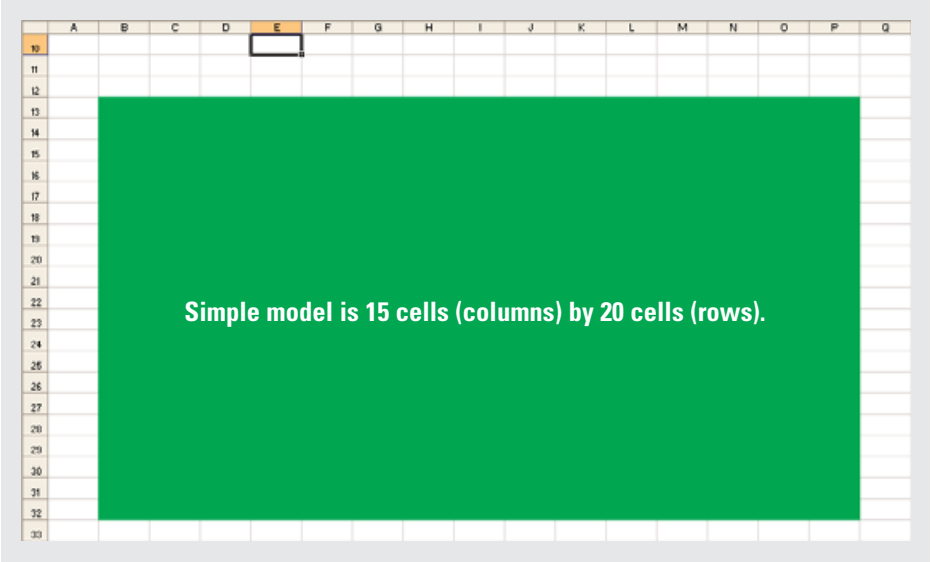


Figure 6. Model of ideal voltage distribution

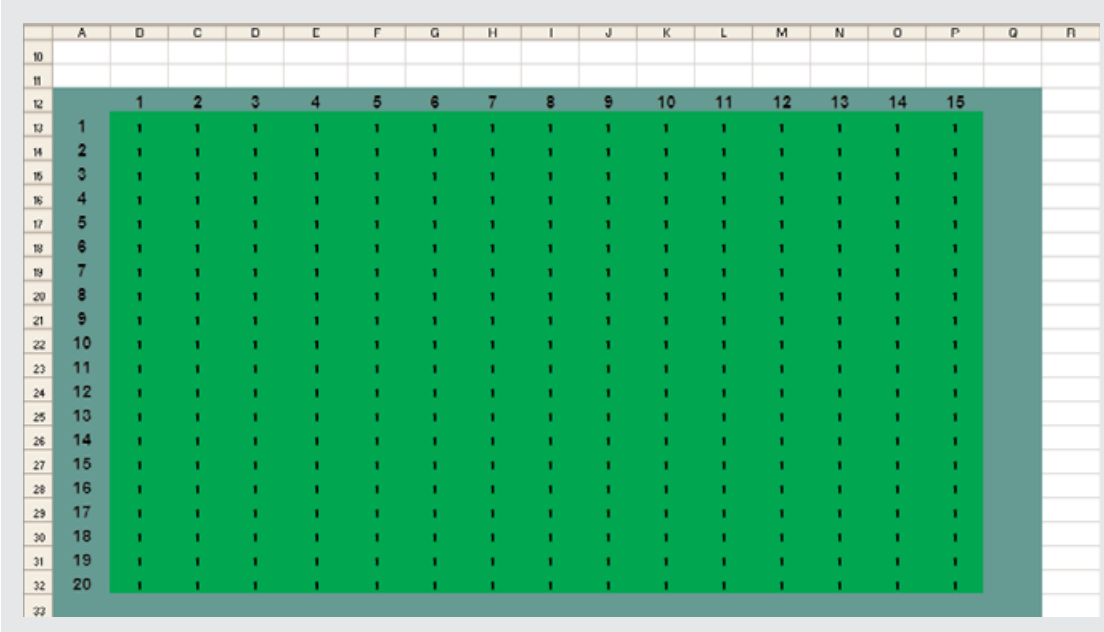
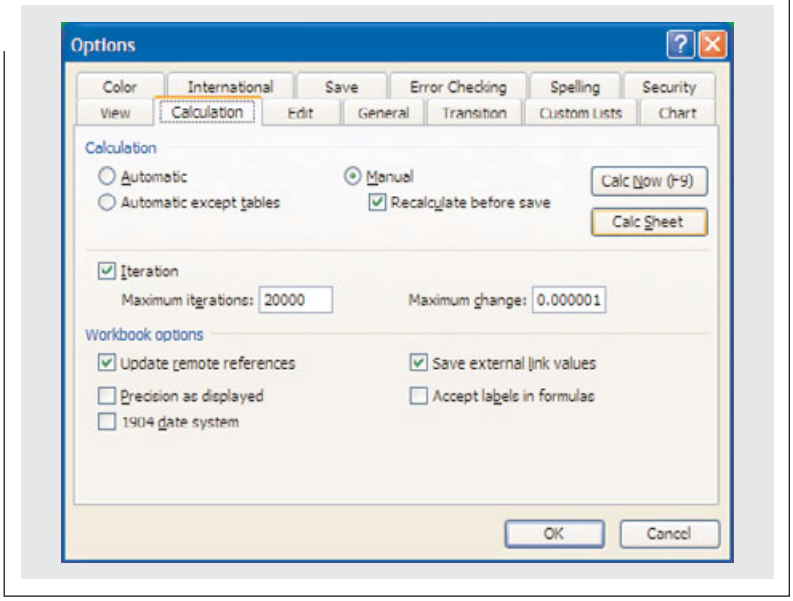


Figure 7. PCB model settings entered in *Calculation* menu



The next step is to disable automatic calculation by checking the *Manual* "radio button" in the *Tools* > *Options* > *Calculation* menu (Figure 7). When a change is made, the F9 key recalculates the worksheet. While this menu is open, the Iteration box should be checked, and the parameters *Maximum Iterations* and *Maximum Change* should be set to 20000 and 0.000001, respectively. This sets the parameters for the solution engine so that iterations occur up to 20,000 times or until the solution converges to within 1 µV. These preliminary settings are required to enable iterative calculations and to avoid convergence errors while the PCB model is being built and modified.

A simplifying assumption

For this example, the sheet resistance is assumed to be uniform in the power and ground planes so that a simplifying assumption can be made. The ground- and power-plane resistances are combined, and the "return" path is assumed to have zero resistance. That assumption makes the voltage at each cell representative of the differential voltage (plane to ground) at every location on the PCB. The resistance of the power plane is simply doubled to account for the return path.

Copper-sheet resistance

The sheet resistance of copper is given as

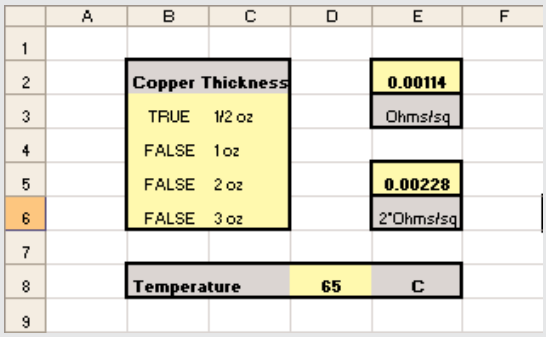
$$\rho = \frac{\rho_{20}\left[1+\alpha\left(T-20\right)\right]}{h}, \qquad (21)$$

where ρ is the sheet resistance of copper in ohms per square (Ω/); ρ_{20} is the resistivity of copper at 20°C equal to 17.241 mΩ/µm†; α is the temperature coefficient of resistance for copper equal to 0.393%/°C†; T is the PCB temperature in degrees Celsius at the square of interest; and h is the thickness of the copper plane in micrometers (1 oz ~ 35.6 µm ±10%). Equation 21 is implemented with the following Excel equation inserted into cell E2 (see Figure 8):

=(0.017241*(1+0.00393*(D8-20)))
/(17.8*(IF(B3,1,IF(B4,2,IF(B5,4,IF(B6,6,0))))))

The temperature is located in cell D8, and one of the copper thicknesses in cells B3 through B6 (½, 1, 2, or 3 oz) is exclusively selected with a "TRUE." The resulting sheet resistance value in ohms per square is in cell E2. The value for twice this resistance (accounting for the combined power- and ground-plane resistances), located in cell E5, is used for the simplifying assumption.

Figure 8. Implementation of Equation 21 in Excel



†*CRC Handbook of Chemistry and Physics*, 58th edition (CRC Press, Inc., 1977), Section E-84.

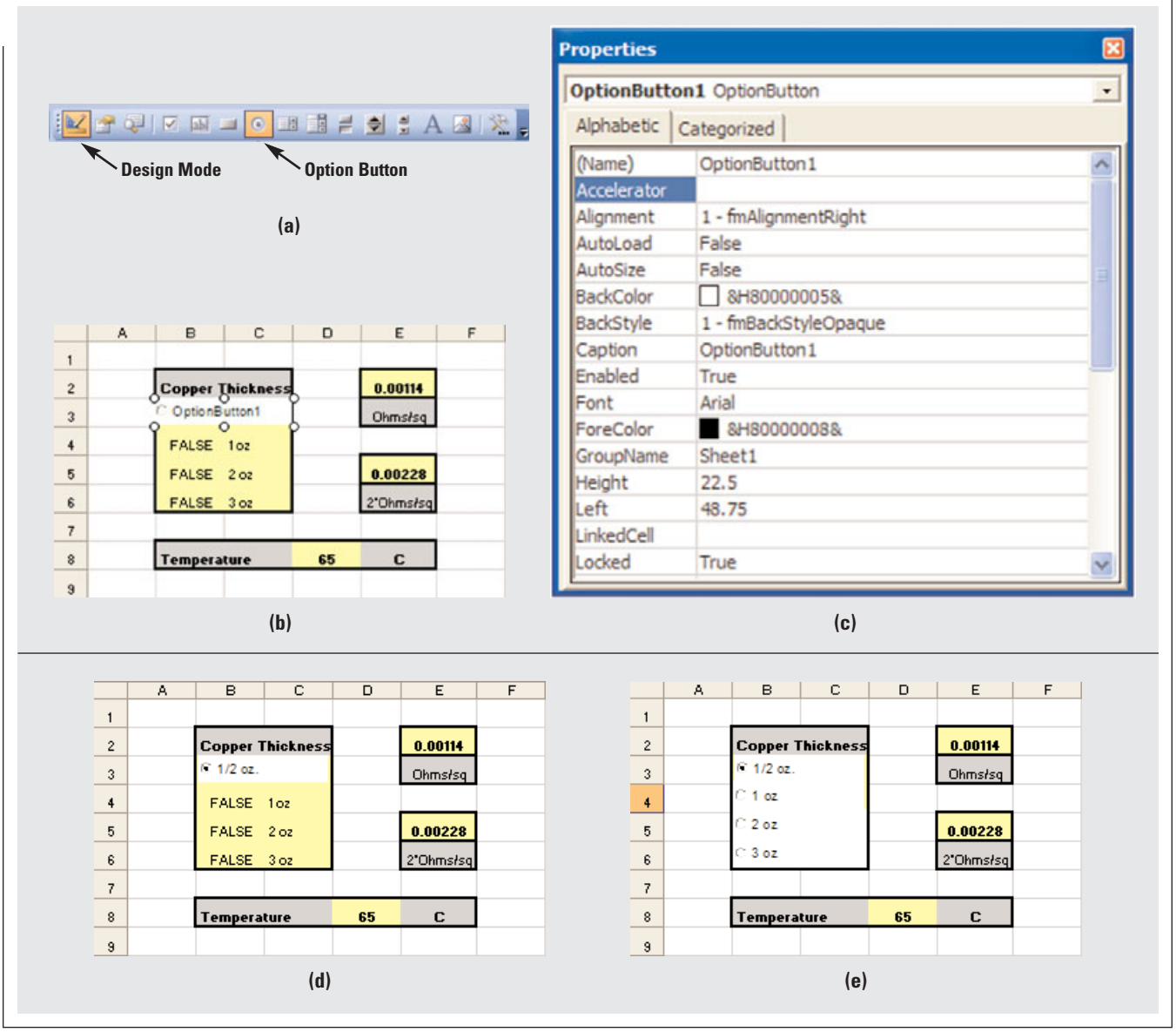
Adding radio buttons to select copper thickness

The copper thicknesses of ½, 1, 2, and 3 oz are arranged as shown in Figure 8 to allow for the convenient use of radio buttons to select them. To place a radio button, turn on the *Control Toolbox* toolbar (*View* > *Toolbars* > *Control Toolbox*) and select *Design Mode* and *Option Button* (Figure 9a). In this mode, use the cursor to draw a box over cells B3 and C3 as shown in Figure 9b. Right-clicking in the new *OptionButton1* area and selecting *Properties* makes the dialog box in Figure 9c appear. Change the *Caption* field from "OptionButton1" to "1/2 oz" and enter "B3" into the *LinkedCell* field, then close the dialog box. The radio button now appears as shown in Figure 9d. With these settings, cell B3 will be true when this radio button is selected.

Repeat the process for 1, 2, and 3 oz, linking their radio buttons to cells B4, B5, and B6, respectively. The results appear as shown in Figure 9e.

Because the *GroupName* field (*Sheet1*) is common to all the radio buttons, only one thickness may be selected at a time. The radio buttons will not work until the design mode is exited, but there is one more task to complete before exiting.

Figure 9. Adding radio buttons to select copper thickness



Adding a command button for recalculation

While design mode is still active, it is advantageous to create a reminder button to initiate recalculation. Select the *Command Button* on the *Control Toolbox* toolbar (see Figure 10a), then click on some empty cells and drag to create a *CommandButton1* box as shown in Figure 10b. Right-clicking on the *CommandButton1* box and selecting *Properties* makes the dialog box in Figure 10c appear. Change the *Caption* field from "CommandButton1" to "Recalculate" and close the dialog box. Now a *Recalculate* button is displayed as shown in Figure 10d. Exit design mode the same way you entered, by clicking the *Design Mode* button on the *Control Toolbox* toolbar (Figure 10e).

To cause the *Recalculate* button to force a recalculation, a simple macro must be assigned to the button. Select *Tools* > *Macro* > *Visual Basic Editor* to open Visual Basic, then select *View* > *Code* to open a window similar to the one shown in Figure 10f. Type in the code shown in Figure 10g and close the window. Now, as the copper thickness and temperature are changed, clicking the *Recalculate* button will update the ohms-per-square values appropriately (see Figure 10h).

Figure 10. Adding a command button for recalculation

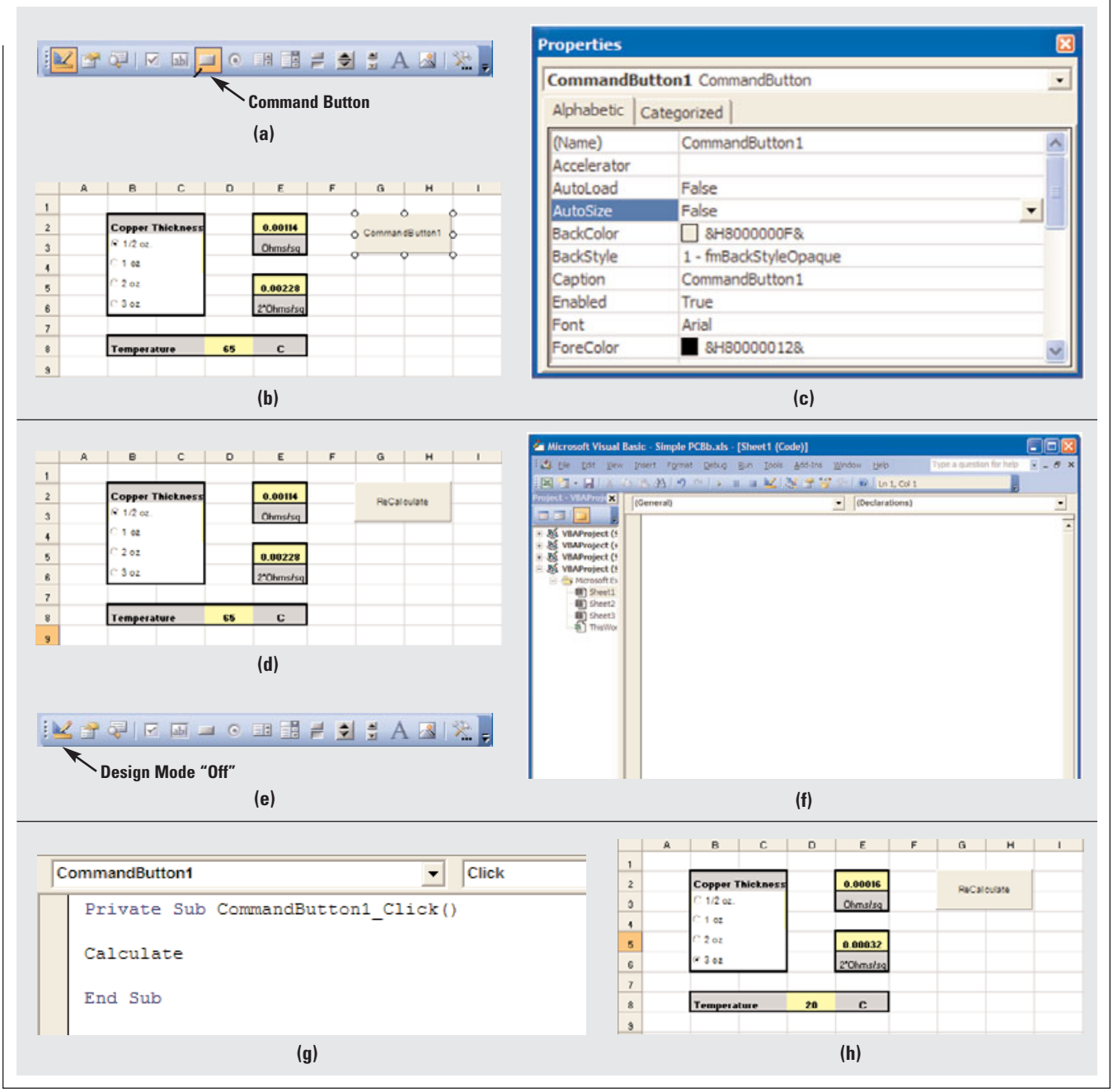
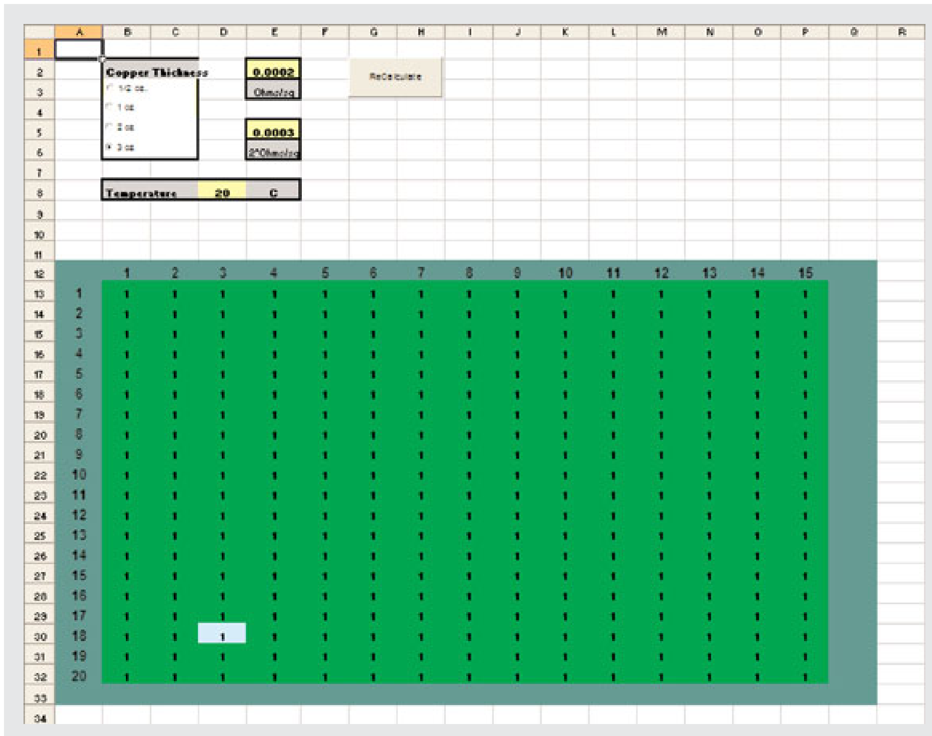


Figure 11. Model with 1-V source entered in cell D30



Building the node-voltage model

To build the node-voltage model, an equation for each node must be entered into the appropriate cell in Excel. Note that for each node, "adjoining cells" refers to those found either above, below, left, or right—not at a diagonal.

Corner nodes: Enter the Excel expression for Equation 12, "=(Sum of the 2 adjoining cells)/2".

Example: For cell B13, enter "=(B14+C13)/2".

Edge nodes: Enter the Excel expression for Equation 8, "=(Sum of the 3 adjoining cells)/3".

Example: For cell F32, enter "=(F31+E32+G32)/3".

Central nodes: Enter the Excel expression for Equation 4, "=(Sum of the 4 adjoining cells)/4".

Example: For cell K23, enter "=(K24+J23+K22+L23)/4".

Fill in all cells with the equations as described and click the *Recalculate* macro button. All voltages remain at 1 V, as there are no sources or loads. It is advisable to save the spreadsheet at this point and to create a backup. New form factors may easily be constructed at this stage by recopying the equations in the desired resolution and form factor.

Adding sources to the model

Sources represent the output of the power supply at the point of regulation. Positioning a source is easily done by placing a fixed numeric value in the cell that corresponds (geometrically) to the location of the actual power-supply output on the PCB. It is convenient to give the cell a contrasting color for ease of identification. Figure 11 shows a 1-V source that was placed in cell D30 by simply entering "1" in place of the equation.

Adding loads to the model

Loads represent current sinks geometrically located on the PCB. Enter a location for a load current in cell H5 and enter "10" in that cell (see Figure 12). Then type the Excel expression for Equation 16 into cell M17 as "=(M18+L17+M16+N17-E5*H5)/4".

"E5" and "H5" are absolute (versus relative) references to the copper resistance and load current, respectively, and will not change as this equation is copied into other cells. The remaining factors should change as the load equation is copied into other cells.

Figure 12. Model with load current of 10 added in cell H5

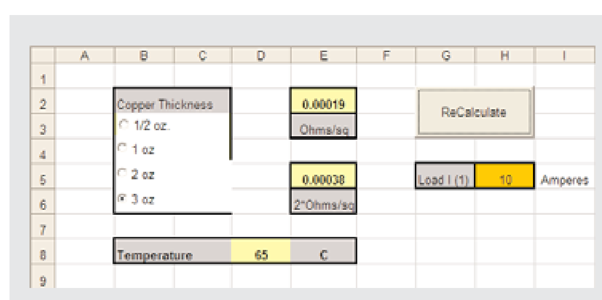


Figure 13. Voltage distribution calculations using 3-oz copper at 25°C with 1 source and 1 load

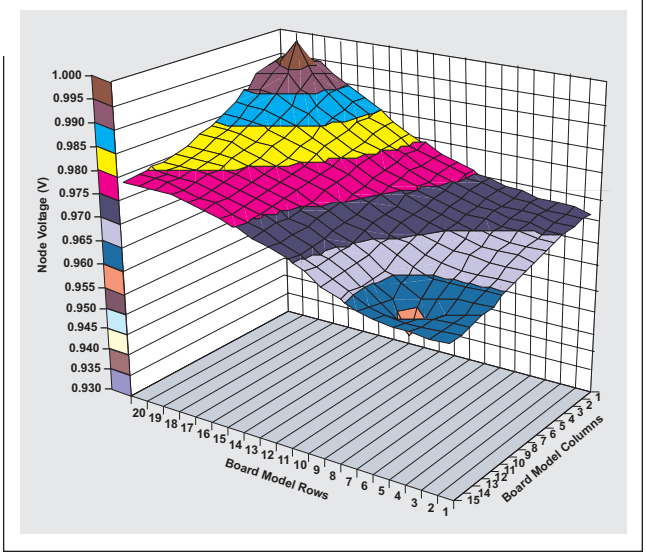
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
1																		
2		Copper Thickness			0.0002		ReCalculate											
3		○ 1/2 oz.			Ohms/sq													
4		○ 1 oz																
5		○ 2 oz			0.0003		Load I (1)	10	Amperes									
6		● 3 oz			2*Ohms/sq													
7																		
8		Temperature		25	C													
9																		
10																		
11																		
12		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
13	1	0.9352	0.9352	0.9352	0.93509	0.935	0.9349	0.9348	0.9346	0.9345	0.9343	0.9341	0.934	0.934	0.9339	0.9339		
14	2	0.9353	0.9352	0.9352	0.93512	0.935	0.9349	0.9348	0.9346	0.9345	0.9343	0.9341	0.934	0.9339	0.9339	0.9339		
15	3	0.9353	0.9353	0.9352	0.93517	0.9351	0.935	0.9348	0.9347	0.9345	0.9343	0.934	0.9339	0.9339	0.9339	0.9339		
16	4	0.9354	0.9354	0.9353	0.93524	0.9351	0.935	0.9349	0.9347	0.9345	0.9342	0.9339	0.9336	0.9337	0.9339	0.9339		
17	5	0.9355	0.9355	0.9354	0.93534	0.9352	0.9351	0.935	0.9348	0.9346	0.9343	0.9338	0.9329	0.9336	0.9339	0.934		
18	6	0.9356	0.9356	0.9355	0.93546	0.9354	0.9353	0.9351	0.9349	0.9347	0.9345	0.9342	0.9339	0.934	0.9341	0.9342		
19	7	0.9358	0.9357	0.9357	0.93561	0.9355	0.9354	0.9353	0.9351	0.9349	0.9347	0.9345	0.9344	0.9344	0.9344	0.9344		
20	8	0.9359	0.9359	0.9359	0.93579	0.9357	0.9356	0.9355	0.9353	0.9352	0.935	0.9349	0.9347	0.9347	0.9347	0.9347		
21	9	0.9361	0.9361	0.9361	0.93598	0.9359	0.9358	0.9357	0.9355	0.9354	0.9353	0.9351	0.935	0.935	0.935	0.9349		
22	10	0.9363	0.9363	0.9363	0.9362	0.9361	0.936	0.9359	0.9358	0.9356	0.9355	0.9354	0.9353	0.9353	0.9352	0.9352		
23	11	0.9366	0.9366	0.9365	0.93644	0.9363	0.9362	0.9361	0.936	0.9359	0.9357	0.9356	0.9356	0.9355	0.9355	0.9354		
24	12	0.9369	0.9368	0.9368	0.9367	0.9366	0.9365	0.9363	0.9362	0.9361	0.936	0.9359	0.9358	0.9357	0.9357	0.9357		
25	13	0.9372	0.9371	0.9371	0.93693	0.9369	0.9367	0.9366	0.9364	0.9363	0.9362	0.9361	0.936	0.9359	0.9359	0.9359		
26	14	0.9375	0.9375	0.9374	0.9373	0.9371	0.937	0.9368	0.9367	0.9365	0.9364	0.9363	0.9362	0.9361	0.9361	0.936		
27	15	0.9379	0.9379	0.9378	0.93764	0.9374	0.9372	0.937	0.9369	0.9367	0.9366	0.9364	0.9363	0.9363	0.9362	0.9362		
28	16	0.9383	0.9383	0.9382	0.93803	0.9378	0.9375	0.9373	0.937	0.9369	0.9367	0.9366	0.9365	0.9364	0.9363	0.9363		
29	17	0.9387	0.9388	0.9389	0.93847	0.9381	0.9377	0.9374	0.9372	0.937	0.9368	0.9367	0.9366	0.9365	0.9365	0.9364		
30	18	0.939	0.9392	1	0.9389	0.9383	0.9379	0.9376	0.9373	0.9371	0.9369	0.9368	0.9367	0.9366	0.9365	0.9365		
31	19	0.9391	0.9392	0.9393	0.93882	0.9384	0.938	0.9377	0.9374	0.9372	0.937	0.9369	0.9367	0.9367	0.9366	0.9366		
32	20	0.9391	0.9391	0.939	0.93875	0.9384	0.938	0.9377	0.9375	0.9372	0.937	0.9369	0.9368	0.9367	0.9366	0.9366		
33																		
34																		

Putting it all together

For the load equation just described, the sheet resistance (actually two times the sheet resistance to account for the return path) is in cell E5, and the load current is in cell H5. Set the temperature to 25°C and select 3-oz copper, then click the *Recalculate* button. When the iterations are complete, the screen appears as shown in Figure 13. Each cell now contains the calculated voltage on the PCB (differential voltage to ground at the load point) for the given copper thickness, source voltage, temperature, and load current. The cells model voltages at the corresponding geometric locations on the PCB.

For a visual representation of voltage distribution using lightweight copper, change the copper thickness to ½ oz and the temperature to 65°C and click *Recalculate*. Selecting the voltage results and applying a surface chart creates the voltage map shown in Figure 14.

Figure 14. Voltage map of recalculated data with ½-oz copper at 65°C



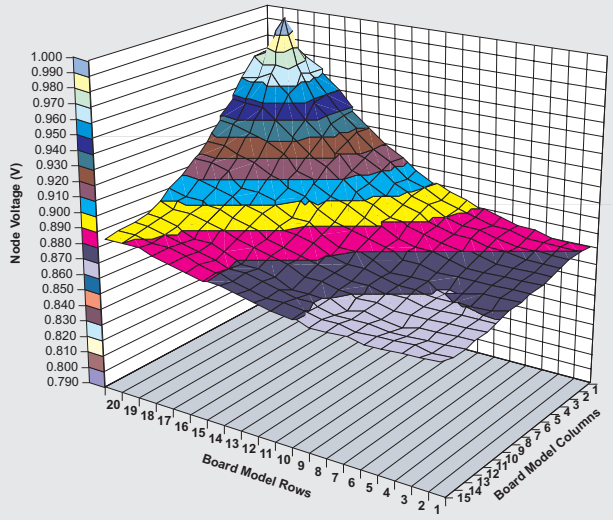
To see an example with multiple loads, reset the copper thickness to 1 oz, the load current to 5 A, and the ambient temperature to 65°C. Then copy the load equation in cell M17 into 9 additional locations on the PCB and click *Recalculate*. The results are shown in Figure 15a. Figure 15b shows the new voltage gradient.

The 50-A total load with 1-oz copper planes causes a worst-case droop of 136 mV—much more than the typical requirement of ±30 mV—and that doesn't include transient response. Obviously, thicker copper planes are required, so the copper thickness should be adjusted back to 3 oz (Figure 15c). In this case, the maximum droop is 23.4 mV—a much better situation.

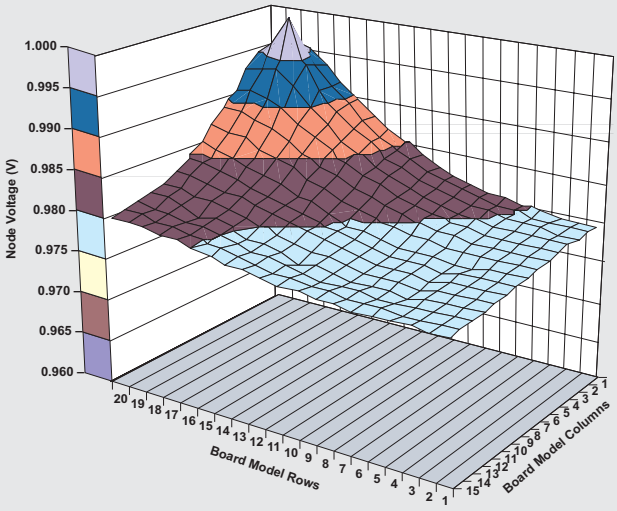
Figure 15. Calculated voltage distribution with 1 source and 10 loads

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0.8803	0.88	0.8792	0.87821	0.8769	0.8754	0.8739	0.8724	0.871	0.8699	0.8689	0.8682	0.8677	0.8675	0.8674
2	0.8807	0.8803	0.8796	0.87847	0.8771	0.8755	0.8738	0.8722	0.8708	0.8697	0.8687	0.8679	0.8675	0.8673	0.8673
3	0.8814	0.881	0.8802	0.87901	0.8775	0.8757	0.8737	0.8718	0.8705	0.8693	0.8682	0.8673	0.8671	0.8671	0.8671
4	0.8826	0.8821	0.8812	0.87989	0.8781	0.876	0.8735	0.8709	0.8699	0.8688	0.8674	0.8661	0.8664	0.8668	0.8669
5	0.8842	0.8837	0.8827	0.88119	0.8792	0.8767	0.8734	0.8685	0.8693	0.8685	0.8667	0.8633	0.8657	0.8666	0.867
6	0.8863	0.8857	0.8846	0.88297	0.8808	0.8781	0.8749	0.8717	0.8705	0.8692	0.8676	0.866	0.8665	0.8671	0.8674
7	0.889	0.8883	0.8871	0.88529	0.8829	0.8799	0.8765	0.8731	0.8716	0.8701	0.8684	0.8668	0.8672	0.8677	0.868
8	0.8922	0.8916	0.8902	0.88819	0.8855	0.8822	0.8781	0.8725	0.8727	0.8713	0.8691	0.8654	0.8677	0.8687	0.869
9	0.8962	0.8955	0.8939	0.89172	0.8888	0.8853	0.8813	0.8773	0.8753	0.8734	0.8714	0.8694	0.8697	0.8701	0.8704
10	0.9009	0.9001	0.8984	0.89594	0.8927	0.8889	0.8845	0.8802	0.8779	0.8757	0.8734	0.8713	0.8714	0.8718	0.872
11	0.9065	0.9055	0.9037	0.90088	0.8973	0.8929	0.8877	0.881	0.8803	0.8781	0.8752	0.871	0.8729	0.8736	0.8739
12	0.913	0.9119	0.9098	0.90665	0.9026	0.8978	0.8925	0.8873	0.8841	0.8813	0.8784	0.8759	0.8757	0.8758	0.8759
13	0.9206	0.9194	0.917	0.91333	0.9086	0.9031	0.8972	0.8913	0.8877	0.8845	0.8813	0.8785	0.8781	0.8781	0.8781
14	0.9293	0.9281	0.9254	0.92106	0.9154	0.9089	0.9017	0.8932	0.891	0.8876	0.8837	0.8787	0.88	0.8803	0.8804
15	0.9393	0.9383	0.9355	0.93009	0.9231	0.9154	0.9076	0.9002	0.8954	0.8912	0.8873	0.8839	0.883	0.8828	0.8827
16	0.9503	0.9501	0.9482	0.94073	0.9315	0.922	0.913	0.9047	0.8993	0.8945	0.8902	0.8866	0.8855	0.885	0.8849
17	0.9616	0.9638	0.9663	0.95321	0.94	0.9282	0.9175	0.9065	0.9023	0.8975	0.8925	0.8867	0.8873	0.8871	0.8869
18	0.9705	0.9773	1	0.96584	0.947	0.9334	0.9223	0.9128	0.9061	0.9005	0.8957	0.8917	0.89	0.8891	0.8886
19	0.9726	0.9743	0.977	0.9631	0.9488	0.9363	0.9254	0.9162	0.9089	0.9023	0.898	0.8943	0.892	0.8906	0.89
20	0.9726	0.9725	0.9701	0.96072	0.949	0.9374	0.9268	0.9178	0.9102	0.9041	0.8992	0.8955	0.893	0.8914	0.8907

(a) With 1-oz copper



(b) With 1-oz copper



(c) With 3-oz copper

The voltage-gradient information provided by the model is very helpful in determining the optimal placement of the remote sense lines relative to the power supply or power module.

Adding slots or vias

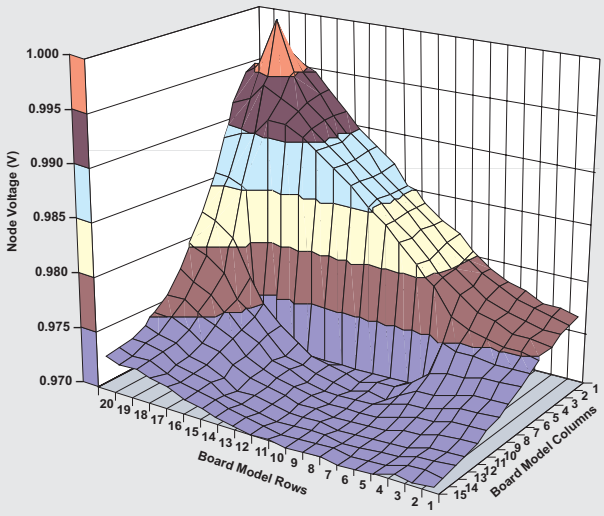
Slots or rows of vias may be modeled by inserting edge and corner nodes into the appropriate locations in the worksheet and placing a "0" in the cells that represent the slots (Figure 16a). With the slots included in the calculation, the voltage plot looks as shown in Figure 16b. The slot changes the worst-case voltage droop to 30.3 mV.

Many situations may be modeled with this simple example. Additional accuracy is expected as more cells are used to model the sheet resistance. The maximum number of columns in Excel is limited to 256, which sets the limitation for the minimum resolution (for one dimension of the PCB). Note that the three-dimensional graphing capability

Figure 16. Model with slots added

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0.3766	0.3764	0.3761	0.37557	0.375	0.3743	0.3736	0.3729	0.3723	0.3718	0.3714	0.3711	0.3709	0.3707	0.3707
2	0.3767	0.3765	0.3762	0.37569	0.375	0.3743	0.3735	0.3728	0.3722	0.3717	0.3713	0.371	0.3708	0.3707	0.3706
3	0.3771	0.3769	0.3765	0.37594	0.3752	0.3744	0.3735	0.3727	0.372	0.3715	0.3711	0.3708	0.3706	0.3705	0.3705
4	0.3776	0.3774	0.377	0.37637	0.3755	0.3744	0.3733	0.3723	0.3717	0.3712	0.3708	0.3704	0.3703	0.3703	0.3703
5	0.3783	0.3781	0.3777	0.37704	0.376	0.3745	0.373	0.3715	0.3713	0.3709	0.3704	0.3697	0.37	0.3701	0.3702
6	0.3792	0.379	0.3787	0.37806	0.377	0.3747	0.3726	0.3715	0.371	0.3706	0.3702	0.3693	0.3699	0.37	0.3701
7	0.3803	0.3802	0.3799	0.37953	0.3791		0.3713	0.3708	0.3706	0.3703	0.37	0.3697	0.3698	0.3699	0.37
8	0.3815	0.3814	0.3812	0.38104	0.3809		0.3705	0.3699	0.3701	0.3701	0.3698	0.3692	0.3697	0.3699	0.3699
9	0.3828	0.3827	0.3826	0.38251	0.3824		0.3702	0.37	0.3701	0.37	0.3698	0.3696	0.3698	0.3699	0.37
10	0.3841	0.3841	0.384	0.38395	0.3839		0.3701	0.37	0.3701	0.37	0.3699	0.3697	0.3699	0.37	0.3701
11	0.3855	0.3855	0.3854	0.38537	0.3853		0.3702	0.3697	0.3701	0.3702	0.37	0.3695	0.37	0.3702	0.3703
12	0.3869	0.3869	0.3868	0.38677	0.3867		0.3706	0.3705	0.3706	0.3706	0.3704	0.3702	0.3703	0.3705	0.3705
13	0.3883	0.3883	0.3882	0.38815	0.3881		0.3713	0.3711	0.3711	0.371	0.3708	0.3706	0.3707	0.3708	0.3709
14	0.3898	0.3898	0.3897	0.3895	0.3894		0.372	0.3715	0.3718	0.3716	0.3713	0.3707	0.3711	0.3712	0.3712
15	0.3913	0.3913	0.3912	0.39081	0.3905		0.3733	0.373	0.3728	0.3725	0.3721	0.3717	0.3716	0.3717	0.3717
16	0.3929	0.3929	0.3928	0.39207	0.3914		0.375	0.3744	0.3739	0.3734	0.3728	0.3723	0.3722	0.3721	0.3721
17	0.3943	0.3947	0.3952	0.39324	0.3916		0.3771	0.3757	0.3751	0.3743	0.3735	0.3725	0.3726	0.3726	0.3725
18	0.3954	0.3965	1	0.39406	0.3902	0.3856	0.3807	0.3781	0.3765	0.3753	0.3743	0.3735	0.3732	0.373	0.3729
19	0.3954	0.3957	0.3957	0.39283	0.3895	0.3858	0.3822	0.3795	0.3775	0.376	0.3749	0.3741	0.3736	0.3733	0.3732
20	0.3953	0.3951	0.3943	0.39209	0.3892	0.3859	0.3827	0.3801	0.378	0.3764	0.3753	0.3744	0.3739	0.3735	0.3734

(a)



(b)

of Excel is limited to about 25 cells, so graphs are not available for higher resolutions. However, this is not a serious limitation, since the cell values are displayed in the table. Simple conditional formatting may be used to color-code the results directly on the spreadsheet without the need for a separate graph.

Further applications

The technique described may be used to construct more complicated geometries. In general, plane thicknesses are not always the same, as ground planes are typically thicker than power planes. Further, power planes may be split rather than uniform, or the "power plane" may be simply a very wide trace on a signal layer. With the described technique, a model for each plane may be constructed and a "difference" sheet created to examine the voltage difference at different load points. Separate temperature and resistance sheets can also aid in constructing more complicated geometries.

One common concern is the voltage drop that occurs due to the "Swiss-cheese" effect of having many vias located in and around high-density ICs. This problem may be addressed by inclusion of the nonuniform resistive effects described in Equations 3, 7, 11, and 15 in the spreadsheet model. Model the resistance of the square by taking the ratio of the copper area to the "empty" area (where vias occur) and increasing the resistance for that square by the ratio.

Including local temperature effects

The copper resistance is a function of temperature, as noted previously. Localized heating due to FPGAs or DSPs will increase the temperature and thus the resistance of the copper around the load points. This variable may be included in models by creating an expected temperature map of the PCB and adjusting the effective resistance for each square according to the local temperature on the board. Again, this requires the inclusion of the nonuniform resistance equations.

Conclusion

The voltage drop of PCB power and ground planes can be a significant contributor to the total voltage-tolerance budget for processor cores. Excel and other spreadsheet software with circular reference /iteration capabilities may be used to construct a model of the PCB that can greatly assist the designer in selecting copper thickness and remote sensing locations, proportioning the voltage-tolerance budget, and optimizing the bypass capacitance necessary to meet transient requirements. The spreadsheet results also provide guidance for power-supply and processor placement.

Related Web sites

dsp.ti.com
www.ti.com/sc/device/TPS40140

A copy of the finished spreadsheet is available for download at: **www.ti.com/lit/zip/slyt274**

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