

# Designing DC/DC converters based on SEPIC topology

By Jeff Falin  
Senior Applications Engineer

## Introduction

The single-ended primary-inductance converter (SEPIC) is a DC/DC-converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of conversion is handy when the designer uses voltages (e.g., 12 V) from an unregulated input power supply such as a low-cost wall wart. Unfortunately, the SEPIC topology is difficult to understand and requires two inductors, making the power-supply footprint quite large. Recently, several inductor manufacturers began selling off-the-shelf coupled inductors in a single package at a cost only slightly higher than that of the comparable single inductor. The coupled inductor not only provides a smaller footprint but also, to get the same inductor ripple current, requires only half the inductance required for a SEPIC with two separate inductors. This article explains how to design a SEPIC converter with a coupled inductor.

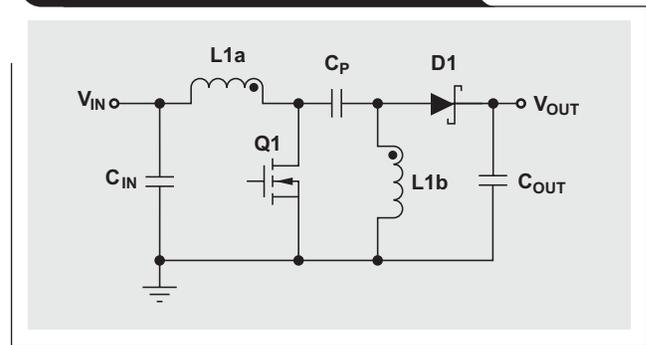
## Basic operation

Figure 1 shows a simple circuit diagram of a SEPIC converter, consisting of an input capacitor,  $C_{IN}$ ; an output capacitor,  $C_{OUT}$ ; coupled inductors L1a and L1b; an AC

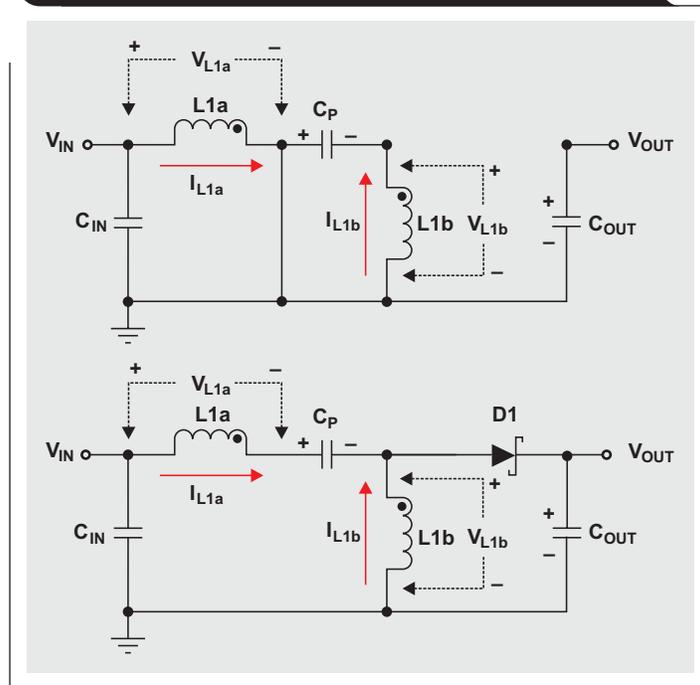
coupling capacitor,  $C_P$ ; a power FET, Q1; and a diode, D1. Figure 2 shows the SEPIC operating in continuous conduction mode (CCM). Q1 is on in the top circuit and off in the bottom circuit.

To understand the voltages at the various circuit nodes, it is important to analyze the circuit at DC when Q1 is off and not switching. During steady-state CCM, pulse-width-modulation (PWM) operation, and neglecting ripple voltage,

**Figure 1. Simple circuit diagram of SEPIC converter**



**Figure 2. SEPIC during CCM operation when Q1 is on (top) and off (bottom)**



capacitor  $C_P$  is charged to the input voltage,  $V_{IN}$ . Knowing this, we can easily determine the voltages as shown in Figure 3.

When Q1 is off, the voltage across L1b must be  $V_{OUT}$ . Since  $C_{IN}$  is charged to  $V_{IN}$ , the voltage across Q1 when Q1 is off is  $V_{IN} + V_{OUT}$ , so the voltage across L1a is  $V_{OUT}$ . When Q1 is on, capacitor  $C_P$ , charged to  $V_{IN}$ , is connected in parallel with L1b, so the voltage across L1b is  $-V_{IN}$ .

The currents flowing through various circuit components are shown in Figure 4. When Q1 is on, energy is being stored in L1a from the input and in L1b from  $C_P$ . When Q1 turns off, L1a's current continues to flow through  $C_P$  and D1, and into  $C_{OUT}$  and the load. Both  $C_{OUT}$  and  $C_P$  get recharged so that they can provide the load current and charge L1b, respectively, when Q1 turns back on.

### Duty cycle

Assuming 100% efficiency, the duty cycle,  $D$ , for a SEPIC converter operating in CCM is given by

$$D = \frac{V_{OUT} + V_{FWD}}{V_{IN} + V_{OUT} + V_{FWD}}, \quad (1)$$

where  $V_{FWD}$  is the forward voltage drop of the Schottky diode. This can be rewritten as

$$\frac{D}{1-D} = \frac{V_{OUT} + V_{FWD}}{V_{IN}} = \frac{I_{IN}}{I_{OUT}}. \quad (2)$$

$D(\max)$  occurs at  $V_{IN(\min)}$ , and  $D(\min)$  occurs at  $V_{IN(\max)}$ .

### Selecting passive components

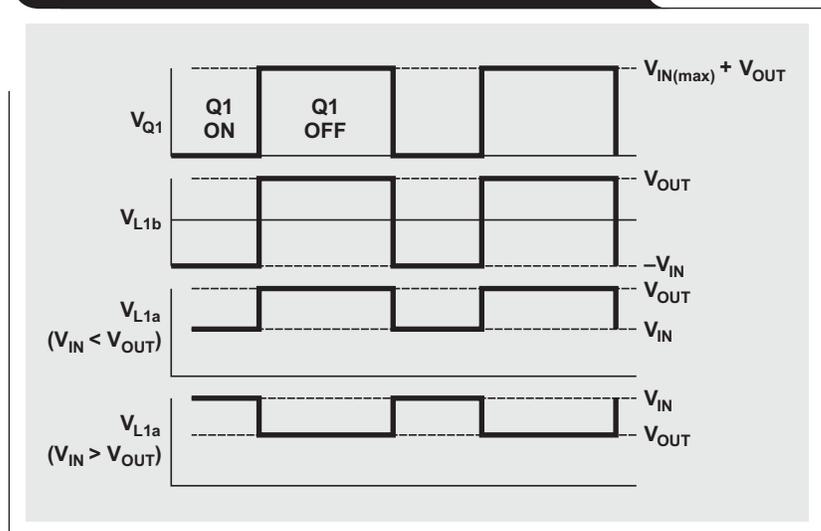
One of the first steps in designing any PWM switching regulator is to decide how much inductor ripple current,  $\Delta I_L$ , to allow. Too much increases EMI, while too little may result in unstable PWM operation. A rule of thumb is to use 20 to 40% of the input current, as computed with the power-balance equation,

$$\Delta I_L = 30\% \times \frac{I_{IN}}{\eta} = 30\% \times I_{IN}'. \quad (3)$$

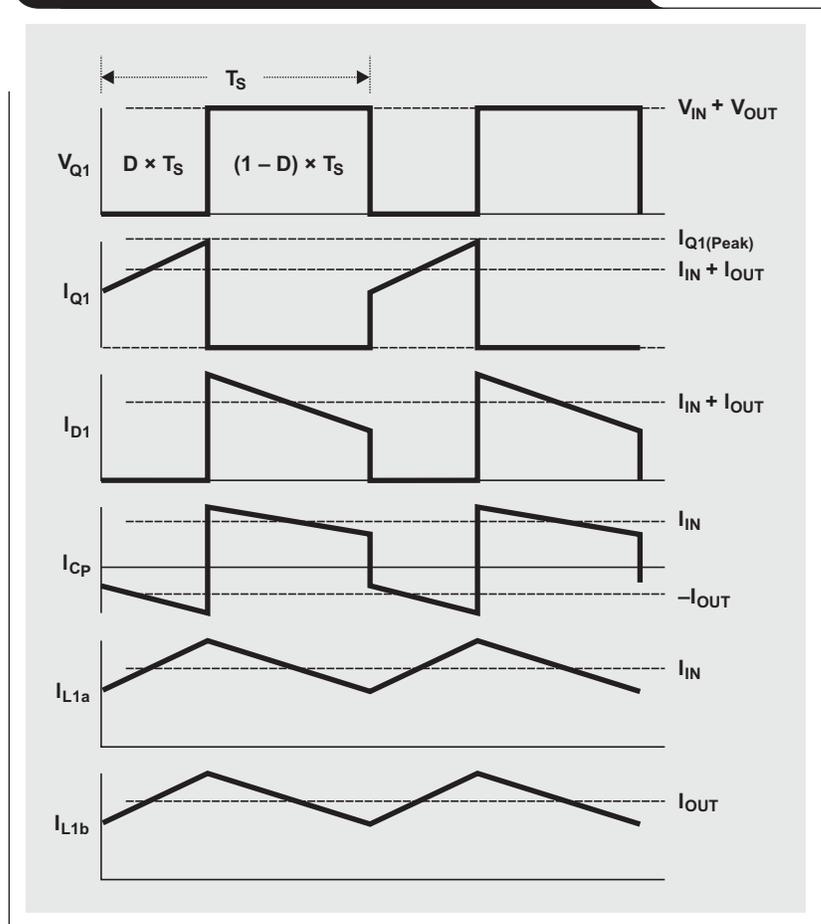
In this equation,  $I_{IN}$  from Equation 2 is divided by the estimated worst-case efficiency,  $\eta$ , at  $V_{IN(\min)}$  and  $I_{OUT(\max)}$  for a more accurate estimate of the input current,  $I_{IN}'$ .

In an ideal, tightly coupled inductor, with each inductor having the same number of windings on a single core, the mutual inductance forces the ripple current to be split equally between the two coupled inductors. In a real coupled inductor, the inductors do

**Figure 3. SEPIC component voltages during CCM**



**Figure 4. SEPIC component currents during CCM**



not have equal inductance and the ripple currents will not be exactly equal. Regardless, for a desired ripple-current value, the inductance required in a coupled inductor is estimated to be half of what would be needed if there were two separate inductors, as shown in Equation 4:

$$L_{1a(\min)} = L_{1b(\min)} = \frac{1}{2} \times \frac{V_{IN(\min)} \times D(\max)}{\Delta I_L \times f_{SW(\min)}} \quad (4)$$

To account for load transients, the coupled inductor's saturation current rating needs to be at least 20% higher than the steady-state peak current in the high-side inductor, as computed in Equation 5:

$$I_{L1a(\text{Peak})} = I_{IN}' + \frac{\Delta I_L}{2} = I_{IN}' \left( 1 + \frac{30\%}{2} \right) \quad (5)$$

Note that  $I_{L1b(\text{Peak})} = I_{OUT} + \Delta I_L/2$ , which is less than  $I_{L1a(\text{Peak})}$ .

Figure 5 breaks down the capacitor ripple voltage as related to the output-capacitor current. When Q1 is on, the output capacitor must provide the load current. Therefore, the output capacitor must have at least enough

capacitance, but not too much ESR, to meet the application's requirement for output voltage ripple,  $\Delta V_{RPL}$ :

$$\Delta V_{RPL} \leq \frac{I_{OUT} \times D(\max)}{C_{OUT} \times f_{SW(\min)}} + ESR \times [I_{L1a(\text{Peak})} + I_{L1b(\text{Peak})}] \quad (6)$$

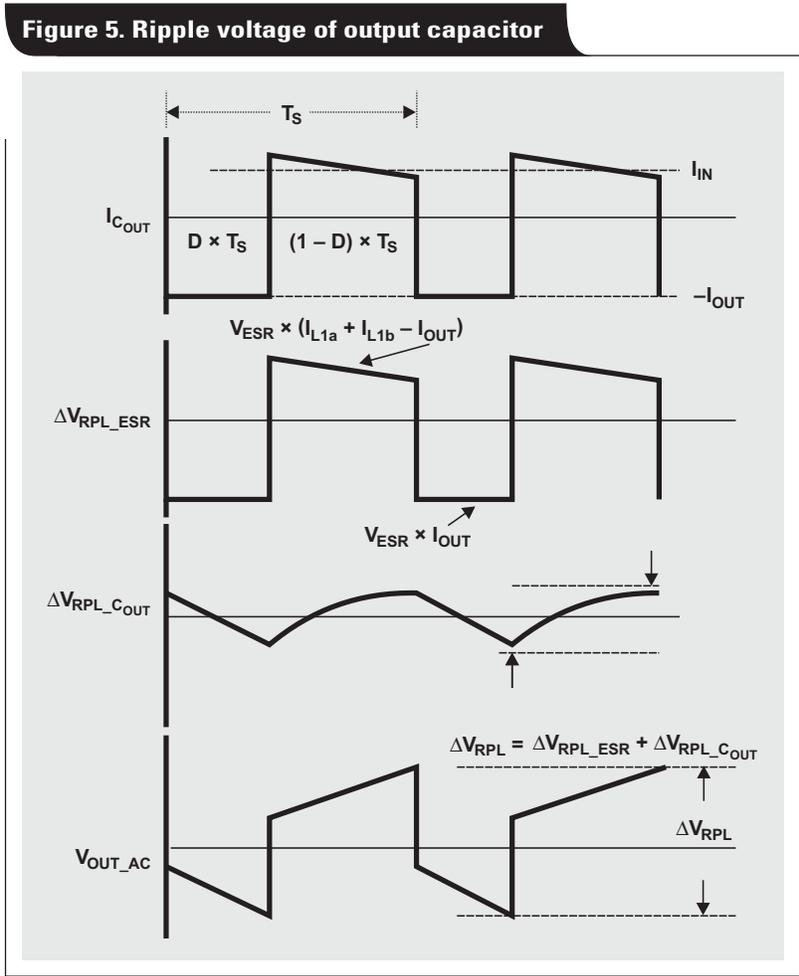
If very low-ESR (e.g., ceramic) output capacitors are used, the ESR can be ignored and the equation reduces to

$$C_{OUT} \geq \frac{I_{OUT} \times D(\max)}{\Delta V_{RPL} \times f_{SW(\min)}}, \quad (7)$$

where  $f_{SW(\min)}$  is the minimum switching frequency. A minimum capacitance limit may be necessary to meet the application's load-transient requirement.

The output capacitor must have an RMS current rating greater than the capacitor's RMS current, as computed in Equation 8:

$$I_{C_{OUT}(\text{RMS})} = I_{OUT} \times \sqrt{\frac{D(\max)}{1 - D(\max)}} \quad (8)$$



The input capacitor sees fairly low ripple currents due to the input inductor. Like a boost converter, the input-current waveform is continuous and triangular; therefore, the input capacitor needs the RMS current rating,

$$I_{C_{IN}(RMS)} = \frac{\Delta I_L}{\sqrt{12}}. \quad (9)$$

The coupling capacitor,  $C_P$ , sees large RMS current relative to the output power:

$$I_{C_P(RMS)} = I_{IN'} \times \sqrt{\frac{1-D(\max)}{D(\max)}} \quad (10)$$

From Figure 3, the maximum voltage across  $C_P$  is

$$V_{Q1(\max)} - V_{L1b(\max)} = V_{IN} + V_{OUT} - V_{OUT} = V_{IN}.$$

The ripple across  $C_P$  is

$$\Delta V_{C_P} = \frac{I_{OUT} \times D(\max)}{C_P \times f_{SW}}. \quad (11)$$

## Selecting active components

The power MOSFET, Q1, must be carefully selected so that it can handle the peak voltage and currents while minimizing power-dissipation losses. The power FET's current rating (or current limit for a converter with an integrated FET) will determine the SEPIC converter's maximum output current.

As shown in Figure 3, Q1 sees a maximum voltage of  $V_{IN(\max)} + V_{OUT}$ . As shown in Figure 4, Q1 must have a peak-current rating of

$$I_{Q1(Peak)} = I_{L1a(Peak)} + I_{L1b(Peak)} = I_{IN'} + I_{OUT} + \Delta I_L. \quad (12)$$

At the ambient temperature of interest, the FET's power-dissipation rating must be greater than the sum of the conductive losses (a function of the FET's  $r_{DS(on)}$ ) and the switching losses (a function of the FET's gate charge) as given in Equation 13:

$$P_{D\_Q1} = I_{Q1(RMS)}^2 \times r_{DS(on)} \times D(\max) + I_{Q1(Peak)} \times [V_{IN(\min)} + V_{OUT} + V_{FWD}] \times \frac{t_{Rise} + t_{Fall}}{2} \times f_{SW}, \quad (13)$$

where  $t_{Rise}$  is the rise time on the gate of Q1 and can be computed as Q1's gate-to-drain charge,  $Q_{GD}$ , divided by the converter's gate-drive current,  $I_{DRV}$ . Q1's RMS current is

$$I_{Q1(RMS)} = \frac{I_{IN'}}{\sqrt{D(\max)}}. \quad (14)$$

The output diode must be able to handle the same peak current as Q1,  $I_{Q1(Peak)}$ . The diode must also be able to withstand a reverse voltage greater than Q1's maximum voltage ( $V_{IN[\max]} + V_{OUT} + V_{FWD}$ ) to account for transients and ringing. Since the average diode current is the output current, the diode's package must be capable of dissipating up to  $P_{D\_D1} = I_{OUT} \times V_{FWD}$ .

## Design example

A DC/DC converter is needed that can provide 12 V at 300 mA (maximum) with 90% efficiency from an input voltage ranging from 9 to 15 V. We select the TPS61170, which has a 38-V switch, a minimum switch-current limit of 0.96 A, and a 1.2-MHz nominal (1.0-MHz minimum) switching frequency. The maximum output voltage ripple allowed is 100 mV<sub>PP</sub>. The maximum ambient temperature is 70°C, and we will use a high-K board. In Reference 1, Ray Ridley explains how to compensate the control loop at the link.

Table 1 summarizes the computations using the equations given earlier. Equations 8 through 11 are not shown because ceramic capacitors with low ESR, high RMS current ratings, and the appropriate voltage ratings were used. Figure 6 shows the schematic. Figure 7 shows the design's efficiency with a Coiltronics DRQ73 inductor and a Würth 744877220. Figure 8 shows the device operation in deep CCM.

## References

1. Ray Ridley. (Nov. 2006). Analyzing the SEPIC converter. *Power Systems Design Europe* [Online]. Available: [http://www.powersystemsdesign.com/design\\_tips\\_nov06.pdf](http://www.powersystemsdesign.com/design_tips_nov06.pdf)
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3. John Betten and Robert Kollman. (Jan. 25, 2006). No need to fear: SEPIC outperforms the flyback. *Planet Analog* [Online]. Available: <http://www.planetanalog.com/showArticle.jhtml?articleID=177103753>

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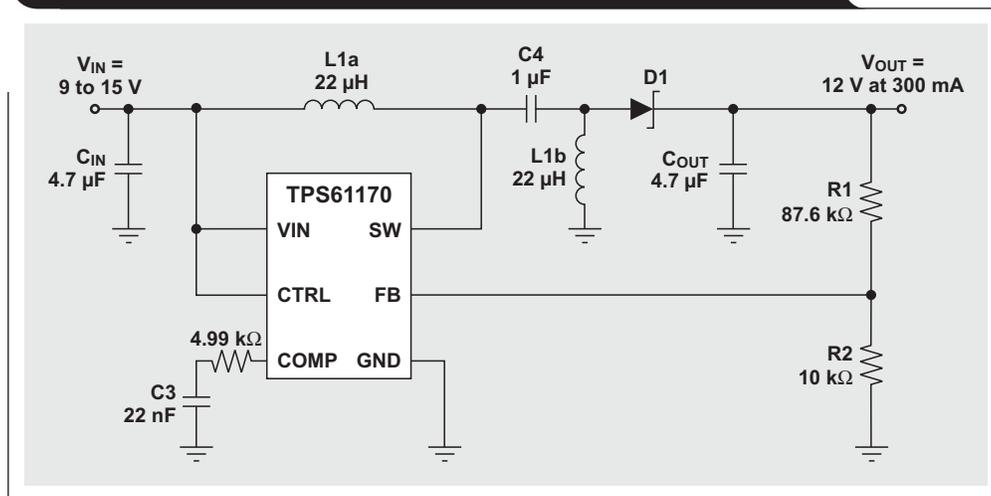
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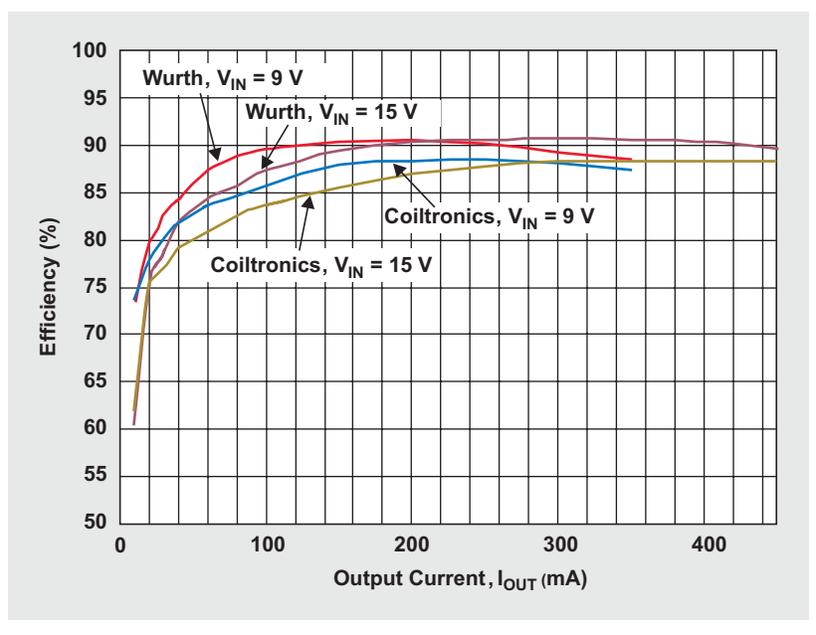
Table 1. Computations for SEPIC design example

DESIGN EQUATION	COMPUTATION	SELECTED COMPONENT/RATING
<b>Passive Components</b>		
(1)	$D(\max) = \frac{12\text{ V} + 0.5\text{ V}}{12\text{ V} + 9\text{ V} + 0.5\text{ V}} = 0.58$	N/A
(2) and (3)	$\Delta I_L = I_{IN}' \times 30\% = \frac{0.3\text{ A} \times 12\text{ V}}{9\text{ V} \times 90\%} \times 30\% = 0.44\text{ A} \times 30\% = 0.13\text{ A}$	N/A
(4)	$L1a = L1b = \frac{1}{2} \times \frac{9\text{ V} \times 0.58}{0.13\text{ A} \times 1\text{ MHz}} = 20.1\text{ }\mu\text{H}$	Coiltronics DRQ73: 22 $\mu\text{H}$ , 1.6 A, and 110 m $\Omega$
(5)	$I_{L1a(\text{Peak})} = 0.44\text{ A} \times \left(1 + \frac{30\%}{2}\right) = 0.51\text{ A}$	
(7)	$C_{OUT} \geq \frac{0.3\text{ A} \times 0.58}{0.1\text{ V} \times 1\text{ MHz}} = 1.74\text{ }\mu\text{F}$	4.7- $\mu\text{F}$ , 25-V X5R ceramic
<b>Active Components</b>		
(12)	$I_{Q1(\text{Peak})} = 0.44\text{ A} + 0.3\text{ A} + 0.13\text{ A} = +0.87\text{ A}$	TPS61170 with 0.96-A-rated switch. Capable of dissipating 825 mW at 70°C.
(14)	$I_{Q1(\text{RMS})} = \frac{0.44\text{ A}}{\sqrt{0.58}} = 0.58\text{ A}$	
(13)	$P_{D_Q1} = (0.58\text{ A})^2 \times 0.3\text{ }\Omega \times 0.58 + 0.87\text{ A} \times (9\text{ V} + 12\text{ V} + 0.5\text{ V}) \times 10\text{ ns} \times 1\text{ MHz} = 246\text{ mW}$	
—	$P_{D_D1} = 0.3\text{ A} \times 0.5\text{ V} = 150\text{ mW}$	MBA140: 1 A, 40 V

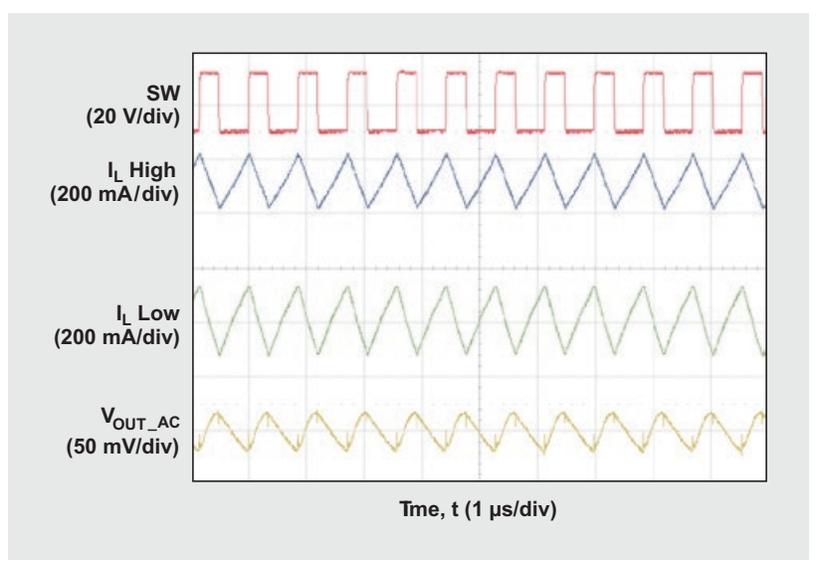
Figure 6. SEPIC design with 9- to 15-V  $V_{IN}$  and 12-V  $V_{OUT}$  at 300 mA



**Figure 7. Efficiency of example SEPIC design**



**Figure 8. Operation at  $V_{IN} = 9$  V and  $I_{OUT} = 200$  mA**



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