Interfacing op amps to high-speed DACs, Part 3: Current-sourcing DACs simplified

By Jim Karki

Member, Technical Staff, High-Performance Analog

Introduction

Most high-speed DACs are current-steering DACs that are designed with complementary outputs that either source or sink current. Part 1 (see Reference 1) of this three-part article series discussed the interface between a current-sinking DAC and an op amp. Part 2 (see Reference 2) discussed the interface between a current-sourcing DAC and an op amp. This interface allows the designer to use the full compliance voltage range of the DAC. This article, Part 3, discusses interfacing a current-sourcing DAC and an op amp by using a simpler approach than that presented in Part 2, along with the associated trade-offs. This article series focuses on using high-speed DACs in end equipment that requires DC coupling, like signal generators with frequency bandwidths of up to 100 MHz and a single-ended output. In these cases, high-speed op amps can provide a good solution for converting the complementary-current output from a high-speed DAC to the required output voltage.

It is assumed that the reader is familiar with the operation of complementary-current-steering DACs, covered in Part 1, and the architecture and compliance voltage of current-sourcing DACs, covered in Part 2.

Simplified op amp interface

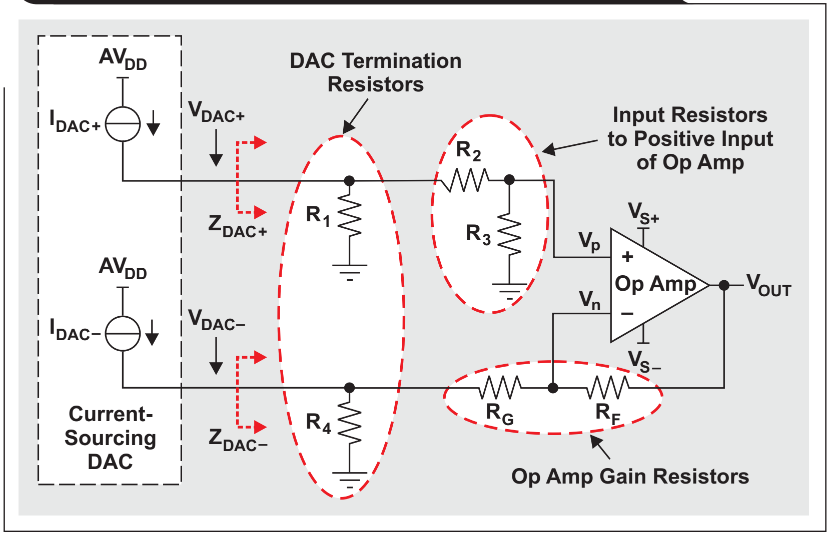
Reference 3 presents a current-sourcing DAC/op amp interface that does not require a negative reference voltage (V_{REF}). The proposed circuit design provides a good working solution, but with one caveat: If the maximum compliance voltage of the DAC is used as a design target on the positive side of the op amp input (V_{DAC+}), the DAC voltage on the negative side ($V_{DAC–}$) will violate the maximum compliance voltage due to an offset that is not at first obvious. The following discussion explains the cause of this offset and proposes an easy workaround. Then a method for inserting a filter between the DAC and op amp is discussed. Please consult Reference 3 for other details concerning the overall design.

Figure 17 shows the proposed circuit with the nomenclature slightly changed from that used in Reference 3 in order to match the circuits presented in Parts 1 and 2 of this article series.

- I_{DAC+} and $I_{DAC–}$ are the current outputs from the DAC.
- R_1 and R_4 are used to adjust the impedance for the DAC outputs to match the design target.
- R_2 and R_3 are input resistors to the positive input of the op amp.
- R_G and R_F are the main gain-setting resistors for the op amp.
- V_{DAC+} and $V_{DAC–}$ are the voltages at the outputs of the DAC.
- V_p and V_n are the input terminals of the op amp.
- V_{S+} and $V_{S–}$ are the power supplies to the op amp.

The op amp is the active amplifier element for the circuit and is configured as a difference amplifier.

Figure 17. Current-sourcing DAC/op amp interface without a negative reference voltage



With no negative reference voltage, the DAC output voltages will not swing below ground, and only positive swings are achieved. On the positive side of the op amp, the voltage is set by the current from the DAC (I_{DAC+}) and the impedance presented by $Z_{DAC+} = R1 \parallel (R2 + R3)$. On the negative side, determining the exact voltage is not as simple due to the action of the op amp, which makes V_n nearly equal to V_p.

Consider the minimum and maximum DAC voltages. On the positive side, the minimum voltage at $I_{DAC+} = 0$ is 0 V, and the maximum voltage when I_{DAC+} is at full scale is $I_{DAC+(FS)} \times Z_{DAC+}$. On the negative side, the minimum voltage at $I_{DAC-} = 0$ is

$$V_n \times \frac{R_4}{R_4 + R_G}.$$

Because the DAC outputs are complementary, when $I_{DAC-} = 0$, I_{DAC+} is at full scale. Using

$$V_p = V_{DAC+}\left(\frac{R_3}{R_2 + R_3}\right)$$

and $V_n = V_p$ for substitution and rearrangement results in a minimum voltage on the negative side of

$$V_{DAC-(min)} = V_{DAC+(max)}\left(\frac{R_3}{R_2 + R_3}\right) \times \left(\frac{R_4}{R_4 + R_G}\right).$$

The maximum voltage when I_{DAC-} is at full scale is $I_{DAC-(FS)} \times R_4 \parallel R_G$. Because the positive-side current is zero ($I_{DAC+} = 0$), there is no contribution from the positive side to the maximum voltage on the negative side.

The result of the foregoing calculations is that V_{DAC-} has a small positive shift in DC level compared to V_{DAC+}. The design equations in Reference 3 account for this positive shift so the op amp output voltage is symmetrical about zero. If the design targets the maximum compliance voltage on the positive side (V_{DAC+}), this positive shift will result in exceeding the compliance voltage on the negative side (V_{DAC-}); therefore a lower voltage should be used as the design target. Due to the interactive nature of the design equations, it was not possible to find a closed-form equation to calculate the maximum allowed voltage for V_{DAC+}, which in essence means that to start the design, the target impedance for Z_{DAC+} must be found. An easy way around this is to set up an Excel® worksheet based on Reference 3 to calculate the component values and DAC output voltages. Different values for Z_{DAC+} can then be tried until an acceptable result is achieved. To view an example worksheet, go to http://www.ti.com/lit/zip/slyt368 and click Open to view the WinZip® directory online (or click Save to download the WinZip file for offline use). Then open the file DAC_Source_to_Op_Amp_Wksht_Part3.xls and select the "Simplified VDAC– Calculation" worksheet tab.

For an example of how to use a worksheet for a design, assume that one of the PMOS DACs noted in Part 2 will be used, with a compliance voltage ranging from –1.0 V to +1.25 V. Since the DAC voltage will be only positive, a reduced voltage ranging from 0 V to +1.25 V will be targeted, and the same worksheet based on Reference 3 will be used.

As in the earlier examples in Parts 1 and 2 of this article series, the DAC's full-scale output is set to 20 mA. A 5-V_{PP}, DC-coupled, single-ended output signal is desired, but this time the circuit shown in Figure 17 is used. Given that $I_{DAC\pm} = 20$ mA and $V_{DAC\pm} = 1.25\ V_{PP}$, the target impedance is calculated as $Z_{DAC\pm} = 62.5\ \Omega$. The THS3095 current-feedback op amp is selected for the amplifier, and R_F is set to 750 Ω. The other items that need to be entered into the worksheet are the gain, which is

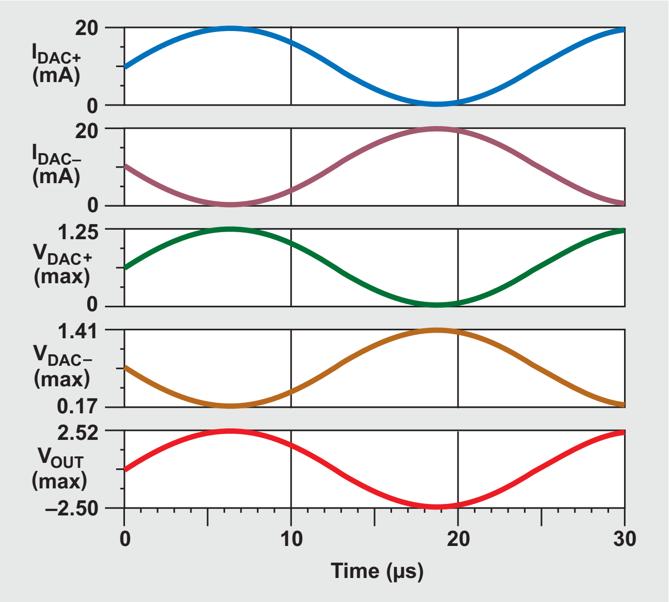
$$\frac{V_{OUT}}{2 \times I_{DAC\pm}} = 125\ \Omega,$$

and lambda (λ), which is set to 0.2 (see page 5 of Reference 3).

With these variables entered, the worksheet shows the following calculated values: $R_G = 425.64\ \Omega$, $R_1 = 121.80\ \Omega$, $R_2 = 24.36\ \Omega$, $R_3 = 104.02\ \Omega$, and $R_4 = 85.13\ \Omega$. The nearest standard 1% values are $R_G = 422\ \Omega$, $R_1 = 121\ \Omega$, $R_2 = 24.3\ \Omega$, $R_3 = 105\ \Omega$, and $R_4 = 84.5\ \Omega$. Using these values in a simulation results in $V_{DAC-(max)} = 1.408$ V, which exceeds the compliance voltage and needs to be reduced. Figure 18 shows the simulation waveforms.

Reducing the target $Z_{DAC\pm}$ to 55 Ω results in a lower target voltage range of 0 V to +1.1 V. With $Z_{DAC\pm} = 55\ \Omega$ and no other change, the worksheet shows the following calculated values: $R_G = 377.03\ \Omega$, $R_1 = 94.83\ \Omega$, $R_2 = 18.97\ \Omega$, $R_3 = 111.98\ \Omega$, and $R_4 = 75.41\ \Omega$. The nearest standard 1% values are $R_G = 374\ \Omega$, $R_1 = 95.3\ \Omega$, $R_2 = 19.1\ \Omega$, $R_3 = 113\ \Omega$, and $R_4 = 75\ \Omega$. The circuit is simulated

Figure 18. Simulation waveforms for maximum V_{DAC}



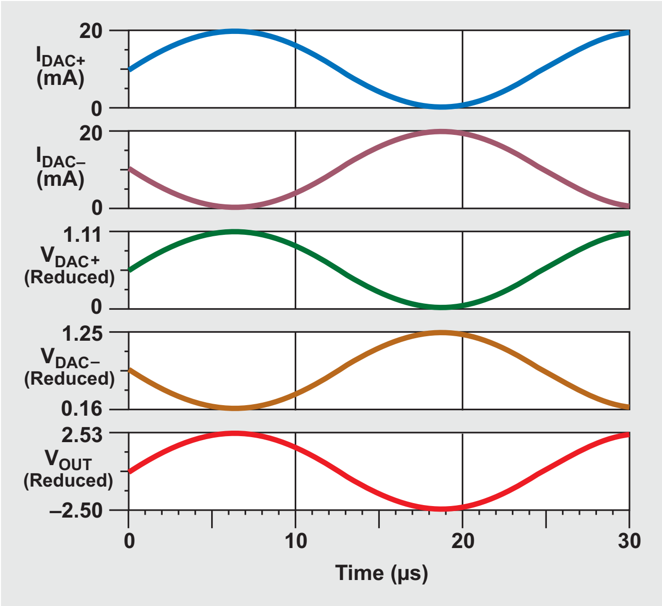
again, and the resulting waveforms (see Figure 19) show that the compliance-voltage specification is just met. The amplitude of the AC sine wave, disregarding the DC offset, is the same at V_{DAC+} and V_{DAC-}. Therefore, when the exact resistor values are used, the iteration process can be shortened by taking the results of the first calculation and making

$$Z_{DAC+} = \frac{V_{DAC+(max)} - V_{DAC-(min)}}{I_{DAC\pm(max)}}$$

in the second try. In the example worksheet, the upper area labeled "Iterative Method" is used for simple trial and error; and the lower area labeled "Shorter Method" uses the results of the first try for the second try, which in this example converges to the same result.

To see a TINA-TI™ simulation of the circuit in this example, go to http://www.ti.com/lit/zip/slyt368 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file Simplified_DAC_Source_Interface.TSC to view the example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button. The simulation circuit and waveforms in this file show that the circuit simulates as expected. I_{DAC+} and I_{DAC-} are the DAC currents, V_{DAC+} and V_{DAC-} are the voltages developed at the DAC outputs, and V_{OUT} is the output of the amplifier. The current-sourcing DAC and op amp are ideal elements constructed with SPICE macros and are intended to show that the equations used are valid for ideal elements. Actual performance will vary depending on selected devices.

Figure 19. Simulation waveforms for reduced V_{DAC}



DAC image-filter considerations

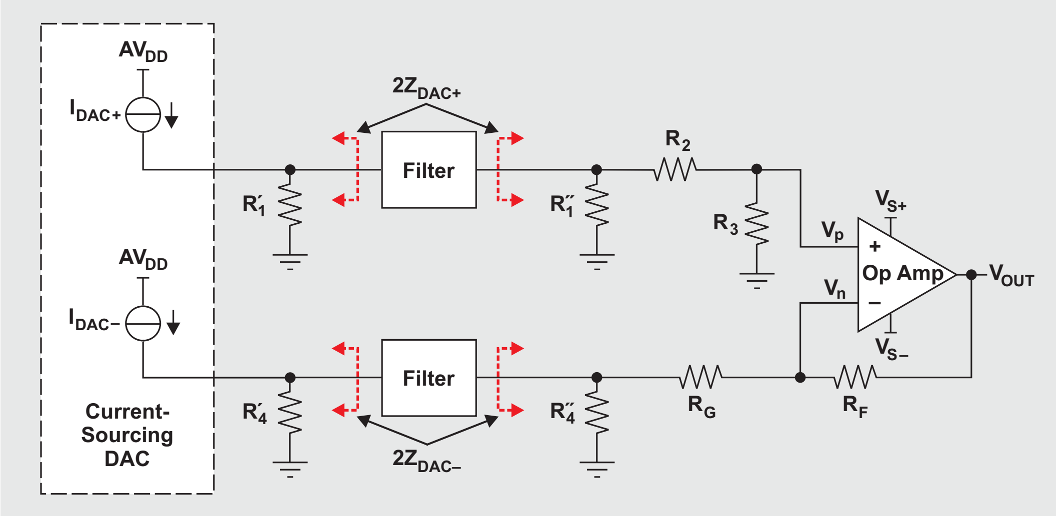
Part 1 discussed the need for a filter to remove the DAC sampling images and recommended that for best performance the filter should be placed directly at the DAC output before the op amp. The situation is the same here. As mentioned in Part 1, it is usually much easier to find standard component values to implement the filter when the input and output impedances to the filter are balanced. Figure 20 shows a proposed circuit implementation where R_1 and R_4 have been replaced with prime and double-prime components on either side of the filter, so that

$$R_1 = R_1' \parallel R_1'',$$

and

$$R_4 = R_4' \parallel R_4''.$$

Figure 20. Inserting DAC image filter



Assuming that R_1 and R_4 are already known, and with the additional constraint that the impedance seen on each terminal of the filter is $2Z_{DAC\pm}$, the new values can be found with the following equations:

$$R_1' = 2Z_{DAC+} \tag{39}$$

$$\frac{1}{R_1''} = \frac{1}{R_1} - \frac{1}{R_1'} \tag{40}$$

$$R_4' = 2Z_{DAC-} \tag{41}$$

$$\frac{1}{R_4''} = \frac{1}{R_4} - \frac{1}{R_4'} \tag{42}$$

These equations are easily solved when set up in a spreadsheet. To see an example Excel worksheet, go to http://www.ti.com/lit/zip/slyt368 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). Then open the file DAC_Source_to_Op_Amp_Wksht_Part3.xls and select the “Simplified VDAC– with Filter” worksheet tab. Similar to the “Simplified VDAC– Calculation” worksheet previously mentioned, the upper area labeled “Iterative Method with Filter” is used for simple trial and error; and the lower area labeled “Shorter Method with Filter” uses the results of the first try for the second try, which in this example converges to the same result.

Please refer to Part 1 for SPICE simulation results that show the effects of matched versus unmatched impedance.

Conclusion

This article has shown a circuit implementation that uses a single-stage op amp to convert differential current outputs from a current-sourcing DAC to a single-ended voltage. This circuit is based on a design methodology presented in Reference 3. This article has also discussed the need to reduce the design’s target voltage on the positive side of the op amp’s input (V_{DAC+}) so that the DAC voltage on the negative side ($V_{DAC–}$) will not violate the maximum compliance voltage. It was shown that such a violation could be due to an offset from the positive side through the action of the op amp, and an easy workaround was proposed to compensate for this offset. A method for inserting a filter between the DAC and the op amp was also shown, along with design equations to compute the new component values.

References

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Document Title	**TI Lit. #**
1. Jim Karki, “Interfacing Op Amps to High-Speed DACs, Part 1: Current-Sinking DACs,” *Analog Applications Journal* (3Q 2009)	slyt342
2. Jim Karki, “Interfacing Op Amps to High-Speed DACs, Part 2: Current-Sourcing DACs,” *Analog Applications Journal* (4Q 2009)	slyt360
3. Michael Steffes, “Wideband Complementary Current Output DAC to Single-Ended Interface: Improved Matching for the Gain and Compliance Voltage Swing,” Application Report	sbaa135

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