Design of a 60-A interleaved active-clamp forward converter

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Introduction

In 48-V-input telecommunications systems, power supplies with a capacity of 100 to 250 W are sufficient to cover many applications. Forward converters are a good choice for these applications. At lower output voltages, synchronous rectification in the secondary circuitry improves efficiency and simplifies system thermal design. Active-clamp forward converters work well in these applications because of the ease of implementing synchronous rectification.

In most cases, the output currents of forward converters are commonly limited to around 30 A. Beyond this current, the inductor design and conduction losses in the secondary circuitry become difficult to manage. From a power standpoint, the primary circuitry (number of parallel FETs) becomes a limiting factor for power ratings above 250 W. In systems with higher power, it is necessary to move to a different topology like the full bridge, or operate two or more forward converters in parallel to increase the output power.

Load-share ICs work great for paralleling supplies that use diodes to rectify their outputs. Diode-rectified supplies allow current to be sourced only from the power supply. Power supplies with synchronous rectifiers, however, can both source and sink power, which can wreak havoc with some load-share controllers. This is particularly true at start-up, where the feedback loop is overridden by the primary controller's slow-start circuit, and the two paralleled supplies could attempt to regulate the output to different voltage levels. These issues can be circumvented by interleaving two separate power stages. This article presents the design of a 5-V, 300-W interleaved isolated supply that is powered from a standard 36- to 72-V telecom input.

Designing the interleaved power stage

In this design example, splitting the power into two interleaved power stages reduces the current in the secondary of each phase to 30 A. This is much more manageable than the 60 A that would be required in a single-phase supply. Both phases actually need to be designed to carry a little more than 30 A to account for phase imbalances. Designing the power stage begins by selecting the turns ratio and inductance for the power transformers. A feature of the active-clamp forward converter is its ability to run at duty cycles of over 50%. It is best to design for a maximum duty cycle of no greater than 75% so that the transformer's reset voltage does not become excessive. In this example, a turns ratio of 4.5:1 results in a duty cycle of around 63% at a 36-V input. Switching each phase at 200 kHz provides a good balance between size and efficiency. Setting the primary inductance at 100 µH ensures that sufficient magnetizing current is flowing to drive the commutation of the power MOSFETs during the switching transitions. The primary inductance and switching frequency determine the value of the resonant capacitor in the clamp. In this case, a 0.1-µF capacitor sets the resonant frequency at 50 kHz.

The output inductors are determined just as in any buck-derived topology. An inductance of 2 µH is used, resulting in 8.5 A of peak-to-peak ripple current in each phase with a worst-case input of 72 V. Accounting for a 20% phase imbalance, the inductor must be able to carry at least 41 A of peak current without saturating.

The output capacitors are selected to meet the requirements for output ripple voltage and for voltage excursions due to load transients. Interleaving the power stages results in some cancellation of the ripple current seen by the output capacitors. The amount of ripple-current cancellation is dependent on the duty cycle and the phase angle between the two phases. Total cancellation occurs with a 50% duty cycle only when the two phases are synchronized 180° out of phase. This reduction in ripple current reduces the number of capacitors required based on the ripple-voltage requirements and the RMS current ratings of the capacitors. For this design, four 180-µF polymer capacitors rated for 4-A RMS each are sufficient to keep the peak-to-peak ripple voltage below 50 mV. More capacitance can be added to support large load transients if necessary.

Selecting the primary MOSFETs is also straightforward. The peak drain voltage is the sum of the input voltage and the resonant transformer's reset voltage. The RMS primary current comprises the reflected load current and the transformer magnetizing current. It is important to select a minimal number of cost-effective transistors and to keep the power loss in each transistor manageable. For this design, each phase uses two 150-V, 50-mΩ MOSFETs in parallel, with a worst-case loss per FET of approximately 700 mW.

Figure 1 shows how self-driven synchronous rectifiers are implemented in each phase of the active-clamp forward converter. One set of synchronous rectifiers (Q4, Q5, and Q6) sees the input voltage reflected through the transformer, while the other set (Q1, Q2, and Q3) sees the transformer's reset voltage reflected to the secondary side. With the selected turns ratio, MOSFETs rated at 30 V are sufficient for this design. Most of the power loss in these components is due to conduction loss. Paralleling multiple 7-mΩ MOSFETs for each phase results in a worst-case loss per FET of around 800 mW. This ensures that the junction temperatures are reasonable, even with a 20% phase imbalance. The gate-drive components Q12, Q13, Q15, and Q16 serve two functions. First, they protect the MOSFET gates from voltage spikes on the switching waveforms. Second, they provide a buffer so that the transformer's secondary windings are not directly connected to a large amount of gate capacitance. This is important to ensure that the power MOSFETs commutate quickly during the switching transitions.

Figure 1. Gate-drive conditioning circuitry for a self-drive synchronous rectifier

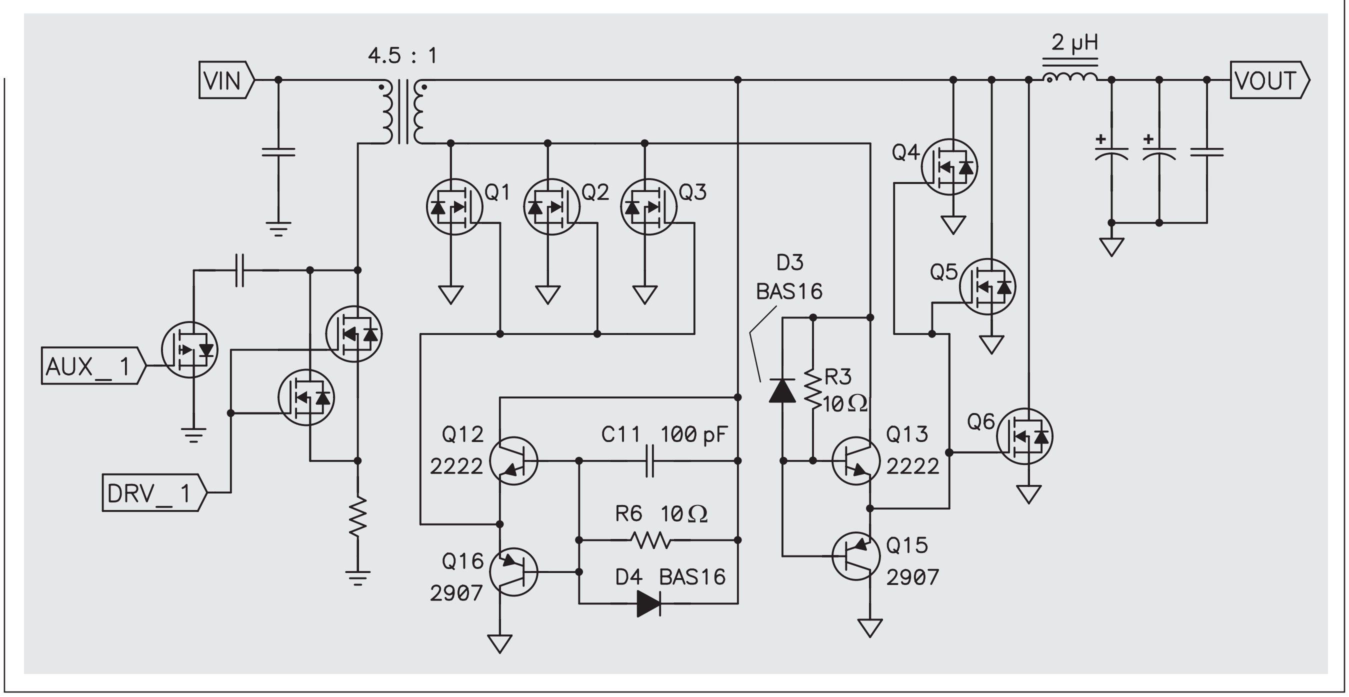


Figure 2. Interleaved controllers sharing feedback network and soft-start circuit

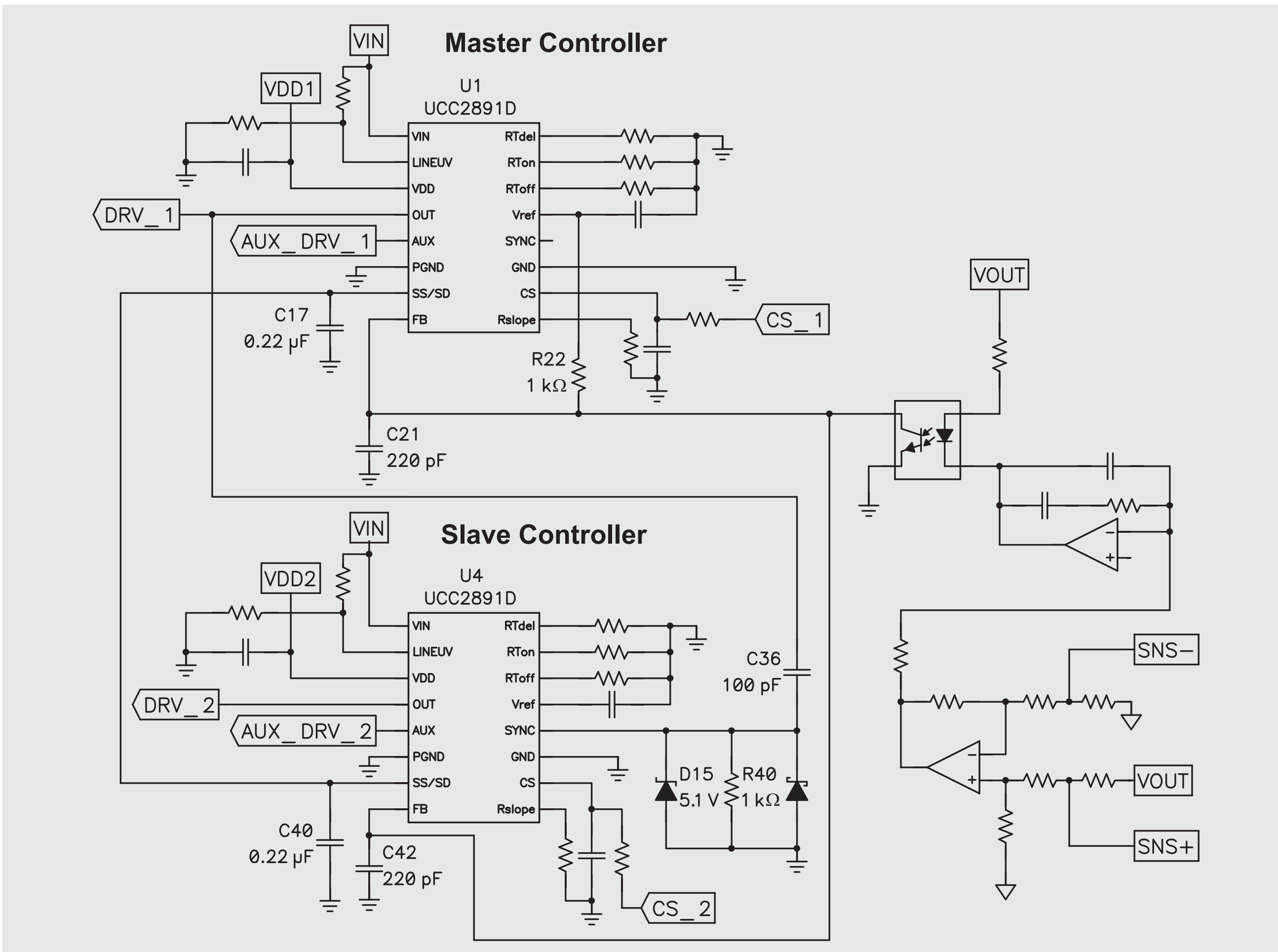
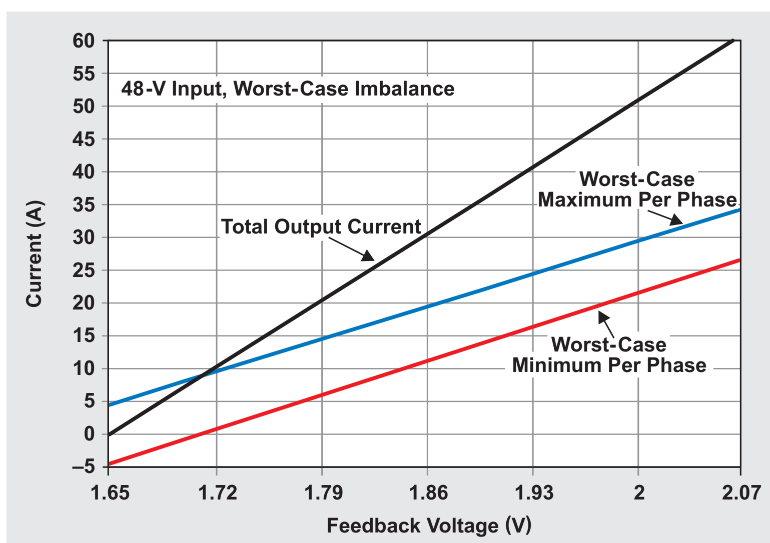


Figure 2 shows how two controllers can be connected in parallel so that they share a common feedback signal and soft-start circuit. With peak-current-mode control, each power stage behaves as a current source that is controlled by the voltage at the feedback pin. A single error amplifier regulates the output voltage by simultaneously controlling the feedback pins of the two controllers. Current imbalance between the two phases is mostly determined by variations of the offsets inside the controllers and by the tolerances of the current sense and slope compensation. Figure 3 plots the current in each phase versus the feedback voltage for a total tolerance resulting in the maximum error between phases. This is not of much concern at high load levels, as one stage will just carry a heavier burden. At light loads, however, the error can allow one phase to sink current, forcing the other phase to source extra current. This leads to increased losses at

Figure 3. Variation in offsets can lead to phase-current imbalance



light loads. The phase imbalance must also be considered when the current limit is programmed.

Synchronization is implemented by designating one controller as the master and the other as the slave. The clock frequency of the slave controller is set 10% slower than that of the master clock to ensure synchronization. The gate-drive signal of the master is used as the clock for the slave. Some conditioning components are needed to shape the magnitude and duration of the synchronization pulse.

For proper start-up, timing is critical. Start-up must be completed before the V_{DD} voltage on either chip falls below the UVLO OFF level, or neither controller will be able to start. Tying the two soft-start pins together ensures that both converters initiate the start-up sequence at the same time. In case of a fault, this also allows both controllers to be disabled by discharging the soft-start capacitance.

The efficiency of this power supply is shown in Figure 4. With a nominal 48-V input and a load current of 60 A, the supply's efficiency is over 92%. The converter's ability to convert to an isolated and regulated 5-V output with no intermediate bus and minimal power loss simplifies the system design and reduces the power demand on the upstream AC/DC rectifier.

Conclusion

In summary, interleaving active-clamp forward power stages can result in a cost-effective and efficient design. The design must account for current imbalances between the phases and ensure proper synchronization and start-up. If properly designed, interleaving extends the practical power range of the active-clamp forward converter to around 500 W and easily supports load currents of up to 60 A.

Please visit www.ti.com/tool/PMP2214 for more information on this design, including the complete schematic, bill of materials, and test results.

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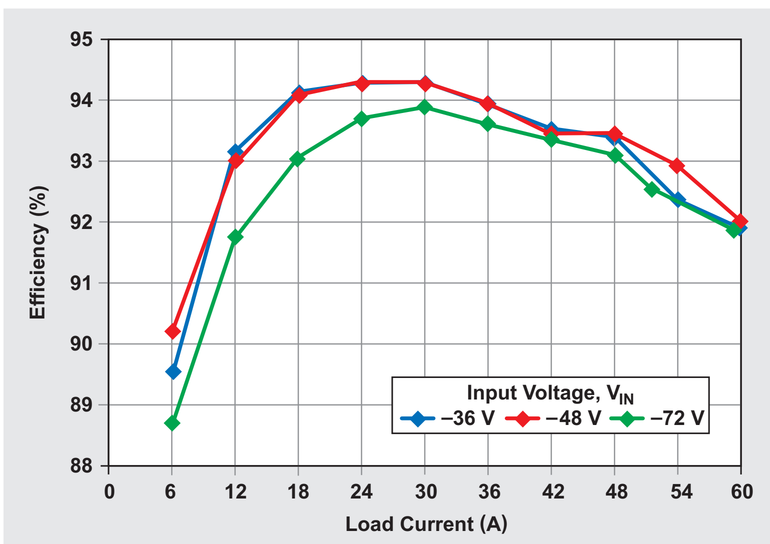
Figure 4. Synchronous rectification enables very high efficiency



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