High-Performance Analog Products

Analog Applications Journal

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Contents

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Introduction

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High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions

By Chris Glaser
Applications Engineer

Texas Instruments (TI) offers synchronous buck converters with DCS-Control™ technology, a regulation topology of Direct Control with Seamless transition into power-save mode. This topology incorporates the advantages of the voltage-mode, current-mode, and hysteretic control topologies while providing a clean entry into power-save mode. This article discusses how the DCS-Control topology works, demonstrating its low output-voltage ripple in power-save mode, its superb transient response, and its seamless mode transitions.

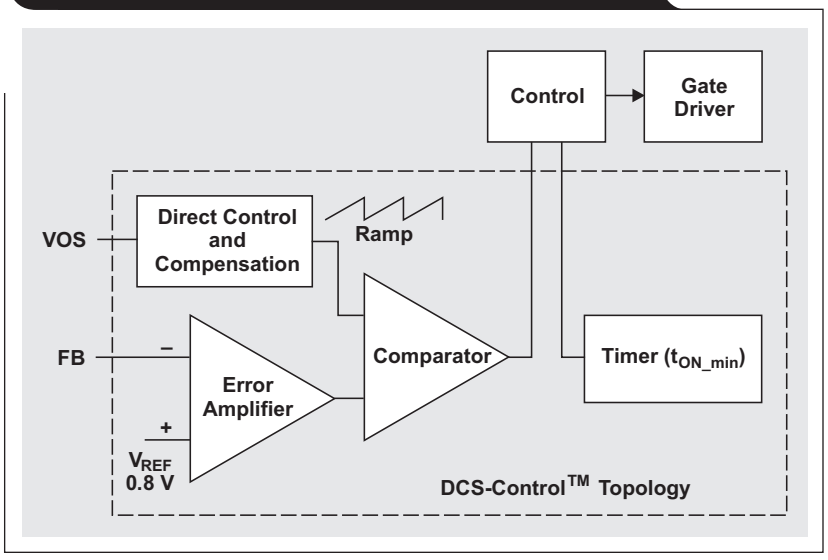
Basic operation

The DCS-Control topology fundamentally is a hysteretic topology. However, it incorporates several circuits that provide the advantages of the voltage- and current-mode topologies. Figure 1 shows the basic block diagram of the DCS-Control topology, taken from the datasheet of TI's TPS62130 step-down converter.[1]

There are two inputs to the DCS-Control topology: a feedback (FB) pin and an output-voltage sense (VOS) pin. The FB pin's input behaves the same as in most DC/DC converters. It is the high-impedance input to an error amplifier, or operational amplifier, whose purpose is to output an error signal of the FB pin to an internal reference voltage, V_{REF}. As in other DC/DC converters, the error amplifier provides precise output-voltage regulation. A voltage divider between the output voltage, FB pin, and ground programs the output voltage's set point. For some devices, like TI's TPS62131, the FB pin is connected internally by using a voltage divider from the VOS pin. This sets the output voltage, reduces the external component count by two, and reduces the FB pin's sensitivity. Appropriate compensation is included around the error amplifier to ensure its stability.

The VOS pin is connected directly to the converter's output voltage at the output capacitor. Like the FB pin, this is a high-impedance input into the control loop. Unlike the FB pin, the VOS pin enters a proprietary circuit, which creates a voltage ramp. This ramp is then compared to the error signal from the error amplifier, as in voltage- or current-mode control. This path from the VOS pin to the comparator provides the fast hysteretic response of the DCS-Control topology. Changes in the output voltage at VOS are directly fed to the comparator and immediately affect the device's operation. For this reason, the VOS pin is noise-sensitive; so the output voltage's route should be as short and direct as possible from the output capacitor back to the device's VOS pin. Appropriate compensation is included around the VOS pin's circuitry to ensure its stability.

Figure 1. Block diagram of DCS-Control™ topology



The comparator then outputs a signal to the control circuit, telling it whether or not to output a switching pulse to the gate driver, which controls the high-side MOSFET. The comparator works with the timer circuit to provide both the fastest response to load transients and a regulated switching frequency.

Based on the ratio of V_{OUT} to V_{IN}, the timer sets a minimum ON time (t_{ON_min}) that can extend the ON-time control from the comparator. The minimum ON time set by the timer typically is shown in the device datasheet with an equation, such as

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400 \text{ ns}.$$

In this example based on the TPS62130, the target switching period is 400 ns; therefore, the switching frequency is its reciprocal, or 2.5 MHz. A regulated switching frequency is maintained over the input and output voltage ranges due to the V_{OUT}/V_{IN} factor, which adjusts the minimum ON time based on the ideal duty cycle for a buck converter. Thus, the ON-time equation also can be written as $t_{ON} = D \times t_{Period}$, which is the exact definition of ON time for any buck converter.

The control of the low-side MOSFET is simple. After the high-side MOSFET turns off, the low-side MOSFET turns on and efficiently ramps down the inductor current. The low-side MOSFET turns off when either the inductor current decays to zero, or the high-side MOSFET is told by the comparator to turn on again. An appropriate dead time is implemented to avoid shoot-through currents in the MOSFETs.

Power-save mode

A key component of the DCS-Control topology is its power-save mode. Generally, most power-save modes activate at lower load currents and increase the conversion efficiency by skipping switching pulses and reducing the device's current consumption (quiescent current). Skipping switching pulses operates the device in discontinuous conduction mode (DCM), which eliminates the negative inductor current (current flowing from the output towards the input) that otherwise would occur at light loads. Such current merely undoes the work of previous switching cycles and incurs additional losses, which decrease efficiency. Reducing the quiescent current improves the efficiency at very light loads, as explained in detail in Reference 2.

The power-save mode in the DCS-Control topology is very simple. It is implemented with the same circuitry as described earlier—there is no switching between two different control modes during the transition from power-save mode to PWM mode. Some other control topologies switch between one control method for power-save mode and a different one for PWM mode. This creates the opportunity for glitches and random noise to occur during the transition. More details about these phenomena are provided later in this article under "Seamless transition."

The DCS-Control topology implements its power-save mode in a straightforward way: If the comparator does not need a switching pulse, then no pulse is given. So, if the output voltage is above its set point (as measured by the error amplifier) when the inductor current decays to zero, the device does not output a new switching pulse; instead, it reduces its quiescent current and enters power-save mode. It waits until the error amplifier tells the comparator that the output voltage has decreased to its set point and should now be increased. Then the device outputs a switching pulse that lasts for the minimum ON time, raising the output voltage just high enough to stay within regulation. Minimum propagation delays through these circuits result in high efficiency and well-regulated output voltage during power-save mode.

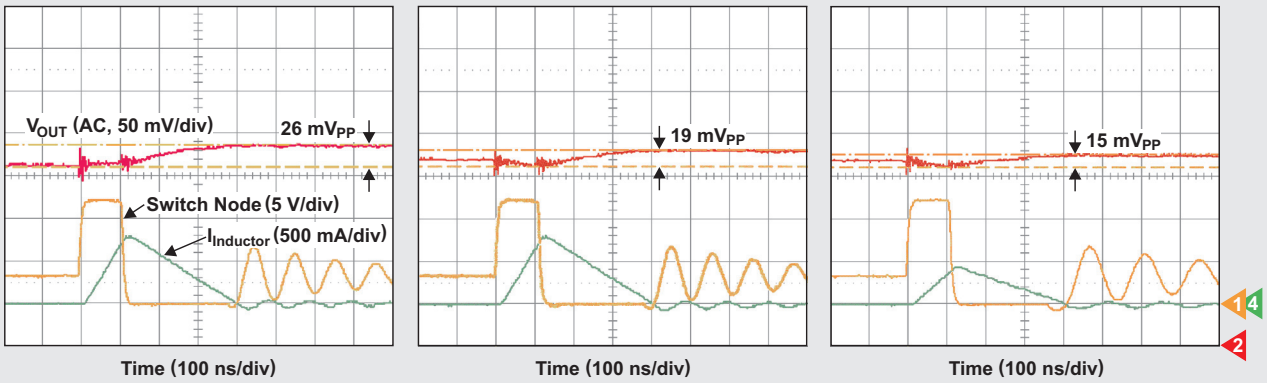
A single switching pulse persisting for the minimum ON time transfers the smallest possible amount of energy to the output, creating the smallest amount of output-voltage ripple. As the light-load current increases, the single pulses occur closer together and increase the switching frequency above the audio band at a faster rate than other power-save topologies. Other topologies use groups or bursts of pulses during the power-save mode that cause much more energy than required to be transferred to the output during a burst. Since the output voltage takes more time to drop back down to its set point, the bursts are spaced further apart, keeping the effective frequency in the audio range longer. The single-pulse architecture of DCS-Control allows operation above the audio band at lower load currents than these other topologies. A case study of the noise performance in power-save mode is given in Reference 3.

When the load increases enough such that there is no time between the single pulses, the inductor current does not return to zero before the comparator tells the high-side MOSFET to turn on again. This load condition occurs at the DCM boundary and is where the converter exits power-save mode and enters PWM mode.

Output-voltage ripple in power-save mode

This combination of predictable operation in power-save mode (a single pulse for the minimum ON time) and entry into PWM mode when a zero inductor current is reached makes the DCS-Control topology much more flexible than other topologies, allowing easier configuration to system

Figure 2. TPS62130's output-voltage ripple



(a) With default EVM

(b) With additional 22-µF output capacitor

(c) With additional 22-µF output capacitor and inductor increased to 2.2 µH

requirements. As an example, consider the output-voltage ripple in the power-save mode of a system with a 12-V input and 3.3-V output. TI's TPS62130 evaluation module (EVM),[4] operating at the 2.5-MHz setting, was used for Figure 2 to demonstrate how to decrease the ripple by increasing the external inductance and output capacitance. The no-load condition was used to show the worst-case output-voltage ripple in power-save mode.

Figure 2a shows the already low output-voltage ripple of 26 mV peak-to-peak, or 0.8% of the 3.3-V output voltage, obtained with the default circuit. Increasing the output capacitance decreases the output-voltage ripple, since the same amount of energy is transferred during each switching pulse. With more output capacitance, this fixed energy results in less voltage ripple (Figure 2b). Increasing the inductance reduces the peak current reached in a switching pulse, since the ON time remains the same. Since a lower peak current stores less energy ($E = \frac{1}{2} \times L \times I^2$), less energy is transferred to the output, again resulting in less voltage ripple (Figure 2c). Note that the ON time is the same for each circuit because it is fixed inside the device and cannot be changed by the external components.

The engineer can also set the load current at which power-save mode is entered by adjusting the inductance, which changes the boundary to DCM. A larger inductance results in less inductor-current ripple, which means the inductor current remains above zero down to lower output-current levels. This ability to adapt the power-save mode's entry point and output-voltage ripple to specific needs allows this topology to be used in a variety of applications, including those that are highly sensitive to noise. Examples include low-power wireless transmitters and receivers in medical or industrial applications (see Reference 5), portable power in consumer devices, and power for solid-state drives.

Transient response

Since the DCS-Control topology detects the actual output voltage through the VOS pin, it is well-suited to respond to load transients. This signal is fed directly to the comparator and does not travel through the bandwidth-limited error amplifier before affecting the ON time. Being hysteretic, the DCS-Control topology responds fastest to load transients, a capability that is further enhanced by its device's 100% duty-cycle mode.

In this mode, the device keeps the high-side MOSFET on for as long as necessary for the output voltage to recover. In other words, the ON time demand of the comparator is fully met. Figure 3 shows the TPS62130 EVM's response to a no-load to 1-A-load transient through its 100% duty-cycle mode. The 300-ns time delay between the

Figure 3. TPS62130 EVM's 100% duty-cycle mode during transient response

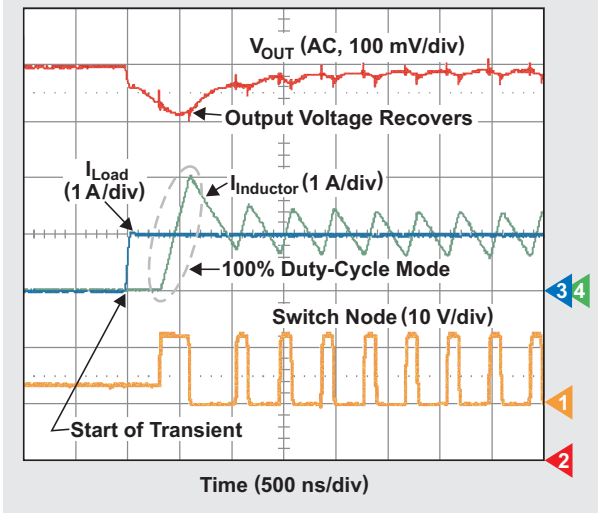
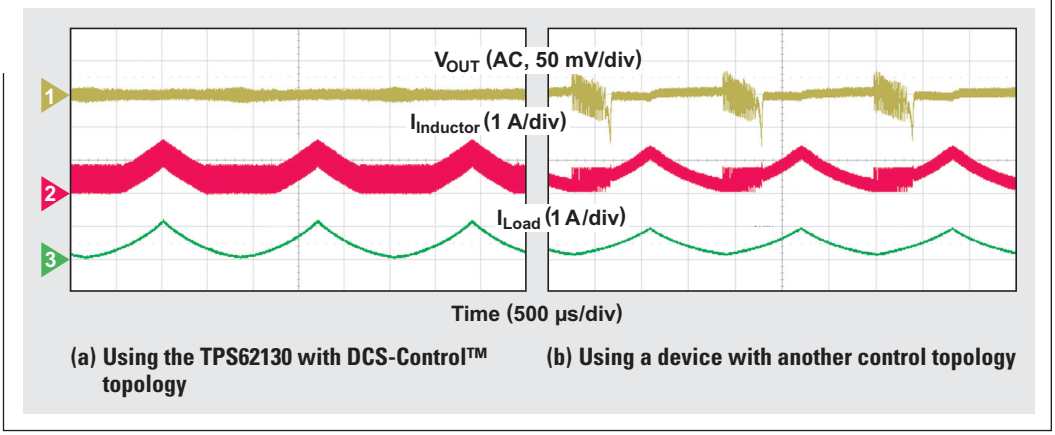


Figure 4. Transition from PWM mode to power-save mode



start of the transient and when the high-side MOSFET turns on means that the transient response is limited almost entirely by large-signal concerns (the inductance) and not by small-signal concerns (the control topology). Thus, the DCS-Control topology is not the main limitation of the transient-response capabilities of the device; rather, it enables outstanding transient response for given output-filter components.

Seamless transition

It was previously noted that, in the DCS-Control topology, only one circuit controls both the PWM and the power-save modes. This allows a faster but also a seamless transition between control modes. It also allows for better performance when the circuit's operating conditions approach the boundary between modes. Since there is no mode switch, there is no glitch at the output.

Figure 4 compares the mode-transition behavior of the TPS62130 to that of a device using another control topology. The load current (bottom trace in green) varies from 10 mA to 1 A in a triangle-like pattern. Both the inductor current and the output-voltage ripple are observed for perturbations or disturbances.

For the TPS62130, which uses the DCS-Control topology, Figure 4 shows much smoother output-voltage and inductor-current waveforms than for the device using another control topology. The TPS62130 outputs lower voltage ripple at all load currents. The ripple increases slightly at lower loads; but, since the device enters power-save mode, this increase is far less than for the device with the other topology. Finally, and most important, there is a relatively large drop in the output voltage (under some limited operating conditions, such as with this load ramp) as the load increases and the device with the other topology exits power-save mode and enters PWM mode. Clearly, this is not desirable for the load or the system and is eliminated with the DCS-Control topology.

Conclusion

The DCS-Control topology is a great improvement over other control topologies because it provides excellent transient response with a seamless transition into power-save mode. Its single-pulse power-save mode provides low output-voltage ripple and improves the performance of numerous types of end equipment and systems, including noise-sensitive applications.

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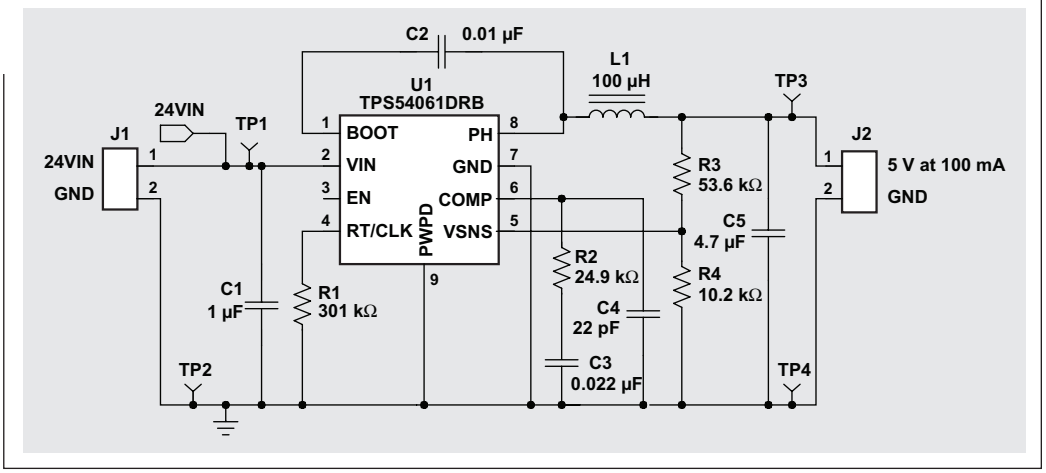
Linear versus switching regulators in industrial applications with a 24-V bus

By Rich Nowakowski, *Product Marketing Manager, Power Management Group,*
and Robert Taylor, *Applications Engineer and Member, Group Technical Staff*

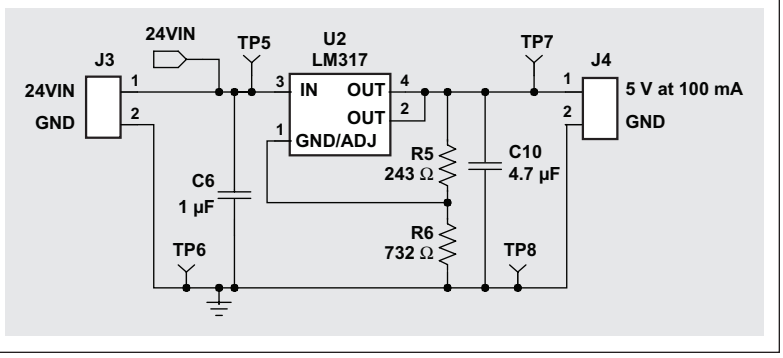
Figure 1. Switching (buck) converter with integrated MOSFETs



Linear regulators have been around for many years. Some designers still use linear regulators that are over 20 years old for new and old projects. Others have made their own linear regulators from discrete components. The simplicity of a linear regulator is hard to beat for a wide range of voltage conversions. However, low-current applications with a 24-V bus, such as for industrial automation or HVAC controls, may have thermal issues if the voltage drop is too large. Fortunately, designers have several choices now that small, high-efficiency, wide-input-voltage switching regulators are available.

This article compares three different solutions that provide a 5-V output at 100 mA from a 24-V bus. A synchronous step-down (buck) converter is compared to an integrated linear regulator and a discrete linear regulator. Size, efficiency, thermal performance, transient response, noise, complexity, and cost are compared to help designers choose the solution that best meets the constraints of a particular application.

Figure 2. Integrated, wide-input-voltage linear regulator



Conditions of comparison

Most industrial applications use a 24-V bus and require 5 V to power various loads, such as logic and low-current microprocessors. An output current of 100 mA is chosen because it accommodates many logic and processor loads. However, the power-dissipation level can affect the decision of whether to use a switching or linear regulator. The circuits shown in Figures 1, 2, and 3 are all built on the same circuit board and use 1-µF input and 4.7-µF output ceramic capacitors with the same ratings.

The design in Figure 1 uses a synchronous buck converter with integrated MOSFETs, the TPS54061 from Texas Instruments (TI). Note that this circuit does not require a catch diode but includes an inductor, five capacitors, and four resistors. The device also employs external compensation and is tuned to use the same input and output capacitors as the linear circuits in Figures 2 and 3.

The design in Figure 2 uses an integrated, wide-input-voltage linear regulator, TI's LM317, which is a popular, industry-standard regulator with a 1.5-A output capability. This circuit uses two external resistors and two external

capacitors. The wide difference between the input and output voltages requires the low thermal resistance of a double-decawatt package (DDPak).

Figure 3 shows a discrete linear regulator that employs a transistor and a Zener diode with two external capacitors and four external resistors. The Zener diode breaks down at 5.6 V, and that voltage is fed to the base of an NPN transistor. Due to the base-emitter voltage drop, the output is regulated to ~5 V. The external resistors are used to help with the power dissipation in the NPN transistor.

Table 1 summarizes the board area and component count of each design.

Linear-regulator solutions require more board area to provide proper thermal relief on the circuit board. At full load, each linear-regulator solution must dissipate about 2 W. As a rule of thumb, approximately 1 W of dissipation in 1 in^2 of board area results in a 100°C temperature rise. The linear-regulator solutions are designed to allow for a 40°C temperature rise. The synchronous buck converter is clearly the design of choice when board area is limited, despite the number of external components and the design effort required to compensate the feedback loop and select the inductor.

Figure 3. Discrete linear regulator

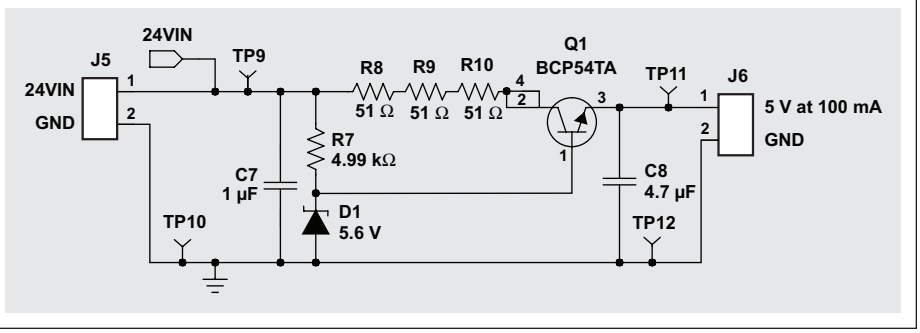


Table 1. Summary of board area and component count

REGULATOR TYPE	BOARD AREA (in^2)	NUMBER OF COMPONENTS	COMPLEXITY
Switching (Buck) (TPS54061)	0.14	11	High
Integrated Linear (LM317)	2.25	5	Low
Discrete Linear (Zener/Transistor)	2.25	8	Medium

Table 2. Summary of thermal performance

REGULATOR TYPE	TEMPERATURE RISE (°C)	MAXIMUM TEMPERATURE (°C)	PACKAGE
Switching	11	40.7	3×3-mm VSON
Integrated Linear	27	56.2	DDPak
Discrete Linear	40	69.1	SOT-23, SOT223

Thermal performance

The thermal image in Figure 4 shows the temperature rise of each design on the circuit board. The board is designed in a manner such that none of the circuits disturb the thermal performance of an adjacent circuit. Table 2 shows that the switching regulator has the lowest temperature rise, at 11°C. With a large difference between the input and output voltages, the switching regulator with synchronous rectification excels in efficiency compared to either

Figure 4. Heat generated from each circuit (white indicates highest temperature)

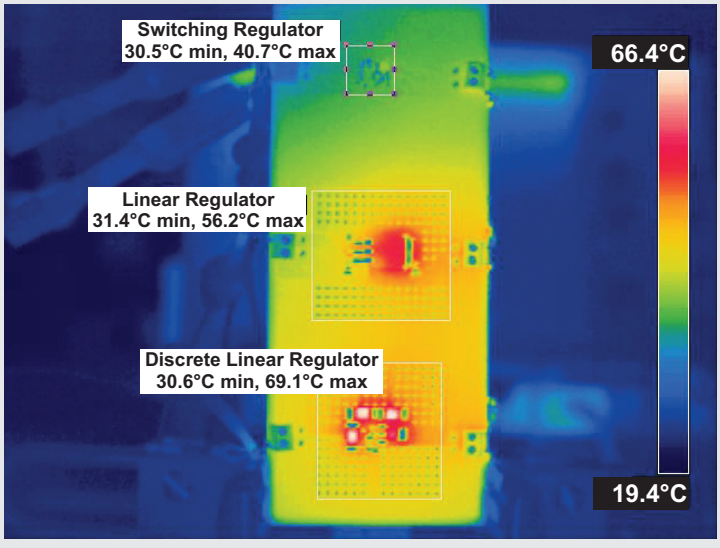


Table 3. Summary of efficiency and power loss

REGULATOR TYPE	MAXIMUM LOAD		NO LOAD
	EFFICIENCY (%)	POWER LOSS (W)	QUIESCENT CURRENT (mA)
Switching	84.5	0.093	0.5
Integrated Linear	20.0	2.06	5.5
Discrete Linear	20.1	2.02	4

linear circuit. (See Table 3.) It is interesting to note that the temperature rise of the integrated linear circuit is different from that of the discrete linear circuit. Since the integrated linear regulator's package (DDPak) is larger, its dissipated heat is spread over more area. The discrete linear circuit using the SOT-23 and SOT223 packages is smaller than the DDPak and has a higher package power-dissipation rating, which makes dissipating the heat more difficult.

Efficiency comparison

The thermal performance is directly related to the efficiency of each regulator. Figure 5 shows an efficiency comparison of all three circuits. As expected, the switching regulator excels at both light-load and full-load efficiency. At light loads, switching losses and quiescent-current losses become more pronounced, which explains the reduced efficiency at lighter loads. At light loads, it is better to view the power-loss graph (Figure 6) than the efficiency graph, since a 50% difference in efficiency at 10 mA seems like a large margin. However, the amount of current consumed by the load is small. When the input voltage is 24 V and the output current is 10 mA, the power loss of the switching regulator is 2.8 mW, and the loss of the integrated linear regulator is 345 mW. At full load, the measured power dissipated is 0.093 W for the switching regulator versus 2.06 W for the linear regulator, which shows a wide margin and a drastic improvement.

Table 3 summarizes the efficiency and power loss of all three circuits. Note that the quiescent current of the discrete linear circuit is lower than that of the integrated linear circuit. The integrated linear regulator has more power-consuming internal circuitry and incorporates more features than the discrete linear circuit.

Figure 5. Efficiency versus load current

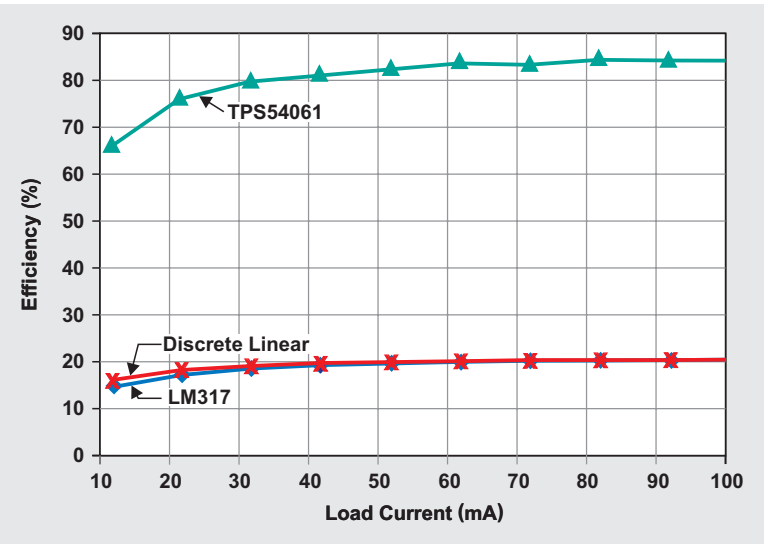
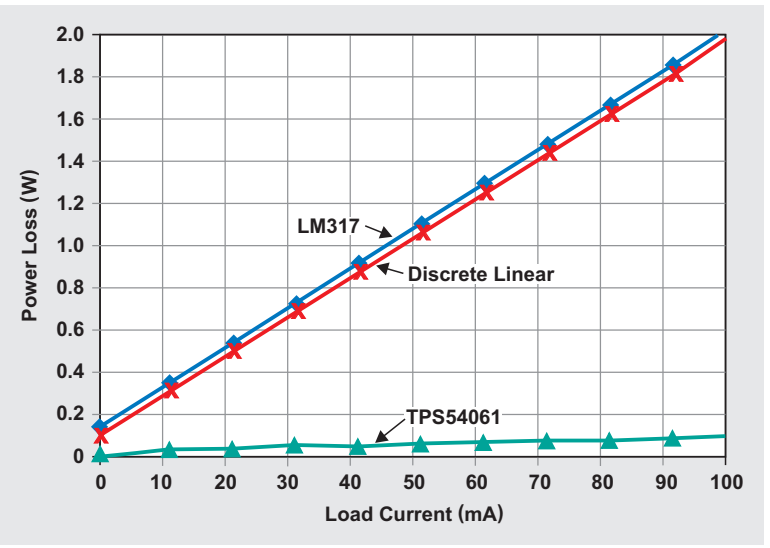


Figure 6. Power loss versus load current



Output-voltage characteristics

Analog circuits may be sensitive to voltage ripple, and digital processors may be sensitive to the accuracy of the core voltage. It is important to check the power supply's voltage ripple, voltage-regulation accuracy, and voltage-peak deviations during load transients. Linear regulators inherently have low ripple and are used to remove noise from switching regulators. The voltage ripple of both the integrated and the discrete linear-regulator circuits under maximum load is under 10 mV. When expressed as a percentage of the output voltage, accuracy is better than 0.2%. On the other hand, the voltage ripple of the switching regulator is 75 mV, or 1.5% of the output voltage. The low equivalent series resistance of the switching regulator's ceramic output capacitor allows for the circuit's low ripple, despite the switching regulator's inherent noise.

Comparing the output-voltage accuracy of the switching and linear regulators from no load to full load shows that the switching regulator has better performance. Further inspection of the product specification tables reveals that the reference voltage of the switching regulator is the most accurate of the three circuits. The switching regulator is a relatively new integrated circuit, and DC/DC converters are trending towards higher reference-voltage accuracies. The discrete linear circuit, which uses a simpler method for regulating the output voltage, has the worst performance. In many cases, applications do not need high voltage accuracy since the 5-V output may be postregulated.

The load-transient plots can be seen in Figures 7 through 9. Although the switching regulator has high output-voltage accuracy, its measured peak-to-peak voltage during a load transient is not as competitive as that of the linear circuits. The switching regulator's measured peak-to-peak voltage during a 50- to 100-mA load step is 250 mV, or 5% of the output voltage, compared to 40 mV for the linear circuits. Additional output capacitance can be added to the switching regulator to reduce the voltage peaks, but with penalties in cost and size. Note that the discrete linear circuit is not designed to attempt recovery of the output voltage during a load transient. Also, the simplicity of the circuit does not allow for current limiting or thermal-shutdown protection!

Figure 7. Switching regulator during load transient

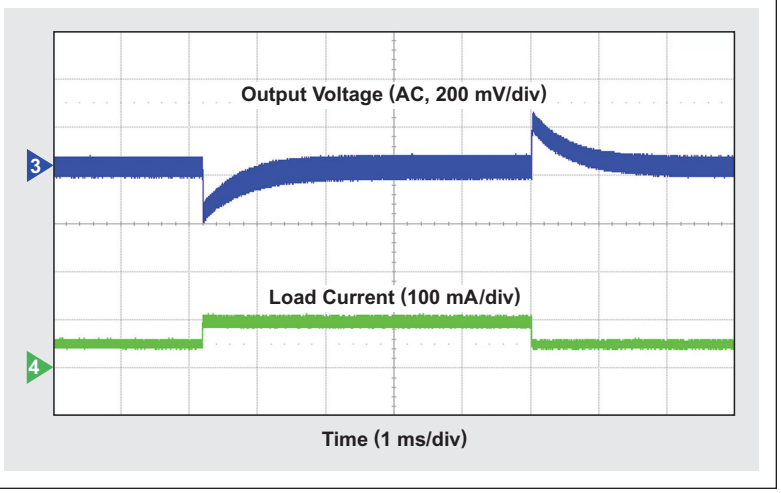


Figure 8. Integrated linear regulator during load transient

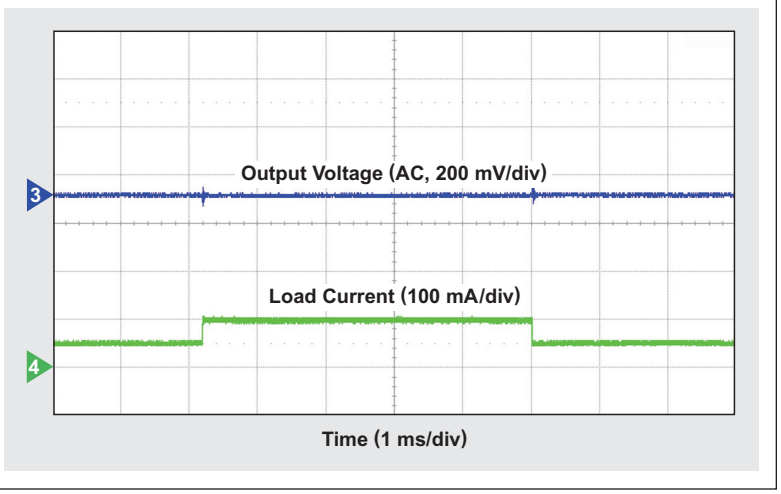


Figure 9. Discrete linear regulator during load transient

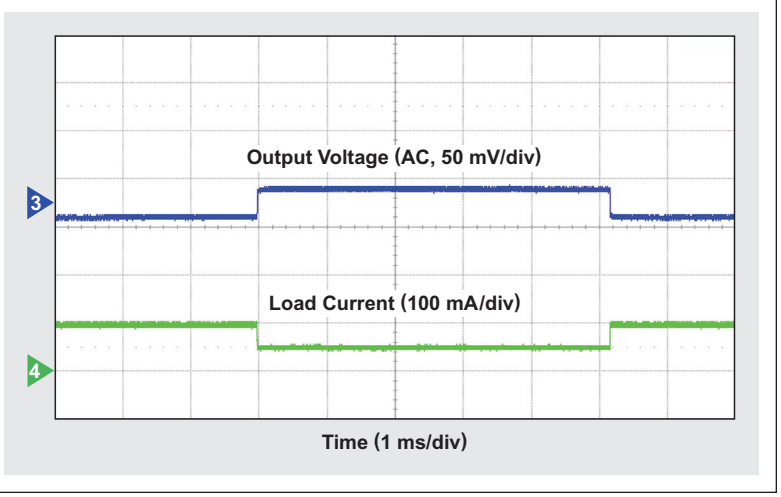


Table 4 summarizes the output-voltage characteristics of the three regulator designs.

Cost comparison

Most of the external components used in these circuits are small, passive resistors and capacitors that cost well below $0.01. The highest-cost component of the three circuits is the silicon. Costs for all three bills of materials (BOMs), shown in Table 5, were collected from U.S. distribution channels at 10,000-unit suggested resale pricing. As can be seen, both linear-regulator solutions cost much less than the switching regulator. Unfortunately, the switching regulator requires an external inductor, which can cost about $0.10; but the improvement in efficiency and size may be worth the additional cost. The cost difference between the integrated and discrete linear circuits is only $0.06! The protection features alone may prove the value of the integrated over the discrete linear regulator.

Conclusion

There are many power-management solutions available to designers, and the best solution depends on the particular needs of the application. Power-management solutions that reduce energy consumption and save board space allow designers to make their products more differentiated and attractive on the market. A synchronous buck converter offers drastic improvements in efficiency and board space compared to either linear circuit. If a design must have the absolute lowest cost, a discrete linear circuit can help, but the trade-off is worse performance with potential penalties, such as the additional cost of heat sinking and the lack of protection features.

Table 6 summarizes the characteristics of all three regulator designs to aid the designer in choosing the best solution for a given application.

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Table 4. Summary of output-voltage characteristics

REGULATOR TYPE	MAXIMUM LOAD RIPPLE (mV)	OUTPUT TRANSIENT WITH 50- TO 100-mA LOAD STEP (mV)	REGULATION ERROR WITH 0- TO 100-mA LOAD STEP (mV)
Switching	75	250	1.5
Integrated Linear	<10	40	0.7
Discrete Linear	<10	40	21.8

Table 5. Summary of BOM cost

REGULATOR TYPE	BOM COST AT 10-ku RESALE PRICE (U.S. DOLLARS)
Switching	1.80
Integrated Linear	0.32
Discrete Linear	0.26

Table 6. Characteristics of 5-V/100-mA regulators with a 24-V input

REGULATOR TYPE	BOM COST AT 10-ku RESALE PRICE (U.S. DOLLARS)	V_{OUT} RIPPLE (mV)	FULL-LOAD EFFICIENCY (%)	BOARD AREA (in^2)	COMPLEXITY
Switching	1.80	75	84.5	0.14	High
Integrated Linear	0.32	<10	20.0	2.25	Low
Discrete Linear	0.26	<10	20.1	2.25	Medium

Improved $LiFePO_4$ cell balancing in battery-backup systems with an Impedance Track™ fuel gauge

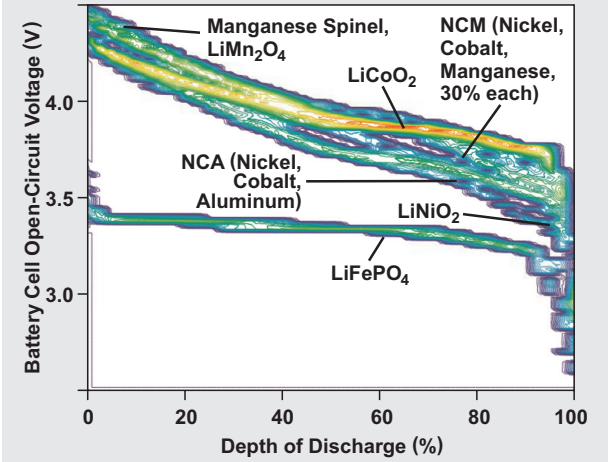
By Keith James Keller
Analog Field Applications

The Impedance Track™ battery-fuel-gauging technology from Texas Instruments (TI) is a proprietary algorithm that learns battery capacity and impedance over time to accurately calculate the state of charge (SOC) and remaining capacity.

There are special conditions that need to be understood when dealing with a battery-backup application where short charge periods occur every couple of days to replenish self-discharge, and a full discharge rarely occurs. When lithium-iron-phosphate ($LiFePO_4$) cells are used, either the gauge's balancing feature must be disabled or an enhanced firmware must be used. This article provides information about TI's specially developed firmware for the bq20z45-R1 gas gauge that allows data-flash parameters to be programmed for proper battery cycling and the best balancing results. Guidelines are also provided for accomplishing off-line cell balancing when balancing has been disabled for normal operation.

Figure 1 shows a voltage-density plot of single-cell, open-circuit voltage (OCV) versus depth of discharge (DOD) for all lithium-based cells that TI has analyzed over a period of approximately ten years. (DOD is simply 1/SOC.) One can see that the voltage profile of the $LiFePO_4$ cells is very flat for a significant portion of the SOC curve. This voltage flatness leads to difficulty in the precise SOC estimation required for cell balancing with the Impedance Track algorithm. The steep voltage increase visible at the end of charge (approximately 0% DOD) can lead to significant cell-to-cell voltage divergence, further complicating SOC estimation and cell balancing.

Figure 1. Map of voltage densities for lithium-based battery cells



Eliminating Q_{max} updates during operation

It is permissible not to have a Q_{max} update during field operation. Although not required, the ideal situation for a highly reliable battery-backup application is for the pack's Q_{max} to be determined with a full discharge during the manufacturing process. After Q_{max} is learned, no further Q_{max} update is required.

Events for determining initial Q_{max}

Table 1 shows typical enhanced data-flash parameters of the bq20z45-R1 with version 7.02 firmware that must be modified via TI's bq Evaluation Software tool to implement a Q_{max} update. These particular parameters are protected (classified as "hidden") but can be unlocked by TI's applications staff. Battery parameters in Table 1 are from the TI database for a 2-series, 2-parallel (2s2p),

Table 1. Protected data-flash parameters that TI's applications staff can unlock based on system characteristics

DATA-FLASH PARAMETER	DEFAULT VALUE	NEW VALUE
Operation Cfg C	0130	05B0
Min % Passed Charge for Q_{max}	37%	No Change
Min % Passed Charge for 1st Q_{max}	90%	No Change
Q Invalid MaxV	3351 mV (chemical ID 404 default)	No Change
Q Invalid MinV	3274 mV (chemical ID 404 default)	No Change
OCV Wait Time	1800 seconds	600 seconds
Max Delta V	40 (10-µV units)	160 (10-µV units)
DOD Capacity Err	2%	No Change
Q_{max} Max Time	18,000 seconds	No Change
Max Capacity Error	1.0%	3.0%
Q_{max} Filter	96	26
Q Invalid MaxT	40.0°C	55.0°C
Q Invalid MinT	10.0°C	No Change
Min Cell Deviation	1750 s/mAh	1909 s/mAh

2500-mAh $LiFePO_4$ battery pack with chemical ID 404. The table also shows the changes that must be made to the data-flash parameters based on these characteristics. The "Operation Cfg C" register change enables the new features provided by the 7.02 firmware. The changes to "OCV Wait Time" and "Max Delta V" allow for the OCV measurements to occur immediately after the charge is complete. The changes to "Max Capacity Error" and "Q_{max} Filter" allow additional time for the Q_{max} update to happen with smaller-capacity batteries (since $LiFePO_4$ cells generally have only 1100-mAh cells in an 18650 size).

Once the default values have been changed, a good Q_{max} update can be achieved with the approach that will now be described.

1. Start of Q_{max} update cycle

A Q_{max} update cycle should start when the battery has rested after a full charge. Ideally the cells should relax as long as possible. However, if the pack has a high self-discharge current because of onboard circuitry, this waiting time could be as short as two hours.

2. Full charge and valid OCV learning

When the charge terminates, the IT enable command (0x0021) must be sent to prevent OCV learning from occurring before the cell voltages have stabilized. The cells then should be allowed to relax as long as possible. $LiFePO_4$ packs have a tendency for one cell's voltage to run away at the end of charge during taper conditions. This runaway can be prevented by charging to a lower voltage (3.5 V per cell) or disabling the charger after one cell's voltage skews beyond 20 mV higher or lower than any other cell.

For chemical ID 404, if the lowest cell voltage in the battery stack is 3353 mV or more after the cells rest, the discharge procedure that follows can be started. If any cell voltage drops below 3353 mV while resting, another charge cycle is required to top off the battery, and the process must be started again. Different voltages apply to different chemical IDs. See Reference 1 and "Related Web sites" at the end of this article for more information.

The IT enable command is again sent to begin the Q_{max} update process. After this command is sent, there should be a five-minute wait before discharge begins, for two reasons: (1) to clear out the coulomb counter's digital filter, which is integrated over five minutes; and (2) to allow the fuel gauge some time for calculations after the enable command is sent.

3. Discharge and rest

The battery should be discharged to empty or to sufficiently below its minimum disqualification voltage. As the cells relax, their voltages increase. All cell voltages must remain under the minimum disqualification voltage during the entire rest time specified by the "Q_{max} Max Time" setting, plus an additional five-minute buffer.

4. Completion of Q_{max} update

The updated Q_{max} values can be read from data-flash "state" offset 82/Q_{max} cell offset 0–8. If Q_{max} is not learned or updated, then the update cycle should be restarted so that the battery is again charged to full capacity, the appropriate commands are issued, and the battery is allowed to rest.

The golden cycle

To create the golden-image data for any battery pack, several charge and discharge cycles should be run to obtain reliable Q_{max} and resistance-table (Ra-table) values. With $LiFePO_4$ cells, it is preferable for Q_{max} to be learned on a discharge cycle following the process outlined previously.

It is important to create a log file (.LOG) with the bq Evaluation Software tool during both the charge and the discharge cycles of the golden cycle. This allows the values for Q_{max} and the Ra table to be verified by a Mathcad® calculation tool provided by TI's applications staff.

When the golden gas gauge (.GG) file is created, conservative numbers based on cycling data should be assigned to the Q_{max} values. The assigned set of Ra-table values should be the same for each cell, and the Q_{max} values should be the same for parallel cells. Using nonsymmetrical Q_{max} and Ra-table starting values with continuous cycling could cause an SOC error and balancing issues. Table 2 shows an example of adjusted golden .GG values that can improve cell balancing in a 2s2p pack configuration.

Table 2. Example of learned data-flash parameters compared to those used in golden .GG file

Example Learned .GG Parameters for 2s2p Configuration with 2500-mAh Capacity (not comprehensive)	Values Used in a Golden .GG File
[Cell Balancing Cfg (Charge Control)]	[Cell Balancing Cfg (Charge Control)]
FC-MTO = 32400	FC-MTO = 0
[State(Gas Gauging)]	[State(Gas Gauging)]
Qmax Cell 0 = 2583	Qmax Cell 0 = 2510
Qmax Cell 1 = 2510	Qmax Cell 1 = 2510
Qmax Cell 2 = 2500 (not used)	Qmax Cell 2 = 2500 (not used)
Qmax Cell 3 = 2500 (not used)	Qmax Cell 3 = 2500 (not used)
Qmax Pack = 2583	Qmax Pack = 2510
Update Status = 06	Update Status = 02
[R_a0(Ra Table)]	[R_a0(Ra Table)]
Cell0 R_a flag = 0000	Cell0 R_a flag = 0055
Cell0 R_a 0 = 34	Cell0 R_a 0 = 34
Cell0 R_a 1 = 37	Cell0 R_a 1 = 37
Cell0 R_a 2 = 49	Cell0 R_a 2 = 49
Cell0 R_a 3 = 59	Cell0 R_a 3 = 59
Cell0 R_a 4 = 54	Cell0 R_a 4 = 54
Cell0 R_a 5 = 60	Cell0 R_a 5 = 60
Cell0 R_a 6 = 73	Cell0 R_a 6 = 73
Cell0 R_a 7 = 67	Cell0 R_a 7 = 67
Cell0 R_a 8 = 73	Cell0 R_a 8 = 73
Cell0 R_a 9 = 81	Cell0 R_a 9 = 81

(Continued on next page)

When the golden-image data is being created and during normal operation, the gas gauge's charge time-out feature, FC-MTO, should be disabled (set to 0) so that the battery can continuously be topped off without requiring a discharge to clear this timer. FC-MTO is hidden in TI's bq20z4x/7x products, but fortunately it is already set to zero by default. The feature is called "FC-MTO" for TI's bq20z80 and "CMTO" for TI's bq20z6x/9x.

Cell balancing

For 3s or 4s cells, only internal cell balancing should be used in a battery-backup application. This is because adjacent cells cannot be balanced properly with external cell balancing. However, it is permissible to use external cell balancing in a 2s pack. Since a backup battery spends most of its time at rest and much less time in charging, adjacent cells need to be balanced correctly.[2]

As discussed earlier, the enhanced bq20z45-R1 firmware's data-flash parameters must be modified for a battery-backup application and for the designer's particular pack characteristics (chemical ID 404 in this article). The enhanced firmware offers a weighted measurement of OCV values throughout the rest period and locks the cell-balancing calculation immediately after the first OCV measurement is taken after the charge is complete. It also disables cell balancing in the disqualified range after power-up or a reset condition.

Periodic discharges to learn Ra-table values is recommended. Updates of these values happen with approximately every 11% change in SOC during discharge (89%, 78%, 67%, etc.).

Additionally, loss in cell capacity over time can be estimated and compensated for by using the reserve-capacity feature of the gas gauge. Another option to compensate for capacity loss is to have the host system calculate it. If the system is to be operated with no Q_{max} update, then the host controller must make sure that a Q_{max} update does not occur by issuing the IT enable command (0x0021) after a charge is complete.

Off-line cell balancing without enhanced firmware

TI's bq20z6x/7x/8x/9x devices do not offer the enhanced firmware for $LiFePO_4$ cells. If these devices are used in a standby application, the balancing must be disabled during normal operation. This is accomplished by setting the minimum cell deviation to zero. If the host system determines that cells are misbalanced over time, the following steps should be taken:

1. Cell balancing should be enabled by setting the minimum cell deviation to 1909 (or whatever the appropriate value is as calculated in Reference 2).

Steps 2 through 6 should be used in conjunction with the events and conditions given earlier to ensure a valid Q_{max} update.

Table 2 (Continued from previous page)

Example Learned .GG Parameters for 2s2p Configuration with 2500-mAh Capacity (not comprehensive)	Values Used in a Golden .GG File
Cell0 R_a 10 = 85	Cell0 R_a 10 = 85
Cell0 R_a 11 = 94	Cell0 R_a 11 = 94
Cell0 R_a 12 = 93	Cell0 R_a 12 = 93
Cell0 R_a 13 = 204	Cell0 R_a 13 = 204
Cell0 R_a 14 = 304	Cell0 R_a 14 = 304
[R_a1(Ra Table)]	[R_a1(Ra Table)]
Cell1 R_a flag = 0055	Cell1 R_a flag = 0055
Cell1 R_a 0 = 137	Cell1 R_a 0 = 34
Cell1 R_a 1 = 144	Cell1 R_a 1 = 37
Cell1 R_a 2 = 165	Cell1 R_a 2 = 49
Cell1 R_a 3 = 178	Cell1 R_a 3 = 59
Cell1 R_a 4 = 168	Cell1 R_a 4 = 54
Cell1 R_a 5 = 180	Cell1 R_a 5 = 60
Cell1 R_a 6 = 211	Cell1 R_a 6 = 73
Cell1 R_a 7 = 210	Cell1 R_a 7 = 67
Cell1 R_a 8 = 223	Cell1 R_a 8 = 73
Cell1 R_a 9 = 241	Cell1 R_a 9 = 81
Cell1 R_a 10 = 257	Cell1 R_a 10 = 85
Cell1 R_a 11 = 287	Cell1 R_a 11 = 94
Cell1 R_a 12 = 322	Cell1 R_a 12 = 93
Cell1 R_a 13 = 650	Cell1 R_a 13 = 204
Cell1 R_a 14 = 962	Cell1 R_a 14 = 304

2. The battery should be discharged to empty and the cells allowed to relax for five hours and five minutes (or five minutes past the setting for "Q_{max} Max Time"). Once this relaxation occurs at empty, a good SOC estimation can be made from the voltage measurement of each cell.
3. The battery should be charged to full to allow cell balancing to occur throughout the entire charge cycle.
4. After charging is complete, the host system should send an IT enable command, read the cell voltages, and determine whether another deep-discharge balancing cycle and rest are required.
5. If an additional balancing cycle is required, the discharge to empty can be begun right away. Another rest period of five hours and five minutes is required at empty as before.
6. After the cells have been determined to be properly balanced, the minimum cell deviation should be set back to zero to disable cell balancing.

Conclusion

TI's Impedance Track battery-fuel-gauging technology is an adaptive gauging algorithm that can provide considerable

SOC accuracy over the life of a battery. However, in battery-backup applications, there are several things to consider and change for the best possible operation. This article has discussed using TI's enhanced bq20z45-R1 firmware with $LiFePO_4$ cells to achieve proper cell balancing and to obtain reliable Q_{max} updates for the best possible accuracy.

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2. Simon Wen, "Fast cell balancing using external MOSFET," Application Report. Available: www.ti.com/slua420-aaj
3. "Theory and implementation of Impedance Track™ battery fuel-gauging algorithm in bq20zxx product family," Application Report. Available: www.ti.com/slua364-aaj
4. Keith James Keller, "Fuel-gauging considerations in battery backup storage systems," *Analog Applications Journal* (1Q, 2010). Available: www.ti.com/slyt364-aaj

Related Web sites

Power Management:
www.ti.com/power-aaj

www.ti.com/bq20z45-r1-aaj
www.ti.com/bq20z70-v160-aaj
www.ti.com/bq20z80a-v110-aaj
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Basics of debugging the controller area network (CAN) physical layer

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Introduction

The controller area network (CAN) standard continues to grow and is being adapted into many new applications outside of automotive and industrial networking. Microprocessors supporting it have become prevalent at low cost, and open-source protocol stacks make it very accessible and easy to add to new systems. There are CAN boards for BeagleBone (Capes), Stellaris® (BoosterPacks), Arduino (Shields), and many other microprocessor development platforms. When a designer's system is powered up and doesn't work, then what? This article presents a sound engineering approach to debugging the CAN physical layer. Basic debugging steps are provided, along with discussion of the expected behavior of a CAN physical layer and tips to help pinpoint the trouble.

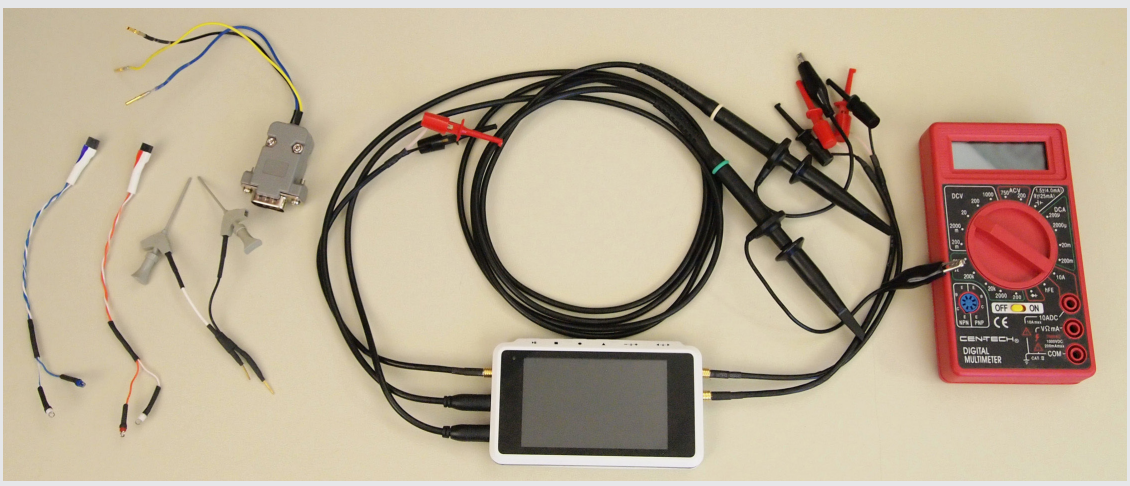
Debugging basics

The ISO11898-2 and ISO11898-5 specifications provide details for the high-speed CAN physical layer or transceiver. With a fundamental knowledge of the CAN physical layer, common problems can be found quickly by using simple debugging tools. The basic lab tools needed are an oscilloscope, a digital multimeter (DMM), and a power supply. If the investigation leads to detailed problems, higher accuracy and more complex tools may be required. Problems at that level are outside the scope of this article, but the basics introduced here will help identify areas of concern and what additional tools will be required for further debugging. A CAN demonstration system assembled by Texas Instruments (TI) and TI's SN65HVD255D evaluation module (EVM)[1] are used for the demonstration hardware. A few other helpful items are also used, such as a CAN connector breakout cable and chip hooks to grab the transceiver pins and bring them to a cable for easy attachment to an oscilloscope probe (Figure 1).

Checking the connections

To begin the debugging session, a DMM is used to make sure the connections on the printed circuit board (PCB) are as expected—while the system is *unpowered*. This seems very basic, but it is amazing how many simple problems have been solved with this technique. Everyone assumes that the schematics, layout, and manufacturing are correct, but unfortunately sometimes they aren't. Improperly seated daughtercards, cold solder joints, and cables not terminated or connected properly are all common issues. The resistance setting of the DMM is used to

Figure 1. Basic tools for debugging the CAN physical layer



make sure all the traces and connections are properly made. A simplified schematic for a CAN application is shown for reference in Figure 2.

The PCB and network connections to check are summarized in Table 1. The expected resistance between the pins on the transceiver and the relevant other connections on the PCB is 0 Ω, unless the design uses some of the options outlined in the table comments. Examples include current-limiting series resistors, bus-termination resistors, or pull-up or pull-down resistors on digital I/Os.

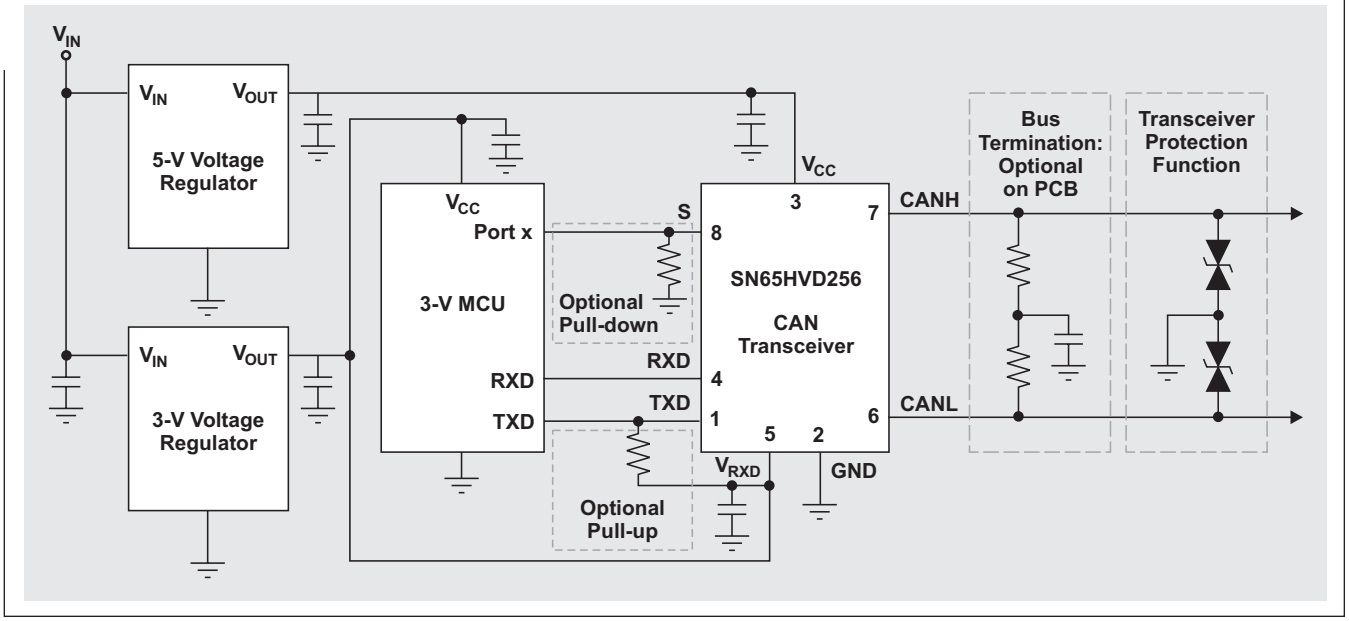
Checking bus termination

Most CAN standards specify a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Termination may be a

Table 1. Summary of PCB and CAN transceiver connections

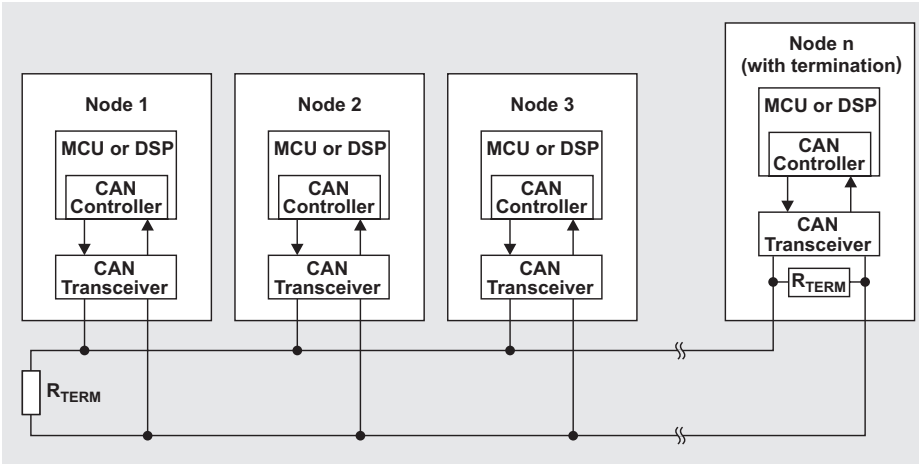
CONNECTION	COMMENTS
Ground	The transceiver GND should be connected to the PCB ground plane.
Power Supply (V_{CC}, V_{IO}, V_{RXD})	The V_{CC} on the transceiver should be connected to the voltage regulator's output. One should be careful in multirail designs: The V_{CC} of the transceiver may be 5 V or 3.3 V, depending on the CAN transceiver family. Some 5-V CAN transceivers have an I/O level-shifting pin (V_{IO} or V_{RXD}).
Transmit Data (TXD or D)	If a current-limiting series resistor is used, that is the expected resistance value. The TXD may need a pull-up to the V_{CC} if an open-drain output on a microprocessor is used.
Receive Data (RXD or R)	If a current-limiting series resistor is used, that is the expected resistance value.
Mode	R_S, S, STB, EN, AB, or LBK may be available, depending on the specific CAN transceiver. R_S provides three modes of operation that need to be checked: 1. *High-speed mode.* There should be a connection to ground or low from the microprocessor's output pin. 2. *Slope-control mode.* There should be a pull-down resistor to ground between 10 and 100 kW. 3. *Low-power mode.* There should be a logic high via a pull-up resistor or via the output from the microprocessor's output pin. The other pins are digital inputs with logic-low and -high thresholds that may be either driven by a microprocessor output or pulled high or low via a resistor. It should be verified that the device is in the proper mode.
V_{REF} or SPLIT pin	Some transceivers may have a $V_{CC}/2$ output reference. It may be floating, connected by a bypass capacitor to ground, or used to actively drive split termination. The application use should be verified.
CAN Bus (CANH, CANL)	The transceiver's CANH and CANL pins should be connected to the respective pins on the CAN bus. More information is provided under "Checking bus termination" in this article.

Figure 2. Simplified schematic for a CAN application



single 120-Ω resistor at the end of the bus on the cable, as shown on the left side of the CAN bus in Figure 3; or it may be in a terminating node, as shown on the right side of Figure 3. The termination resistance should not be removed from the bus. If the resistive load of the CAN termination is not present, signal integrity will be compromised and the bit timing will not be met. If filtering and stabilization of the bus's common-mode voltage is desired, split termination may be used as in Figure 2. In this figure, each resistor is 60 Ω, and the split capacitor may be anywhere from 1 nF to 100 nF, depending on the frequency desired for the common-mode filter.[2] The measured resistance from CANH to CANL should be between 45 and 65 Ω to account for the tolerances within the CAN standard, the parallel impedance of the two termination resistors, and the input resistance of many nodes in parallel. The power rating of the termination resistors should be sized according to the worst-case fault conditions they may encounter, usually the power-supply voltage of the system to ground.

Figure 3. Typical CAN bus



Checking the power supply

Before the system is powered up, the power supply (or supplies) to the CAN transceiver should first be checked. The V_{CC} should be powered with 3.3 V or 5 V, depending on the transceiver type used. Believe it or not, there have been several cases where a missing V_{CC} was the root cause of the problem. Therefore, it should be ensured that the V_{CC} is present at the transceiver's V_{CC} pin. A simple check with a DMM will confirm that power supplies are present. Care must be taken not to short the supply to ground, which unfortunately is a pin next to the V_{CC} pin.

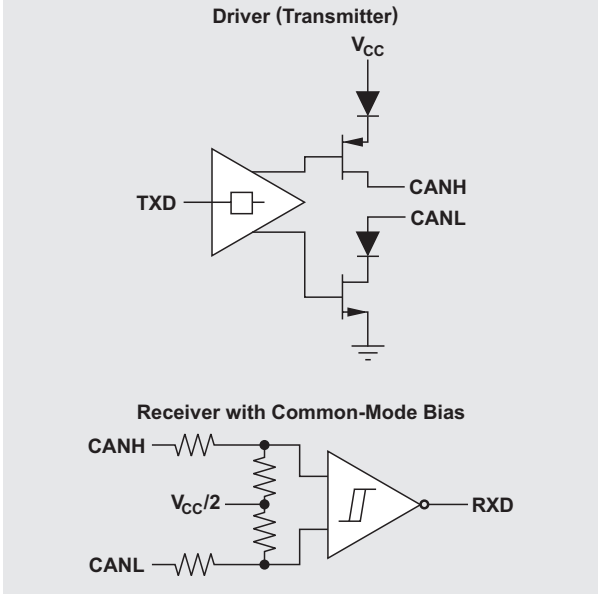
There is approximately a 50-mA difference in current (I_{CC}) needed between the dominant state (~60 mA with a 60-Ω bus load) and the recessive state (10 mA). This 50-mA difference is needed to generate the differential voltage across the termination resistance during the dominant bus state and varies with bus loading. The DMM also may be used in current mode to verify the expected I_{CC} supply currents. Due to the switching nature of CAN, current measured with a DMM is a pseudo-average reading.

A local bypass capacitor of at least 4.7 µF is recommended to ensure adequate supply buffering during the bus-state transitions. Otherwise, there may be significant voltage-supply ripple caused by the inrush current of the transceiver. An oscilloscope can be used to verify whether the supply voltage is stable or varying with the bus state. It would be undesirable to "starve" the transceiver during the transitions. The transceiver will be protected by its current limiting, but the supply current will be significantly higher if one of the bus lines is shorted to a supply or ground when the transceiver is trying to drive the bus to a dominant state. If the voltage regulator cannot supply that amount of current, the voltage level may drop out of the transceiver's specification range, or may even be low enough to trip an undervoltage lockout condition on the transceiver.

CAN physical-layer basics

Once all the basics have been checked, the heart of the CAN physical layer—the CAN bus—can be examined. The transceiver's two key components are the receiver and the transmitter. The transmitter is normally called the driver in a CAN. The CAN physical layer is biased with a common-mode point of $V_{CC}/2$, or approximately 2.5 V (Figure 4).

Figure 4. Simplified CAN bus transceiver



The transceiver translates the single-ended digital logic signals, TXD (or D) and RXD (or R), to the levels required by the differential CAN bus. When the bus is dominant, it has a differential voltage ($V_{diff(D)}$) defined by the CAN standard of >1.2 V at the receiving nodes and is in a logic-low state. When the bus is recessive, it has a differential voltage ($V_{diff(R)}$) defined by the CAN standard of –120 mV ≤ ($V_{diff(R)}$) ≤ 12 mV at the receiving nodes and is in a logic-high state. Both of these bus states are biased via the common-mode network in the transceiver. The typical bus levels are shown in Figure 5.

To debug the bus, one of the most useful tools is an oscilloscope. While a single-channel scope allows the signals to be seen, a dual- or quad-channel scope is the best. Ideally, TXD, RXD, CANH, and CANL can be seen at the same time to ensure that the transceiver and bus are behaving as expected with respect to each other. For the initial debugging, a low-bandwidth scope is all that is needed, since the CAN is limited to 1 Mbps in the standard. (In the near future this may change, with the introduction of a CAN with flexible data rates.) If the node is transmitting the bitstream of data, the input data can be seen on the TXD input. There is a propagation delay to the differential CAN bus pins (CANH/CANL), followed by another propagation delay to the RXD output. These delays are the loop time, or loop delay, in a CAN. If the node is receiving, then TXD will be idle; but the bus and RXD output will show the CAN frame.

To demonstrate basic CAN-bus operation, Figure 6 shows an oscilloscope with two analog channels and two digital channels, plus a function generator. The CAN bus is made up of two SN65HVD255D EVMs, each with 120-Ω termination set on the bus. The function generator from the scope is connected to the TXD input pin of the top EVM. In Figure 7, digital channel 1 shows the TXD input (light purple); analog channel 1 shows the CANH signal (blue); analog channel 2 shows the CANL signal (yellow); and digital channel 2 shows the RXD signal (green). While

Figure 5. CAN bus states

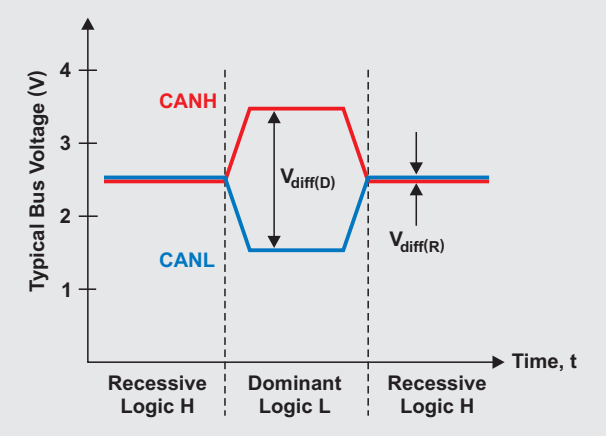


Figure 6. Debugging on a CAN bus of two EVMs

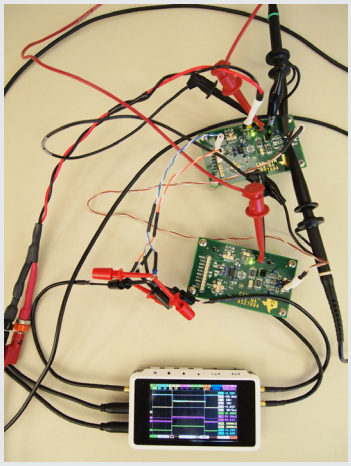
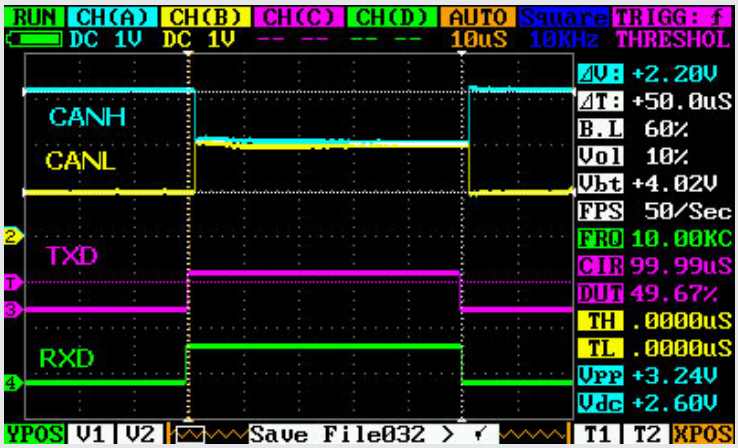


Figure 7. TI CAN EVM signals



the accuracy of this scope is very low, it appears from this simple test that in general the CAN physical layer is behaving as expected.

Figure 8 shows the oscilloscope and probe set up to debug on the TI CAN demonstration system. The nodes are set up in a daisy chain that uses CANopen® D-SUB 9-pin connectors. A bus breakout connector is in the upper left portion of Figure 8. It is used to easily connect the analog scope probes to the CANH and CANL pins of the CAN bus and to GND. Because the probes are too large to grab the TXD and RXD IC pins of the middle CAN node, these pins are connected to the digital channels of the scope with chip hooks and a short cable going to the probes. Another option is to solder a small wire to each transceiver pin so the scope probe may be more easily attached.

Figure 9 shows the CAN signals in more detail as captured by the scope. While these signals are not high in resolution or accuracy, they help determine what needs to be known about the operating CAN nodes. The scope was triggered on TXD of the middle node; the CANH and CANL signals are differential as expected; and the acknowledge (ACK) bit with the higher differential voltage is clearly visible at the end of the CAN frame. This higher voltage is the result of multiple CAN nodes generating this ACK bit at the same time in parallel. Another way to easily identify the ACK bit is that it is visible in the RXD signal but not in the TXD signal, which means it was generated by the other nodes as it should be.

CAN debugging examples

Figure 10 shows a CAN demonstration system where the CANH trace leading to the daisy-chain output has been broken on the righthand PCB. This occurred because a mounting bolt on the rear of this system had rubbed against the PCB while the system was being carried around the world over a number of years. When this system was connected to other CAN nodes via this daisy-chain bus connection, it didn't work.

Figure 8. Debugging on the TI CAN demonstration system

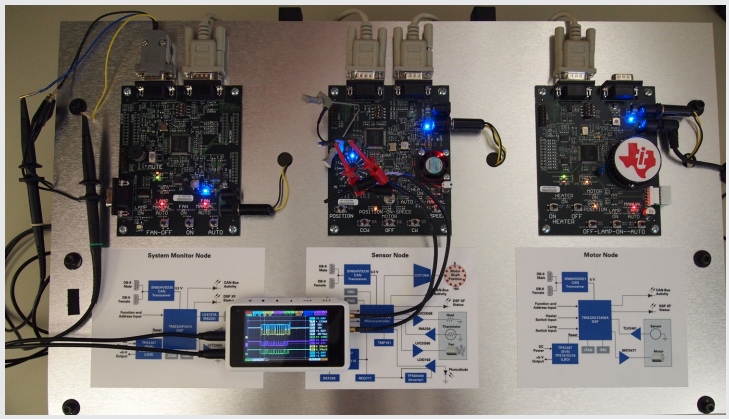
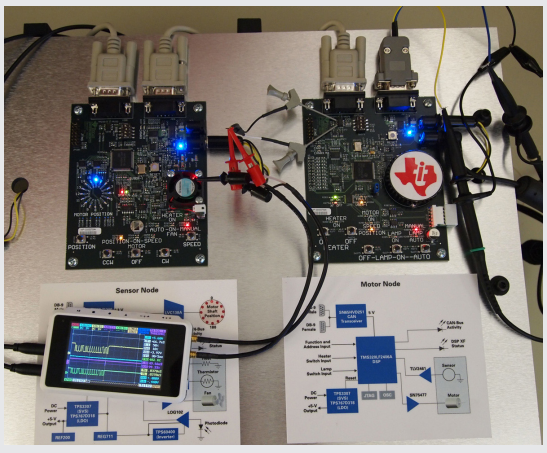


Figure 9. TI CAN demonstration system's signals

Figure 10. CAN demonstration system with broken CANH trace



The CANH signal in Figure 11 shows the result of this broken PCB trace. A DMM continuity check also confirmed the open circuit.

Figure 11 also highlights in detail another important part of the CAN frame, the ACK bit. The scope was used in single mode and triggered on the TXD pin of the right-hand node until a trigger on a single bit was found. This single bit is the ACK bit generated by this node to acknowledge that a valid CAN frame was received. All receiving nodes acknowledge the CAN frame from the sending node. The ACK bit seen on the bus has a slightly longer bit time than the transmitted ACK bit seen on TXD. This is an artifact of the multiple nodes transmitting ACK bits at the same time. Factors affecting this longer bit time are a 5-ns/m delay through the cabling; clock timing drift between the three CAN nodes; and the higher bus differential voltage resulting from two nodes transmitting an ACK bit concurrently. If these factors cause the ACK bit (slot) to become too long and to remain dominant in the ACK delimiter, it may cause a CAN error frame.

Another example of CAN bus debugging was a system where only very slow CAN data rates (bit timings) would work. Connecting an oscilloscope to the TXD pin showed very slow rise times on the TXD input (Figure 12). The 9.6-µs timing delay was equivalent to 10 bits at a CAN data rate of 1 Mbps. This discovery led to the root cause: A microprocessor with an open drain was being used to drive the transceiver's TXD pin. In this case there was no real drive to the logic-high level. Only the weak internal pull-up of the CAN transceiver was bringing the TXD pin high, so it had a very long RC time constant. This problem was easily solved by adding a pull-up resistor on the TXD pin.

Figure 11. TI CAN signals with broken CANH trace on PCB

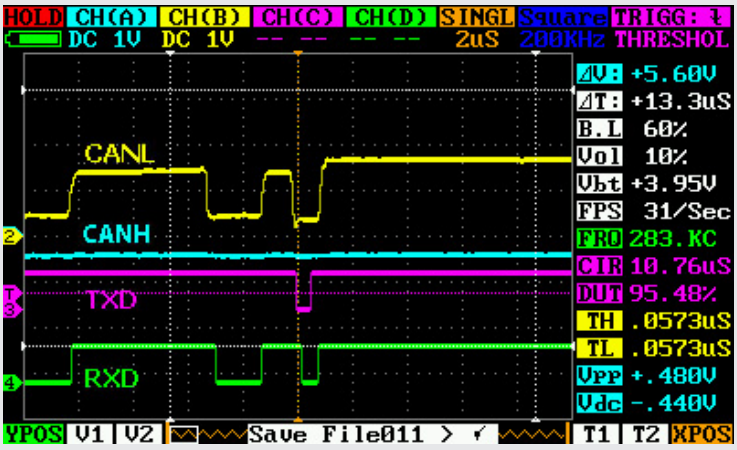
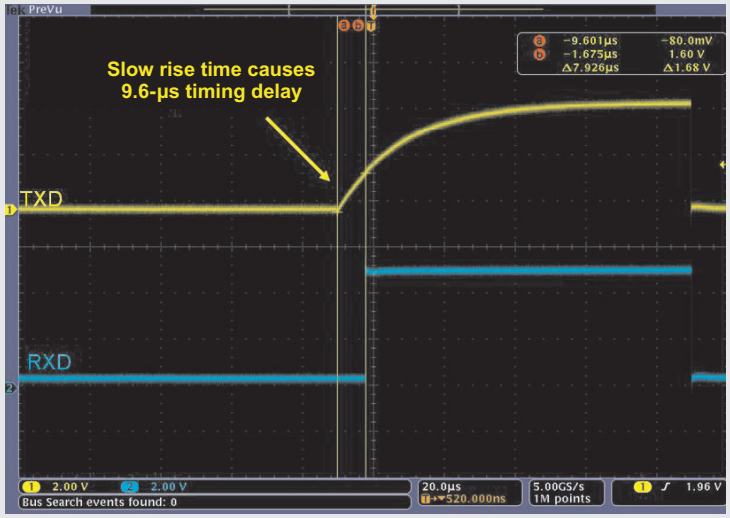


Figure 12. Example with slow rise time on TXD pin



Conclusion

The basics of the CAN physical layer and the debugging examples presented in this article should ease any fear of jumping into the CAN world. With the additional references provided here and the appropriate datasheets, designers should have their CAN systems up and running in no time.

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Exploring anti-aliasing filters in signal conditioners for mixed-signal, multimodal sensor conditioning

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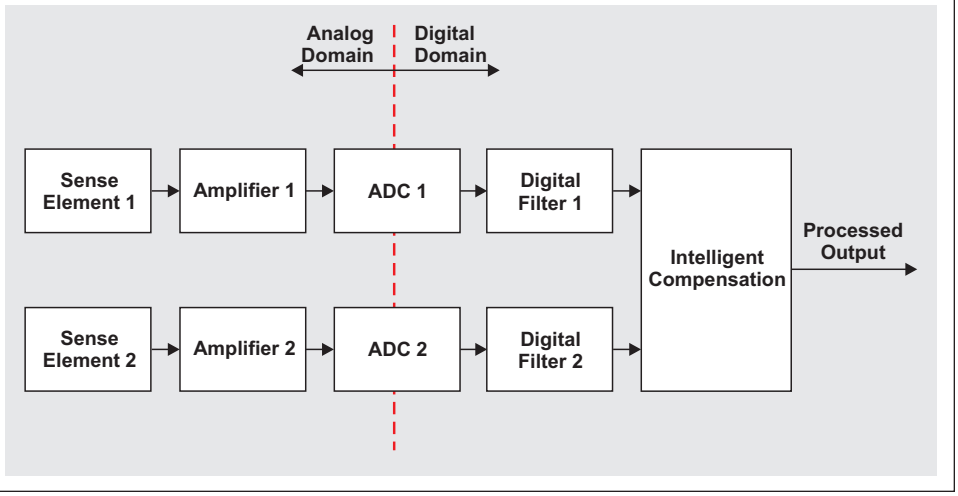
Systems Architect, Enhanced Industrial

Introduction

Some sensor-signal conditioners are used to process the output of multiple sense elements. This processing is often provided by multimodal, mixed-signal conditioners that can handle the outputs from several sense elements at the same time. This article analyzes the operation of anti-aliasing filters in such sensor-signal conditioners.

Figure 1. Multimodal, mixed-signal sensor-signal conditioner



Basics of sensor-signal conditioners

Sense elements, or transducers, convert a physical quantity of interest into electrical signals. Examples include piezoresistive bridges used to measure pressure, piezoelectric transducers used to detect ultrasonic waves, and electrochemical cells used to measure gas concentrations. The electrical signals produced by sense elements are small and exhibit nonidealities, such as temperature drifts and nonlinear transfer functions.

Sensor analog front ends such as the Texas Instruments (TI) LMP91000 and sensor-signal conditioners such as TI's PGA400/450 are used to amplify the small signals produced by sense elements into usable levels. The PGA400/450 include complete signal-conditioning circuits as well as circuits that generate stimuli for sense elements, manage power, and interface with the external controllers. Furthermore, devices such as the PGA400 provide the ability to correct for the nonidealities of the sense elements.

Multimodal signal conditioning

Often, for the purpose of signal conditioning or higher-level monitoring, there is a need to measure outputs of more than one sense element. For example, processing the output of a typically piezoresistive bridge requires measuring the outputs of both the bridge and a temperature sensor. Similarly, processing the output of a thermocouple requires measuring the outputs of both the thermocouple and a sensor that measures the connector temperature. The connector temperature is measured in order to perform cold-junction compensation. The scenario where more than one sense element is processed by the same signal conditioner is called *multimodal signal conditioning*.

Mixed-signal signal conditioning

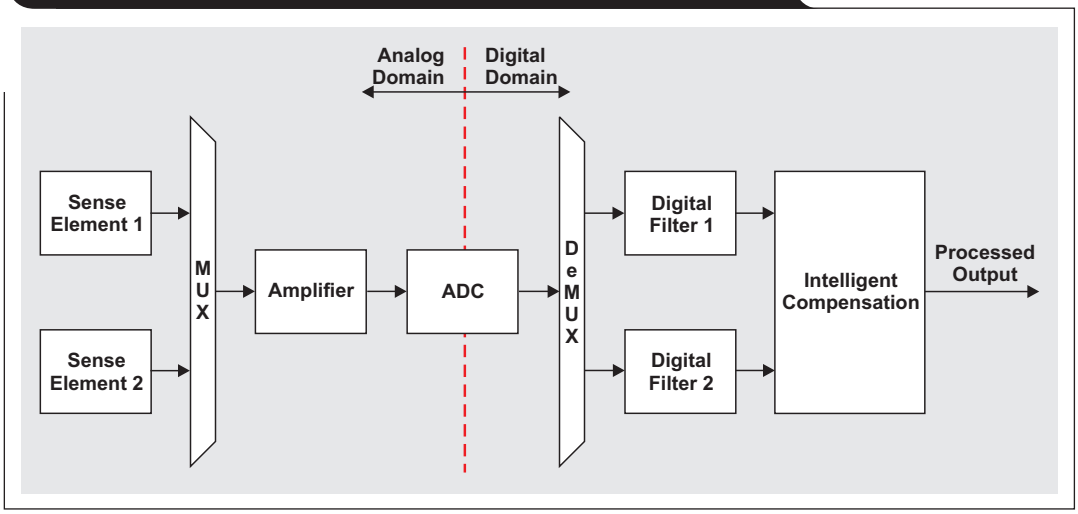
Another aspect of sensor-signal conditioning is the electrical domain in which the signal conditioning occurs. TI's PGA309 is an example of a device where the signal conditioning of resistive-bridge sense elements occurs in the analog domain. In devices such as the PGA400, the signal conditioning occurs in both the analog and the digital domains. The latter scenario is called *mixed-signal signal conditioning*.

A critical component of mixed-signal conditioners is the analog-to-digital converter (ADC). Figure 1 shows a block diagram of a multimodal, mixed-signal sensor-signal conditioner. This figure shows that the two sense elements have independent signal paths until the signals reach the intelligent compensation block. This block then combines the two signals to produce the processed output.

Nyquist criterion

A key aspect of mixed-signal sensor-signal conditioning is the discretization of the continuous-time analog-domain signal into a discrete-time digital-domain signal. In other words, mixed-signal conditioners are sampled systems. Hence, the well-known Nyquist criterion of sampling is applicable to mixed-signal sensor-signal conditioning. This

Figure 2. Analog signal paths sharing an amplifier and an ADC



criterion simply states that the sampling frequency has to be double the signal bandwidth of interest. For Figure 1 it is assumed that the amplifiers in each signal path limit the bandwidth of the signal in order to satisfy the Nyquist criterion. In other words, the amplifiers amplify the signals while at the same time providing the necessary anti-aliasing, or limiting of bandwidth, to satisfy the criterion.

Figure 1 also shows digital filters in the signal paths. The digital filters are used to reduce the signal bandwidths further to help improve the system's signal-to-noise ratio (SNR).

Unwanted sinusoid signals

For some applications, it may be desirable to reduce the cost of the circuit shown in Figure 1. Figure 2 shows a more cost-effective example wherein the two analog signal paths share an amplifier and an ADC. The signal paths in either circuit could have out-of-band sinusoid components introduced into either the sense element (for example, due to electromagnetic interference) or the signal path itself (for example, due to interference from adjacent circuits). Because of the common signal path in Figure 2, the digital filters may not be effective in eliminating out-of-band or unwanted sinusoid components. This section analyzes this problem.

For this analysis it is assumed that the circuits in Figures 1 and 2 share the same conditions:

- ADC sampling rate: 10 kHz
- Amplifier bandwidth to satisfy Nyquist criterion: 5 kHz
- Signal band of interest or digital-filter bandwidth: 2.5 kHz
- Unwanted sinusoid component at 3 kHz in sense element 1's path

In the circuit in Figure 1, the unwanted 3-kHz signal is effectively attenuated by the digital filter. This is because the 3-kHz signal is not aliased into the baseband. That is, the 3 kHz will show up at 3 kHz—even in the digital domain.

However, if the same 5-kHz amplifier is used for the circuit in Figure 2, and if the signals from the two sense elements are alternately sampled, the digital filter will be ineffective in attenuating the unwanted 3-kHz signal. This is because the effective sampling frequency of the signal from sense element 1 is only 5 kHz, even though the ADC sampling rate is 10 kHz. Thus, the 3 kHz will alias into the baseband (or appear as an in-band signal), rendering the digital filter ineffective in removing the unwanted signal.

It is noted that in order to prevent aliasing of the unwanted signal and to satisfy the Nyquist criterion, the amplifier bandwidth has to be lowered to 2.5 kHz. In this case, a 2.5-kHz digital filter is not needed any more; the digitized signal's bandwidth is limited to 2.5 kHz by the analog amplifier.

Unwanted wideband white noise

The signal paths in Figures 1 and 2 can produce unwanted wideband white noise. To investigate and clearly understand this, it will be assumed that the signal path does not have any unwanted sinusoid components. It will also be assumed that the signal path's white noise is the dominant source of noise compared to the quantization noise, which is usually the case in such signal paths.

Anti-aliasing filters for white noise: Case 1

With the independent signal paths shown in Figure 1, each 5-kHz amplifier acts as an anti-aliasing filter to limit the white-noise bandwidth of the respective signals to 5 kHz. The digital filters further reduce these bandwidths to 2.5 kHz, thus achieving a certain signal-to-white-noise ratio.

With the two analog signal paths in Figure 2 sharing a 5-kHz amplifier, sense element 1's effective sampling frequency is once again 5 kHz, assuming that the two sense-element outputs are sampled alternately. In this case, all

analog-domain noise from 2.5 to 5 kHz aliases into the 0- to 2.5-kHz range, which is the frequency band of interest. However, the root mean square (RMS) noise in this frequency range is not affected! In other words, the SNR is the same for this circuit as for that in Figure 1.

Anti-aliasing filters for white noise: Case 2

For Case 2, it is assumed that the signal band of interest is 1.25 kHz, which is half the band of interest used in Case 1. That is, the signal band is reduced because there is no signal content beyond 1.25 kHz that is wanted, and because limiting the noise bandwidth improves the SNR. Assuming that the 5-kHz amplifier is used for anti-aliasing, one will naturally conclude that a 1.25-kHz digital filter will reduce the bandwidth and achieve the same SNR for the circuit in Figure 1 as for the one in Figure 2. However, this is not the case. While it is true that, with the 5-kHz anti-aliasing filter, the RMS noise in the sampled domain is the same in both architectures, their noise densities are different. With the independent signal paths, the noise density of the sampled signals is $Noise_{RMS}/\sqrt{5\ kHz}$, while the noise density for the common signal path is $Noise_{RMS}/\sqrt{2.5\ kHz}$. Thus, using a 1.25-kHz band-limiting filter in the common analog signal path results in RMS noise of $\sqrt{1.25\ kHz} \times Noise_{RMS}/\sqrt{2.5\ kHz}$ at the digital filter's output. This noise is higher than the RMS noise in the independent signal paths, which is $\sqrt{1.25\ kHz} \times Noise_{RMS}/\sqrt{5\ kHz}$. That is, the SNR in the common signal path is worse than that in the independent signal paths. Note that these RMS calculations assume ideal filters, which are filters with 0-dB gain in the passband and infinite attenuation in the stopband.

Simulation model

Figure 3 shows a MATLAB®/Simulink® model used to analyze the effect of signal-path architectures on unwanted wideband white noise. The model includes both the circuit with independent signal paths and the circuit with a common signal path. Note that the downsample-by-2 block is used to represent the effects of alternate sampling of the common signal path. The analog amplifier is assumed to have a gain of 10 and is a fourth-order elliptical low-pass filter. The FDA tool in MATLAB/Simulink was used to design the digital filters in Figure 3, which are also fourth-order elliptical low-pass filters.[1]

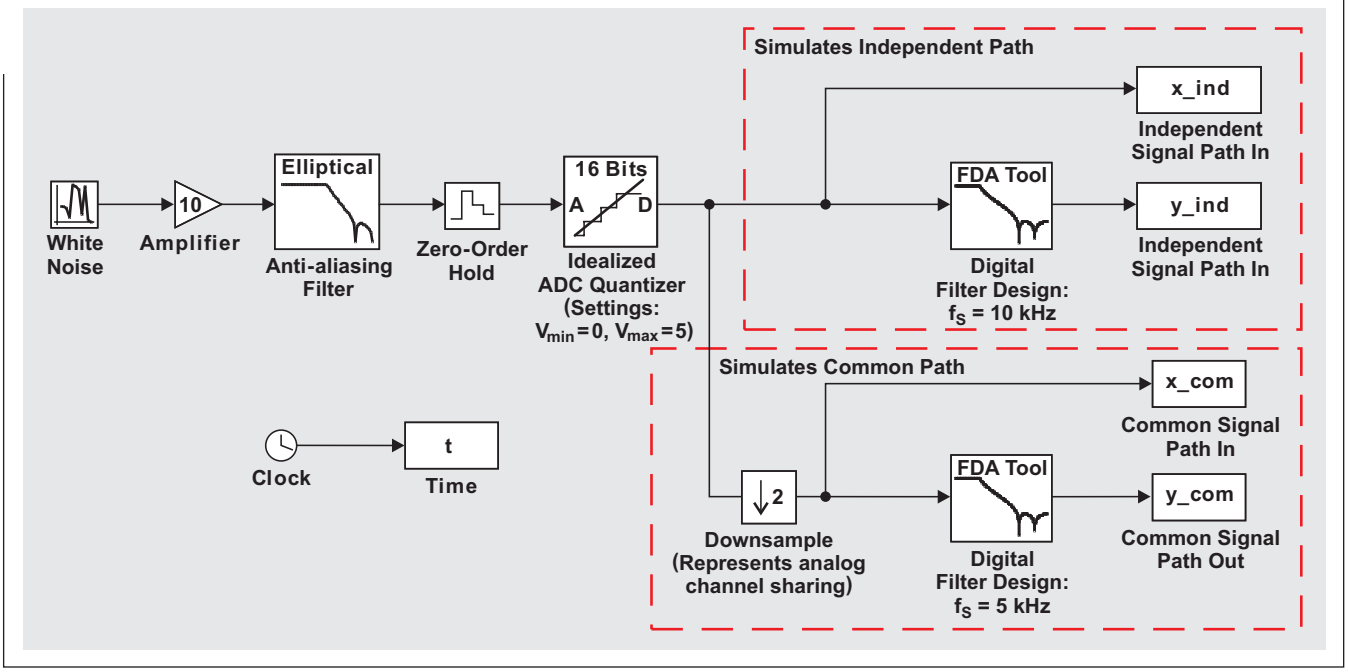
Table 1. RMS noise of the independent and common signal paths

AMPLIFIER BANDWIDTH (kHz)	std(x_ind)	std(y_ind) WITH DIGITAL FILTER	std(x_com)	std(y_com) WITH DIGITAL FILTER
5	7018	3250	7004	4806
2.5	4934	3300	4938	3365

Table 1 summarizes the RMS noise of the 1.25-kHz digital filter when the amplifier bandwidth is 5 kHz or 2.5 kHz. The MATLAB "std" function was used to calculate the RMS noise.

For the amplifier bandwidth of 5 kHz, the RMS value of the ADC output and its downsampled-by-2 value shown in the "std(x_ind)" and "std(x _com)" columns, respectively, are about the same. That is, the downsampling does not

Figure 3. MATLAB®/Simulink® simulation model



affect the RMS value. Therefore, if the downsampled value is used directly without further digital filtering, then the signal-to-white-noise ratio for the common signal path is the same as for the independent signal path.

For the amplifier bandwidth of 2.5 kHz, the RMS values of the digital-filter outputs are shown in the "std(y_ind)" and "std(y_com)" columns. From the data in these columns, it is clear that the effect of the 1.25-kHz digital filter depends on the frequency of the analog anti-aliasing filter. If the anti-aliasing filter's bandwidth is 2.5 kHz, which corresponds to half of the sampling frequency in the common signal path, then the noise at the output of the common-path digital filter matches the noise at the output of the digital filter in the independent signal path. If, however, the anti-aliasing filter's bandwidth is 5 kHz, then the RMS values of the digital-filter outputs are very different, resulting in different signal-to-white-noise ratios.

Conclusion

For multimodal, mixed-signal sensor-signal conditioners, the bandwidths of anti-aliasing filters have to be chosen appropriately to remove unwanted signals and to achieve the desired SNRs. If a sigma-delta modulator ADC is used, ADC samples that are unsettled after switching have to be discarded. This reduces the effective sampling rate even more.

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