High-Performance Analog Products

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Introduction

The *Analog Applications Journal* is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they apply to the following product categories:

- Data Converters
- Power Management
- Interface
- Amplifiers
- Low-Power RF
- General Interest

Analog Applications Journal articles include many helpful hints and rules of thumb to guide readers who are new to engineering, or engineers who are just new to analog, as well as the advanced analog engineer. Where applicable, readers will also find software routines and program structures.

Low-cost solution for measuring input power and RMS current

By Bosheng Sun
Systems Engineer

Introduction

Real-time measurement of energy consumption, including measurement of real input power and input RMS current for off-line power supplies, is becoming ever more important nowadays. These measurements can be used to adjust power delivery and optimize energy usage. More specifically, data centers, which contain many servers, are interested in submetering at the server level to implement low-cost data services and intelligently manage power processing during lower-power operation. The usual method of measuring input power and current uses a dedicated power-metering chip and an extra sensing circuit. While the power-metering chip provides acceptable results, it significantly increases the cost and design effort. This article provides a novel, low-cost but accurate solution for measuring input power and RMS current. It utilizes the existing digital power-factor-correction (PFC) control chip and hardware, with simple two-point calibration and optimized mathematical calculations. This provides excellent measurement accuracy and greatly reduces the cost and design effort, while having no impact on normal PFC control.

Measurement setup

Figure 1 shows a conventional PFC setup controlled by a digital controller for isolated power. The input line and neutral voltages are both sensed through an attenuation network and are subsequently sampled by two separate analog-to-digital-converter (ADC) inputs. The current signal is sensed by a current shunt and is amplified and filtered by a signal-conditioning circuit. It is then connected to an ADC for current-loop control. Since the input voltage and current measurements are already available, they can be used to measure the input power and RMS current as well. The same conventional PFC setup is used for these measurements. The traditional dedicated power-metering chip and extra sensing circuit are eliminated.

Current measurement and calibration

The current-sense signal-conditioning circuit (Figure 1) normally consists of an operational amplifier and a low-pass filter to amplify the small sensed signal and remove high-frequency noise. The signal is then measured by an ADC and reported in ADC counts. To get the real current value, the ADC counts need to be translated back to current in amperes. The relationship between ADC counts and amperes can be derived from the schematic; however, the component tolerances could make the measurement accuracy unacceptable. Therefore, a calibration is needed.

Given the circuit in Figure 1, at any moment the input current through the current shunt in milliamperes is

$$i = k_i C_i - m_i, \quad (1)$$

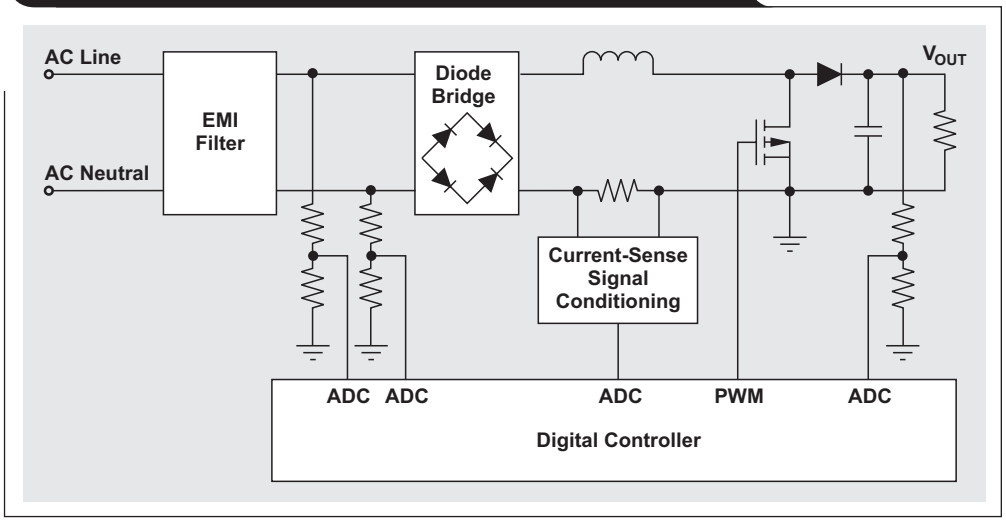
where k_i is the current-sense gain or slope, C_i is the ADC-conversion output (count), and m_i is the current-sense offset.

For constant direct-current (DC) input, the average value equals the instantaneous value, so Equation 1 is still valid:

$$I_{DC} = k_i C_i - m_i \quad (2)$$

Equation 2 indicates that a DC source can be used to calibrate the current-measurement circuit. A constant DC power is applied to the PFC input, and measurements are taken with a 25% load and then a 75% load. For comparison, a meter is used to provide benchmark measurements of actual input current for both load conditions. The count output of the ADC conversion is also read for both load

Figure 1. PFC setup for measuring input power and current



conditions to determine the accuracy of the digital controller. The controller uses the following mathematical relationships. For a 25% load,

$$I_{DC1} = k_i C_{i1} - m_i. \quad (3)$$

For a 75% load,

$$I_{DC2} = k_i C_{i2} - m_i. \quad (4)$$

The current slope and offset can be calculated from Equations 3 and 4:

$$k_i = \frac{I_{DC2} - I_{DC1}}{C_{i2} - C_{i1}} \quad (5)$$

$$m_i = \frac{C_{i1} I_{DC2} - C_{i2} I_{DC1}}{C_{i2} - C_{i1}} \quad (6)$$

The calculated k_i and m_i are decimals and could be less than 1, while most of the digital controllers in PFC applications use a fixed point in mathematical calculation. To reduce the rounding errors and maintain enough accuracy in the calculations, the small decimal values are multiplied by 2^N and then rounded to the closest integer. For example, if the current-sense gain and offset for a PFC circuit are calculated as $k_i = 1.59$ and $m_i = 229.04$, then k_i will be multiplied by 2^8 and rounded to 407; and m_i will be multiplied by 2^0. The current slope and offset will respectively be

$$k_i = \text{iin\_slope} >> \text{iin\_slope\_shift}$$

and

$$m_i = \text{iin\_offset} >> \text{iin\_offset\_shift},$$

where iin_slope = 407, iin_slope_shift = 8, iin_offset = 229, and iin_offset_shift = 0.

When the input power and RMS current are calculated, if k_i and m_i are multipliers, then instead of using them directly, one can use iin_slope and iin_offset to do multiplication first. Then the result is right shifted by iin_slope_shift and iin_offset_shift. For example, instead of the calculation $y = k_i \times x + m_i \times z$, the following can be used:

$$y = [(\text{iin\_slope} \times x) >> \text{iin\_slope\_shift}] + [(\text{iin\_offset} \times z) >> \text{iin\_offset\_shift}]$$

Input-voltage measurement and calibration

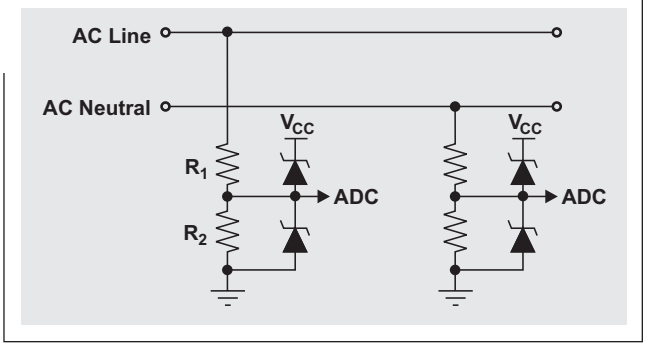
The voltage-sense circuit is quite simple and can be just a voltage divider, as shown in Figure 2. Usually there are clamp diodes to protect the ADC pins. Since the reverse leakage current of the diodes affects the ADC's measurement accuracy, diodes with low reverse leakage current should be chosen.

At any moment, the input voltage is

$$v = k_v C_v - m_v, \quad (7)$$

where k_v is the voltage-sense gain, C_v is the ADC-conversion output (count), and m_v is the voltage-sense offset. k_v and m_v can be calibrated in a way similar to calibrating the current-sense gain and offset. However, a much simpler way is to just calculate from the schematic. Since there is no calibration, the accuracy of the resistance used for the voltage divider affects measurement accuracy. Using low-tolerance resistors as the voltage divider is recommended—for example, 0.1% tolerance.

Figure 2. Voltage-sense circuit for AC input



For a digital controller with a 12-bit ADC and referenced to 2.5 V, the input voltage is attenuated by the voltage divider to a magnitude of less than 2.5 V. Then the attenuated signal is converted to a digital signal by the ADC. Therefore,

$$C_v = \frac{vR_2}{2.5(R_1 + R_2)} \times 4096. \quad (8)$$

By rearranging Equation 8, the input voltage can be calculated as

$$v = \frac{2.5(R_1 + R_2)}{4096 R_2} \times C_v. \quad (9)$$

Therefore,

$$k_v = \frac{2.5(R_1 + R_2)}{4096 R_2}, \quad (10)$$

and

$$m_v = 0. \quad (11)$$

Similar to the input-current measurement, the voltage-sense gain and offset need to be manipulated to accommodate a fixed-point microprocessor and to reduce the calculation error.

V_{IN} and I_{IN} correlation

Real input power is defined as

$$P = \frac{1}{T}\int_0^T v(t)i(t)dt. \quad (12)$$

In discrete format, it is defined as

$$P = \frac{\sum[v(n)i(n)]}{N}, \quad (13)$$

where N is the total number of samples. Equation 13 indicates that V_{IN} and I_{IN} need to be sampled at the same time. However, V_{IN} and I_{IN} are sampled at different times by two different ADC channels. Even the small time discrepancy can contribute to a measurement error. In some

digital controllers, such as the Texas Instruments UCD3138, a mechanism called *dual sample-and-hold* is provided that allows these two channels to be sampled simultaneously, eliminating this error.

Due to the low-pass filter used in the current-sense circuit, the measured current signal is delayed and out of phase with the actual current. This is shown in Figure 3, where Channel 2 is the actual current signal; and Channel 1 is the same signal amplified, which then comes out of the low-pass filter. The amplified signal has a phase delay of about 220 µs. This delay needs to be compensated for; otherwise it will affect the accuracy of the input-power measurement. A simple way to compensate is to delay the V_{IN}-sense signal by about 220 µs, then use the delayed V_{IN} signal to do an input-power calculation. So if V_{IN} is measured every 20 µs, it needs to be delayed by 220/20 = 11 times.

Calculating real input power

Combining Equations 1, 7, and 13 yields

$$P = \frac{k_v k_i \sum C_v(n) C_i(n)}{N} - \frac{k_v m_i \sum C_v(n)}{N} - \frac{k_i m_v \sum C_i(n)}{N} + m_v m_i. \quad (14)$$

V_{IN} and I_{IN} are measured by ADCs in the standard interrupt loop, which has a limited time period and is mainly used for PFC loop control. Therefore, to save CPU calculation time and prevent overflow in the standard interrupt loop, only $C_v(n)C_i(n)$ is calculated in this loop. Also, the terms

$$\frac{\sum C_v(n) C_i(n)}{N}, \frac{\sum C_v(n)}{N}, \text{ and } \frac{\sum C_i(n)}{N}$$

from Equation 14 are implemented with infinite impulse response (IIR) filters. The final calculation of real input power is done in the background loop.

Calculating input RMS current

The current measurement by the digital controller in Figure 1 does not represent the total input current, since the contribution of the capacitance in the electromagnetic-interference (EMI) filter is not included. At high line voltage and light load, this filter current is not negligible any more and must be included for accurate input-current reporting.

Figure 4 shows a simplified EMI filter where the inductors are removed and the total capacitance is replaced with a single capacitor (C). In this figure, I_{EMI} is the RMS reactive current of the EMI capacitor, $I_{Measure}$ is the input RMS current measured by the digital controller, and I_{IN} is the total input RMS current.

The reactive current produced by the EMI filter is

$$I_{EMI} = 2\pi f C V_{IN(RMS)}. \quad (15)$$

To calculate the reactive current of the EMI capacitor, the input-voltage frequency first needs to be determined. The AC line and neutral voltage are sensed by two ADC channels and then rectified by firmware. The zero crossing is

Figure 3. Current-sense phase shift

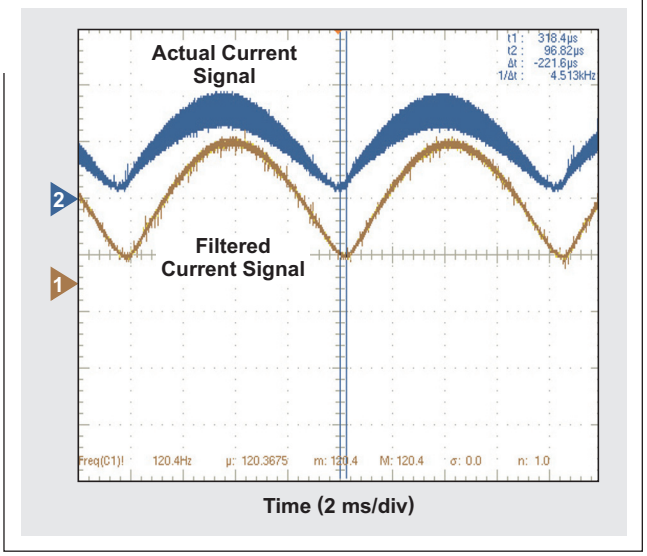
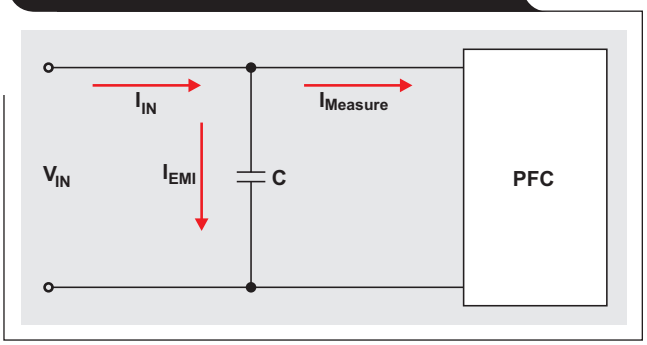


Figure 4. Current in simplified EMI filter



found by comparing the two ADC results. Since the input voltage is sampled at a fixed rate, the AC frequency can be calculated by counting the number of samples between two consecutive zero-crossing points. Once the input-voltage frequency is known, the reactive current of the EMI capacitor is calculated as

$$I_{EMI} = 2\pi f C \sqrt{\frac{k_v^2 \sum C_v^2(n)}{N} - \frac{2k_v m_v \sum C_v(n)}{N} + m_v^2}. \quad (16)$$

As stated earlier, the voltage is measured in the standard interrupt loop; so, to save CPU calculation time and prevent overflow in this loop, only $C_v^2(n)$ is calculated in it. The terms

$$\frac{\sum C_v^2(n)}{N} \text{ and } \frac{\sum C_v(n)}{N}$$

from Equation 16 are implemented with IIR filters. The final EMI reactive current is calculated in the background loop.

The current measured by the ADC is defined as

$$I_{Measure(RMS)} = \sqrt{\frac{1}{T}\int_0^T i(t)^2 dt}. \quad (17)$$

In discrete format, it is defined as

$$I_{Measure(RMS)} = \sqrt{\frac{\sum i_{IN}(n)^2}{N}}. \quad (18)$$

Combining Equations 1 and 18 leads to

$$I_{Measure(RMS)} = \sqrt{\frac{k_i^2 \sum C_i^2(n)}{N} - \frac{2k_i m_i \sum C_i(n)}{N} + m_i^2}. \quad (19)$$

As stated earlier, the current is measured in the standard interrupt loop; so only $C_i^2(n)$ is calculated in this loop. The terms

$$\frac{\sum C_i^2(n)}{N} \text{ and } \frac{\sum C_i(n)}{N}$$

from Equation 19 are implemented with IIR filters.

Finally, the EMI filter's reactive current (I_{EMI}) is added to $I_{Measure(RMS)}$ to get the total input current. I_{EMI} leads the measured current ($I_{Measure(RMS)}$) by 90°; therefore,

$$I_{IN(RMS)} = \sqrt{I_{EMI}^2 + I_{Measure(RMS)}^2}. \quad (20)$$

The final input RMS current is calculated in the background loop.

Test results

This method of measuring input power and RMS current was tested on a 360-W PFC evaluation module. The results, shown in Table 1, demonstrate that this method provides excellent measurement accuracy.

Conclusion

A low-cost but accurate method of measuring input power and RMS current for off-line power supplies has been presented. This method uses the existing PFC controller chip and hardware, eliminating the traditional dedicated power-metering chip and extra sensing circuit, with no impact on normal PFC control. In addition, it provides the following features:

- Extremely low cost
- Simple two-point calibration
- Simultaneous sampling of V_{IN} and I_{IN} with dual sample-and-hold
- Firmware EMI-current compensation
- Firmware current-sense, phase-shift compensation
- Optimized mathematical calculations with little overhead in CPU usage

Reference

1. "Highly integrated digital controller for isolated power," UCD3138 Data Manual. Available: www.ti.com/slusap2-aaj

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Table 1. Test results of measuring input power and RMS current

OUTPUT LOAD (%)	P_{IN} (W)			$I_{IN(RMS)}$ (mA)		
	WITH METER	WITH DIGITAL CONTROLLER	DIFFERENCE	WITH METER	WITH DIGITAL CONTROLLER	DIFFERENCE
$V_{IN(RMS)}$ = 110 V						
2.50	11.5	10.3	1.2	112	101	11.0
5	18.8	17.9	0.9	180	170	10.0
10	35.4	34.3	1.1	328	317	11.0
20	72.7	71.7	1.0	665	659	6.0
30	107.7	107.2	0.5	989	985	4.0
40	143.5	143.1	0.4	1314	1315	–1.0
50	181.0	180.4	0.6	1656	1661	–5.0
60	216.3	215.4	0.9	1980	1987	–7.0
70	251.6	250.4	1.2	2305	2315	–10.0
80	287.0	285.3	1.7	2631	2643	–12.0
90	324.9	322.8	2.1	2981	2994	–13.0
100	360.6	357.9	2.7	3313	3325	–12.0
$V_{IN(RMS)}$ = 230 V						
2.50	11.0	9.1	1.9	88	87	1.0
5	19.0	16.8	2.2	111	105	6.0
10	36.5	34.5	2.0	177	168	9.0
20	71.1	69.1	2.0	320	311	9.0
30	107.7	106.0	1.7	477	469	8.0
40	144.9	143.1	1.8	637	631	6.0
50	179.4	177.6	1.8	786	782	4.0
60	216.1	214.6	1.5	945	942	3.0
70	253.1	251.6	1.5	1105	1106	–1.0
80	287.7	286.4	1.3	1256	1258	–2.0
90	324.5	322.9	1.6	1416	1419	–3.0
100	361.2	359.9	1.3	1576	1580	–4.0

Dynamic power management for faster, more efficient battery charging

By Samuel Wong
Systems Engineer

Introduction

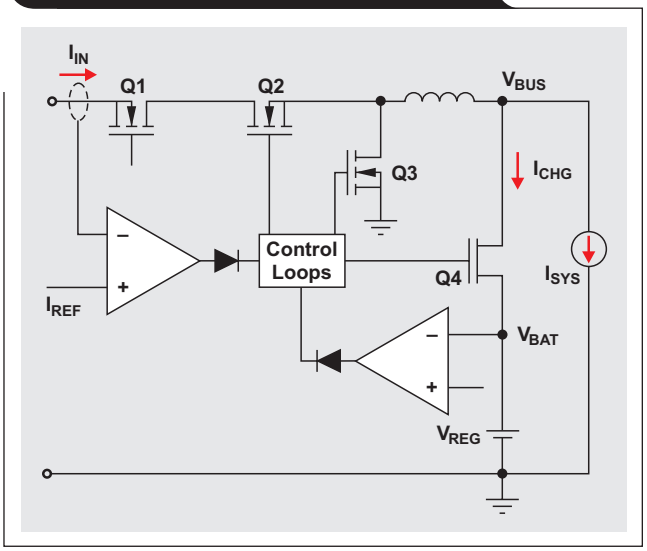
With the fast-growing demand for emerging portable devices such as tablets and smartphones, there are many new challenges in improving battery-operated system performance. The battery-management system must be intelligent to support different types of adapters and battery chemistries and must provide fast charging with high efficiency. At the same time, it is important to provide a good user experience with instant turn-on of the system, longer battery run time, and fast charging. This article discusses how to achieve fast battery charging and improve battery-charging performance with dynamic power management (DPM). DPM helps to avoid system crashes and maximizes the power available from the adapter. It can be based on input current or input voltage, or combined with a battery-supplement mode. This article also discusses critical design considerations for extending battery run time.

The lithium-ion (Li-Ion) battery is desirable for the ever-growing power need in portable devices because it has very high energy density. Nowadays, it is common for a 10-inch tablet to include a battery pack with 6- to 10-Ah capacity to support a long run time. With the high-capacity battery, it is critical for the portable device to have fast and efficient charging for a good user experience. Additionally, tablets require other features such as superior thermal performance and instant turn-on, even with a deeply discharged battery. These requirements present a few technical challenges. One is how to maximize available power from the power source to efficiently and quickly charge the battery —while not crashing the power source. Another is how to charge a deeply discharged battery while simultaneously operating the system. Last is how to extend the battery run time and improve thermal performance.

Dynamic power management (DPM)

How can available power be maximized to charge the battery quickly and efficiently? Every power source has its output current, or power limit. For example, the maximum output current is limited to 500 mA from a high-speed USB (USB 2.0) port, and up to 900 mA from a SuperSpeed USB (USB 3.0) port. The power source can crash if the system's power demand exceeds the power available from the power source. When the battery is being charged, how can a power-source crash be prevented while the power output is being maximized? The following discussion presents three control methods: DPM based on input current, DPM based on input voltage, and DPM used with a battery-supplement mode.

Figure 1. DPM based on input current



DPM based on input current

Figure 1 shows a high-efficiency switch-mode charger with DPM controls. MOSFETs Q2 and Q3 and inductor L make up a synchronous switching buck-based battery charger. Using a buck converter ensures that the adapter's input power is efficiently converted to achieve the fastest battery charging. MOSFET Q1 is used as a battery reverse-blocking MOSFET for preventing leakage from the battery to the input through the body diode of MOSFET Q2. It also is used as an input-current sensor to monitor the adapter current.

MOSFET Q4 is used to actively monitor and control the battery-charging current to achieve DPM. When the input power is sufficient to support both the system load and battery charging, the battery is charged with the desired charge-current value of I_{CHG}. If the system load (I_{SYS}) is suddenly increased and its total adapter current reaches the current-limit setting (I_{REF}), the input-current regulation loop actively regulates and maintains the input current at the predefined I_{REF} input reference current. This is achieved by reducing the charge current while giving higher priority to powering the system so it can reach its highest performance. Therefore, the input power is always maximized without crashing the input-power source, while the available power is dynamically shared between the system and battery charging.

DPM based on input voltage

If a third-party power source is plugged into a system that cannot identify its current limit, it is difficult to use DPM based on limiting the input current. Instead, DPM is based on the input voltage (Figure 2). Resistor dividers R1 and R2 are used to sense the input voltage and are fed into the error amplifier of the input-voltage regulation loop. Similarly, if the system load is increased, causing the input current to exceed the adapter's current limit, the adapter voltage starts to decrease and eventually reaches the predefined minimum input voltage. The input-voltage regulation loop is activated to maintain the input voltage at the predefined level. This is achieved by automatically reducing the charge current so that the total current drawn from the input-power source reaches its maximum value without crashing the source. Therefore, the system can track the adapter's maximum input current. The input-voltage regulation is designed to keep the voltage high enough to fully charge the battery. For example, the voltage can be set around 4.35 V to fully charge a single-cell, Li-Ion battery pack.

Battery-supplement mode

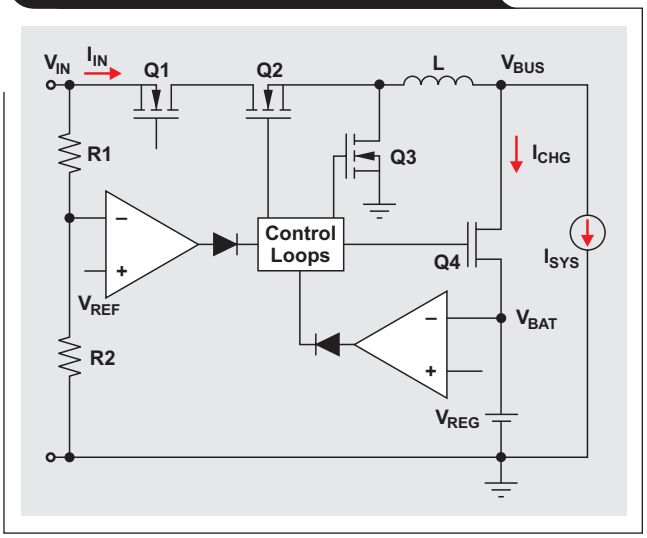
DPM based on input current or input voltage can draw the maximum power from the adapter without crashing it. For portable devices such as smartphones and tablets, the system load is usually dynamic with a high pulsating current. What happens if the pulsating system's peak power is higher than the input power, even when the charge current is already reduced to zero? The input-power source could crash without active control.

One solution is to increase the adapter's power rating, but this increases the adapter's size and cost. Another solution is to temporarily have the battery provide additional power to the system by turning the MOSFET Q4 on to discharge the battery instead of charging it. Combining the DPM control and the battery-supplement mode allows the adapter to be optimized to support the average power instead of the maximum peak system power, reducing the cost and achieving the smallest solution size.

Design considerations for improving system performance

Portable systems such as tablets and smartphones require instant turn-on to provide a good user experience. This means that whether the battery is fully charged or deeply discharged, the system will turn on instantly when an adapter is plugged in.

Figure 2. DPM based on input voltage

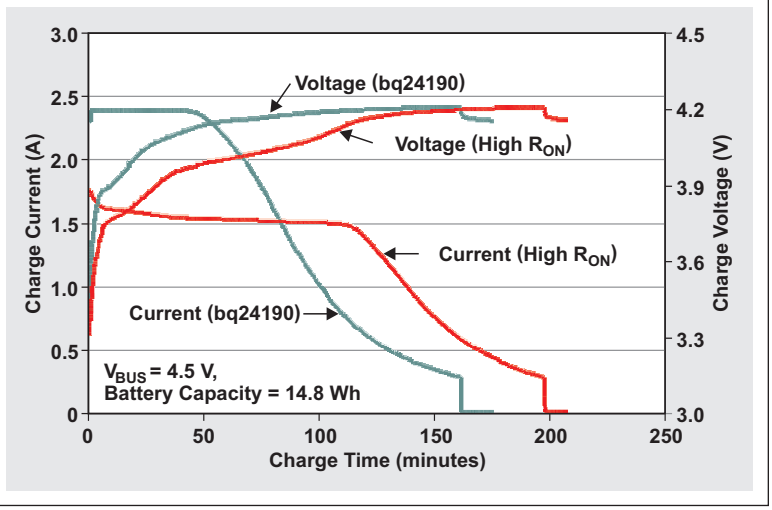


As an example, suppose that a one-cell Li-Ion battery is used for the systems in Figures 1 and 2. If the battery is directly connected to the system without MOSFET Q4, the system bus voltage (V_{BUS}) is the same as the battery voltage. A deeply discharged battery with less than 3 V may prevent system turn-on. The user may have to wait until the battery is charged to 3.4 V before turning on the system. In order to support instant turn-on, MOSFET Q4 is added to operate in linear mode to maintain the minimum system-operation voltage while simultaneously charging a deeply discharged battery. The minimum system voltage is regulated by the switching converter, and the charge current from Q4 is regulated with a linear control loop. Once the battery voltage reaches the minimum system voltage, MOSFET Q4 is fully turned on. Its charge current is then regulated by the duty cycle of the synchronous buck converter. So the system voltage is always maintained between the minimum system-operation voltage and the maximum battery voltage for powering the system.

In a 5-V USB charging system, all series resistance between the power source and the battery contributes to charging efficiency. This resistance in the charging path consists of the ON resistance of FETs Q1, Q2, and Q4 and about 250 mΩ from the USB cable. It is not unusual to have a 4.5-V charger input after a cable voltage drop. Therefore, it is critical to design a charger with the lowest possible

FET ON resistance to minimize charging time. Figure 3 compares the charging time of a design using the Texas Instruments bq24190 USB/adapter charger and an alternative design having an extra 80 mΩ in the charging path. It can be seen that, with a 4.5-V input voltage, the charging time of the bq24190 design is reduced by 20% compared with the other design.

Figure 3. Effect of high ON resistance in the charging path

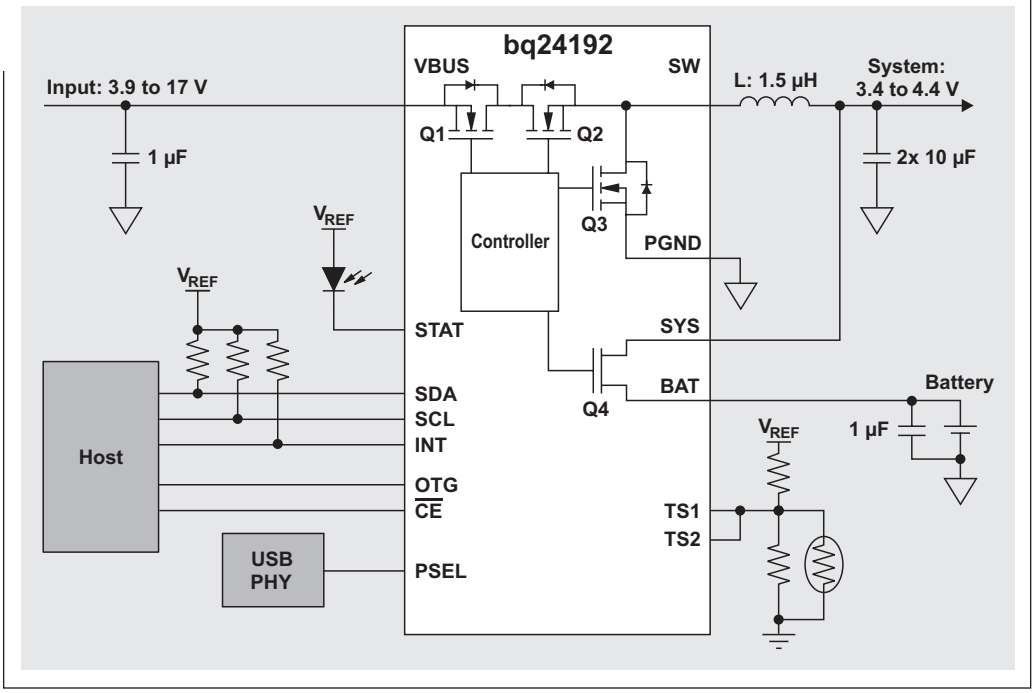


Extending battery run time

Of course, the higher the battery capacity, the longer is the battery run time. For a single-cell operating system that usually requires a 3.3-V output, the typical minimum system voltage is around 3.4 V. If the ON resistance of MOSFET Q4 is 50 mΩ, and the battery-discharge current is 3 A, the battery cutoff voltage is 3.55 V. This means that over 15% of the battery capacity is unused. In order to maximize the battery run time, the MOSFET Q4's ON resistance must be as small as possible. For instance, with an ON resistance of 10 mΩ and the same peak battery-discharge current of 3 A, the battery cutoff voltage will be 3.43 V. This provides 10% more battery capacity than with an ON resistance of 50 mΩ.

Figure 4 shows an example of a high-efficiency, single-cell I²C battery charger with integrated MOSFETs. This charger supports both USB and AC adapter inputs for tablets and portable media devices. All four power MOSFETs are integrated, while MOSFETs Q1 and Q4 are used to sense the input current and battery-charge current, further minimizing the system's solution size. This charger can distinguish between a USB port and an adapter to quickly set the correct input-current limit. Additionally, the charger can operate as a stand-alone charger with internal default charge current, charge voltage, a safety timer, and input-current limits—even when the system is turned off. The charger also has a USB On-the-Go (OTG) function, operating in boost mode to provide a 5-V, 1.3-A output at the USB input from the battery.

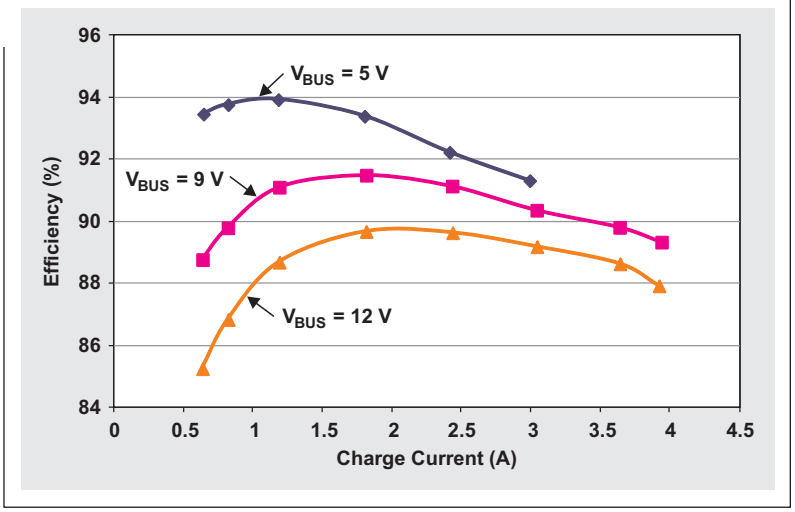
Figure 4. High-efficiency, 4-A I²C switching charger with DPM



Thermal performance

Thermal performance is critical for portable devices with a very thin profile because users can easily feel the heat dissipated from the printed circuit board. This heat is due to components that consume a lot of power, such as the battery charger. To combat this, a high-efficiency charger and a good layout are very important. To further improve the thermal performance, a thermal-regulation loop is available in the bq2419x family. It maintains the maximum junction temperature by reducing the charge current once the device reaches the predefined junction temperature. Figure 5 shows the measured battery-charging efficiency in a bq24190 design. Up to 94% efficiency can be achieved with a 5-V USB input. With a 9-V input and a 4-A charge current, there is only a 32°C temperature rise.

Figure 5. Measured battery-charging efficiency at different charge currents



Conclusion

This article has shown that DPM based on either input current or input voltage can be used to power portable devices, providing instant system turn-on while simultaneously charging the battery. It has also been shown that adding a battery-supplement mode is critical for optimizing power-system performance. Other design considerations have also been discussed, such as instant turn-on with a depleted battery, battery run time, charging-path resistance, and thermal performance.

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Techniques for accurate PSRR measurements

By John Rice, *System Engineer, Texas Instruments,*
and Steve Sandler, *Managing Director, Picotest*

Introduction

In theory, measuring the power-supply-rejection ratio (PSRR) is relatively simple. A variable-frequency signal modulates the power-supply input, and the attenuation of that signal is measured at the output. However, the measurement is highly sensitive to setup noise, including noise from the probe-loop area and the layout of the printed circuit board (PCB). This article explores commonly encountered setup issues that limit PSRR measurement and offers a method to overcome them using high-fidelity signal injectors and a highly sensitive/selective vector network analyzer (VNA).

Input-signal modulation

The easiest way to modulate the input to a regulator is with a line injector, such as the Picotest J2120A. This device accommodates 50 V at the input and an input current of 5 A. Coupled with a VNA, the J2120A directly modulates the input voltage while the VNA measures the input/output attenuation. The drawbacks of this method are the need to break into the input lines and the need to accommodate a voltage drop across the injector. While these drawbacks are generally not issues for bench testing, they can be troublesome when the measurement is performed in circuit.

An alternative way to modulate the input is to capacitively connect the VNA to the device under test by using a low-frequency DC blocker, such as the J2130A DC bias injector. The amplitude of the signal at the input is limited by the VNA's 50-Ω source impedance, but the signal is usually large enough to be measured by the VNA. This method does not require breaking into the input connection and therefore can be performed in circuit without adding any DC loading to the voltage bus being modulated.

Calibration

Before performing a PSRR measurement, it is important to correct for any probe variations. It is also important to measure the noise floor of the setup to determine measurement limitations. The image in Figure 1 shows the test board setup for calibration. The black and white wires are the input from the J2120A line injector. The red and black clips on the right are connected to a J2111A current injector that serves as a 25-mA load. The two probes are connected to a common output ground; and both probe tips are connected to the same input so they see the same modulation signal. A THRU calibration is then performed on the VNA in order to correct for any probe or cable-related imperfections. A flat gain response should be seen on the VNA over the frequency band of interest.

Figure 1. Test board setup for THRU calibration

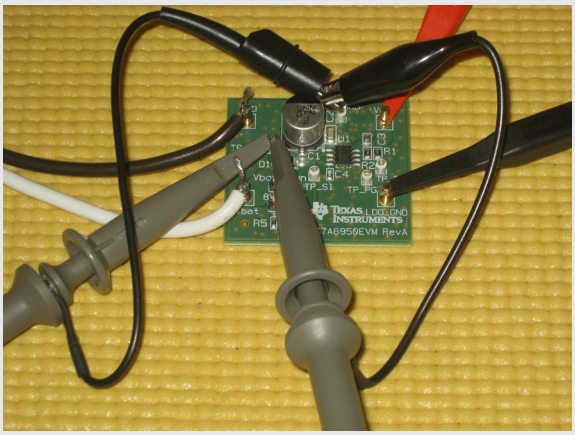


Figure 2. Noise-floor measurement with setup using scope probes

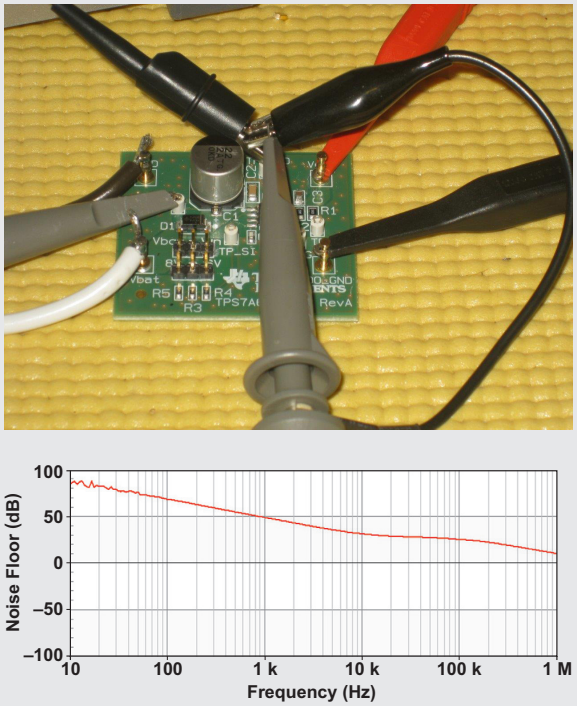
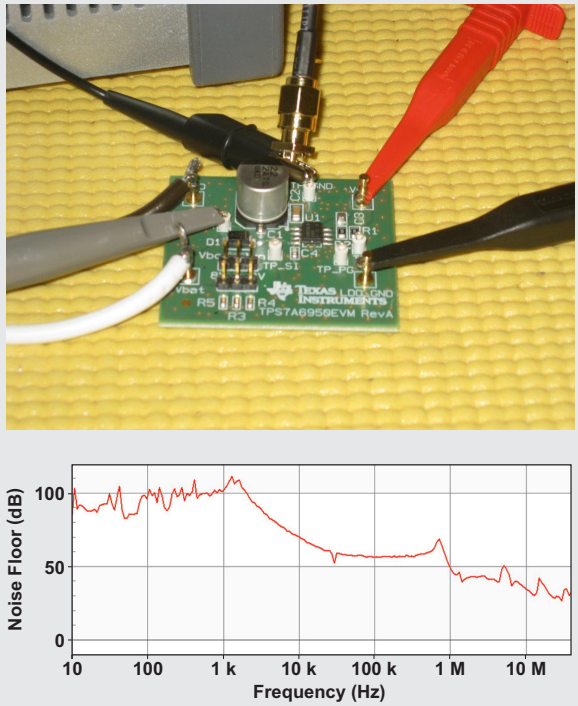


Figure 3. Noise-floor measurement with output scope probe replaced by 50-Ω coaxial cable



Assessing the noise floor

With the probe calibration completed, the noise floor can be assessed by shorting the output sense probe to the ground connection (Figure 2). It is clear from this measurement that this noise floor is far too high in relationship to the PSRR of most regulators today and that a better setup is required to ascertain the actual PSRR. In general, high-fidelity measurements like PSRR necessitate the use of carefully terminated connections with minimal probe-loop area. In fact, the low-fidelity measurement in Figure 2 is largely a result of induced noise in the wire loop created by the scope probe's ground clips.

In the next measurement setup, shown in Figure 3, the output scope probe is replaced with a 50-Ω coaxial cable via an SMA adapter soldered directly to the output capacitor. The cable is connected to the VNA through a J2130A DC blocker and a J2102A common-mode transformer. The probe is shorted at the output ground to assess the noise floor. From Figure 3 it is clear that the noise floor has been improved with over 90 dB out to 1 kHz. However, since most quiet power regulators from Texas Instruments (TI) have good PSRR out beyond 1 MHz, this noise floor is still unacceptable.

Next, the input-side scope probe is replaced with a 50-Ω coaxial cable soldered directly to the input capacitor (Figure 4). The complete setup (two 50-Ω coaxial cables

Figure 4. Input scope probe replaced by 50-Ω coaxial cable

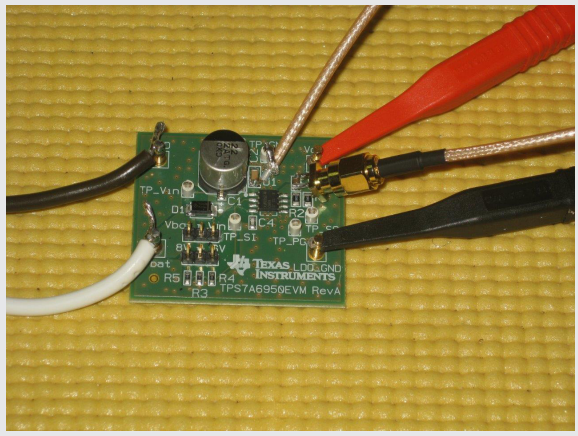


Figure 5. Complete setup and noise-floor/PSRR measurements

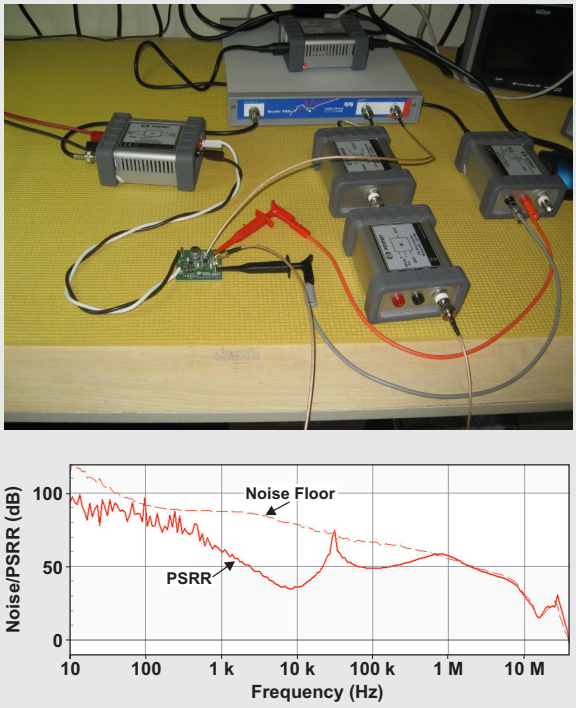


Figure 6. Optimized high-fidelity PSRR and noise-floor measurements

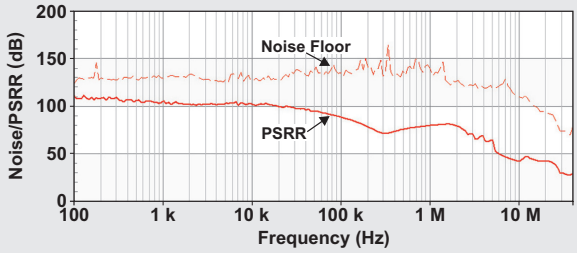
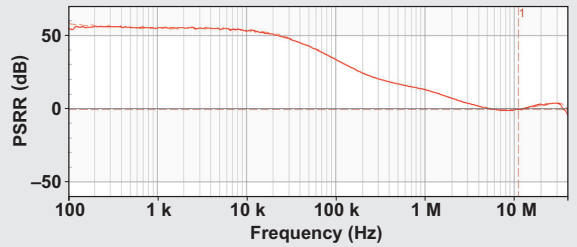


Figure 7. LM317's PSRRs measured with J2120A and J2130A



and the J2102A, J2130A, J2120A, and J2111A) and the noise-floor/PSRR measurements are shown in Figure 5. The setup has a much lower noise floor, facilitating a PSRR measurement to 1 MHz and a low-frequency PSRR over 90 dB. The PSRR resonance near 30 kHz is likely a result of the PCB layout or component parasitic interaction.

To illustrate the significance of a good setup, the PSRR of a carefully designed regulator, PCB layout, and setup is shown in Figure 6. This measurement shows that with careful setup and appropriate measurement equipment, it is possible to obtain a significantly lower noise floor, enabling very accurate PSRR measurements. Lastly, to validate the injection methods discussed earlier, the PSRR of TI's LM317 adjustable regulator was measured using a J2120A line injector (method 1) and a J2130A DC bias injector (method 2). Figure 7 shows nearly perfect overlapping plots, which means there is a very good correlation between the two injection methods.

Conclusion

This article illustrates that although PSRR measurement is simple in concept, the setup is of great significance in achieving an accurate result. A methodology for lowering the noise floor has also been presented.

Reference

1. Masashi Nogawa, "A topical index of TI LDO application notes," Application Report. Available: www.ti.com/sbva026-aaj

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Correcting cross-wire faults in modern e-metering networks

By Thomas Kugelstadt
Senior Systems Engineer

Electricity metering (e-metering) for commercial and residential applications relies heavily on long-haul, differential data-transmission networks based on the TIA/EIA-485 standard, commonly referred to as RS-485. In order to overcome the large ground-potential differences often encountered between remotely located bus nodes, each node is galvanically isolated, with regards to signal and supply lines, from the local e-metering circuitry.

The e-metering network is a typical master/slave system in which a host processor in the master node (located in a control center) sequentially addresses multiple slave nodes (located in the individual end customer's premises) along the bus.

With a single network comprising up to 60 nodes typically, the potential for unintentionally cross-wiring the two conductors of the twisted-pair bus cable can be rather high, if neither preventive measures during network installation nor corrective measures during network operation are applied.

The e-metering companies in the United States and Europe rely heavily on trained installation personnel and visually distinctive, color-coded cabling as preventive measures. This approach allows for the use of standard transceivers and cabling, such as isolated RS-485 transceivers and CAT-5 cable.

To further reduce the risk of wiring faults, recent network designs have been implementing a so-called training sequence that causes the slave nodes to adjust to the signal polarity of the master. During this sequence, the master broadcasts a unique bit pattern to all slaves. The same bit pattern, initially stored in each slave processor during power-up, is then compared with the pattern sent by the master. If the patterns match, the slave maintains its signal polarity. In the case of a mismatch, the slave processor inverts the signal polarity of both the incoming receive data and the outgoing transmit data. This inverting process is typically accomplished through an Exclusive-OR function within the slave processor and does not require any changes in hardware design. Thus, the proper operation of standard transceivers is still maintained.

In contrast to this approach, Asian e-metering companies push for more cost savings in network designs by using:

- Personnel inexperienced in network installation
- Low-cost, non-color-coded lamp wire instead of twisted-pair cable
- Dedicated transceivers with integrated signal-polarity correction

Figure 1 shows a typical e-metering network with SN65HVD888 polarity-correction (POLCOR) transceivers from Texas Instruments (TI). The master node contains a failsafe-biasing resistor network (R_{FS} and R_T) that determines the signal polarity on the bus. Both master and slave nodes require integrated polarity-correction logic in

Figure 1. Typical e-metering bus with POLCOR transceivers

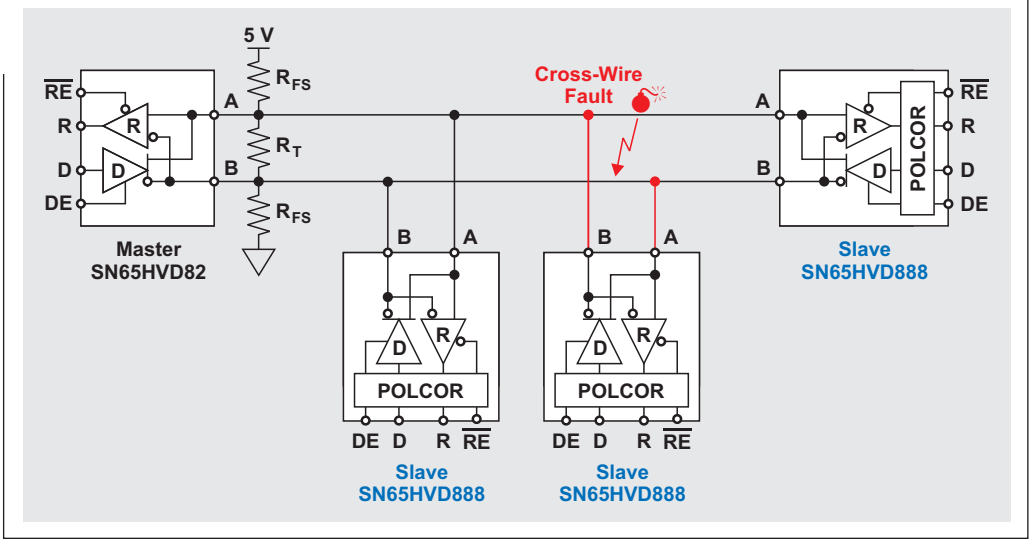
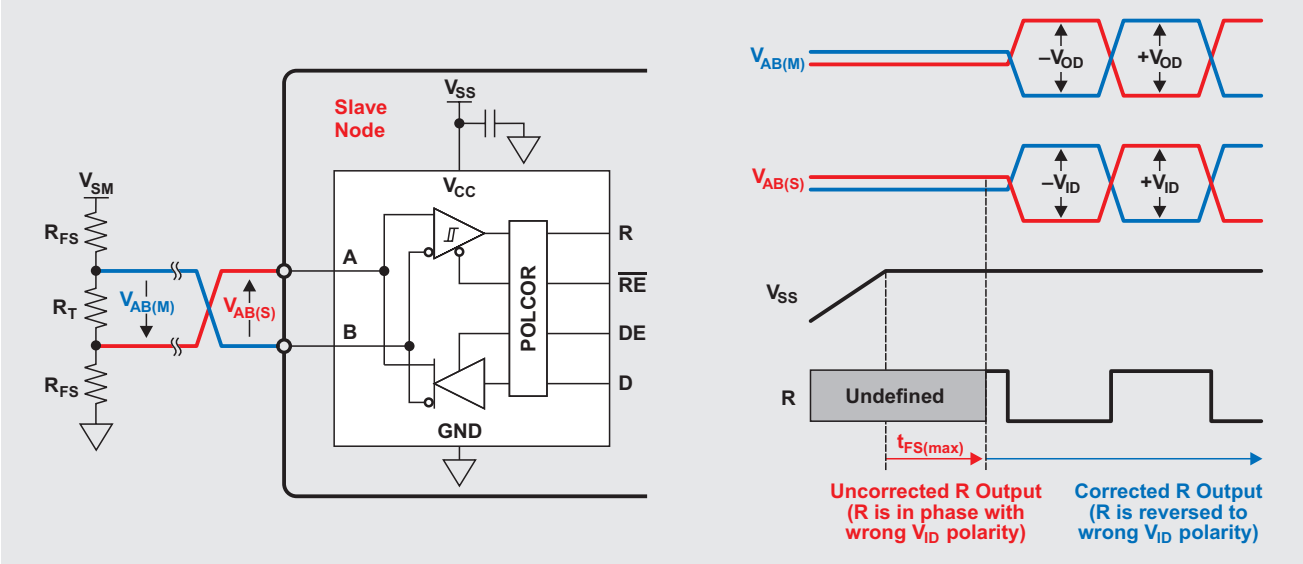


Figure 2. Polarity-correction timing after power-up



order to match the bus's signal polarity during bus idling. This correction logic consists of a debounce filter whose debounce time distinguishes between long data strings of the same signal polarity and actual bus-idle time. Due to the wide temperature range, across which the SN65HVD888 must be able to operate, the debounce time can vary between a lower limit of $t_{FS(min)}$ = 44 ms and an upper limit of $t_{FS(max)}$ = 78 ms.

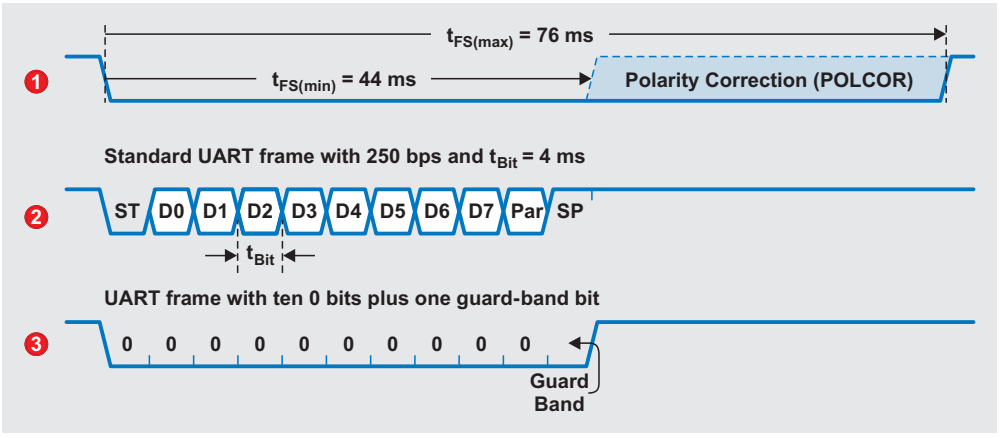
This means that a polarity correction might be initiated by a constant bus voltage that is present for as little as 44 ms. Therefore, a data string of consecutive 0 bits must be shorter than 44 ms to avoid causing polarity correction. Alternatively, an intended polarity correction, typically required after powering up the network or after the installation of a new bus node, requires a bus-idle voltage to be present for longer than 78 ms to ensure that the polarity correction is completed.

Hence, constant bus signals shorter than 44 ms are considered valid data. Those exceeding 78 ms are considered bus-idle states. Only idle states with differential voltages more negative than the negative receiver input threshold (V_{IT-}) cause the correction logic to invert signal polarity. Otherwise, a transceiver maintains its polarity status. Figure 2 gives an example of the polarity correction after a power-up sequence.

During power-up, the receiver output (R) is undefined. Once the slave-node supply (V_{SS}) is stable, the bus must idle for at least $t_{FS(max)}$ to ensure that the polarity correction is completed. Because of the cross-wire fault, the positive bus voltage at the master's failsafe network ($V_{AB(M)}$) appears negative at the transceiver input. Thus, after completion of $t_{FS(max)}$, the transceiver's internal polarity is switched to invert receive and transmit data. Hence, the negative input voltage ($V_{AB(S)}$) is converted into a positive output voltage.

The minimum debounce time of $t_{FS(min)}$ = 44 ms allows for the transmission of a 250-bps UART frame with eleven 0 bits without triggering the POLCOR logic. The bit rate of 250 bps was chosen to be lower than the minimum 300 bps used in e-metering. The structure of the UART frame with its start, data, parity, and stop bits is shown in Figure 3.

Figure 3. Standard UART frame will not trigger a polarity correction



Polarity correction with DL/T645 protocol

The e-metering protocol standard DL/T645 has further provisions to distinguish between long data strings of the same polarity and bus-idle states. Figure 4 shows how an example power value of 340078.56 W is processed within slave and master nodes.

The DL/T645 protocol calls for the measured decimal value in the driving slave node to be divided into groups of two digits. Each two-digit pair is converted into hexadecimal format (indicated by "h"). When these hex values arrive at the driver input, a 33h value is added. The resulting sum pattern is then transmitted through the driver output across the bus towards the master.

At the receiving master input, 33h is subtracted from the incoming sum pattern, thus yielding the original raw transmit data. Further, data processing converts the hex values back into decimal format.

Figure 5 shows a DL/T645-compliant data frame operating at the minimum rate of 300 bps and compares it to the minimum debounce time of 44 ms. Here the DL/T645 protocol requires a string of ten 0 bits (eight data bits plus the start and parity bits) to be converted into a bit sequence with a maximum of two consecutive 1 or 0 bits. However, because the start bit is always 0, a maximum of three consecutive 0 bits can occur at the beginning of a frame. Their combined duration of 10 ms, however, is far too short to cause an unintentional polarity correction.

Based on the three 0 bits at the frame start, it can be determined how far the data rate can be safely reduced when one bit is added as a guard band. If the four bits are spread across the 44-ms time window, the bit interval becomes 11 ms. This results in a minimum data rate of 1/11 ms ~ 91 bps. Therefore it is safe to say that the SN65HVD888 transceiver supports DL/T645-compliant data rates down to 100 bps.

Figure 4. Adding 33h to raw transmit data ensures short bit strings of the same polarity

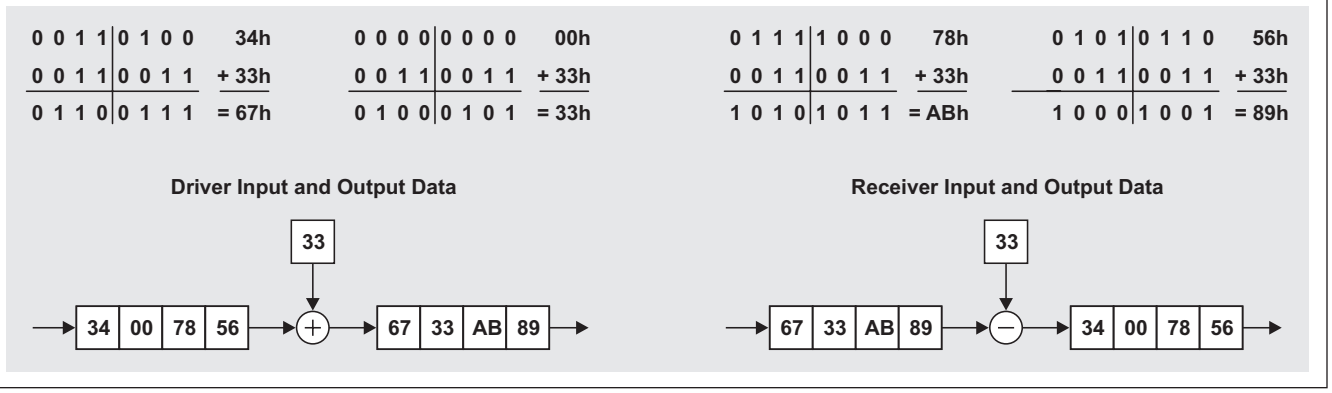


Figure 5. DL/T645-compliant data frame does not falsely trigger polarity correction

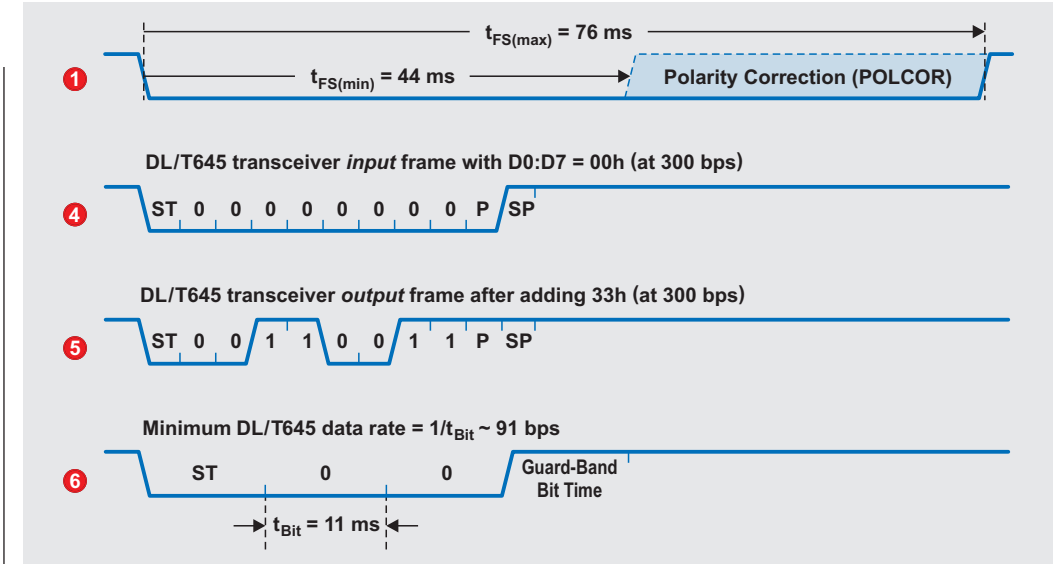
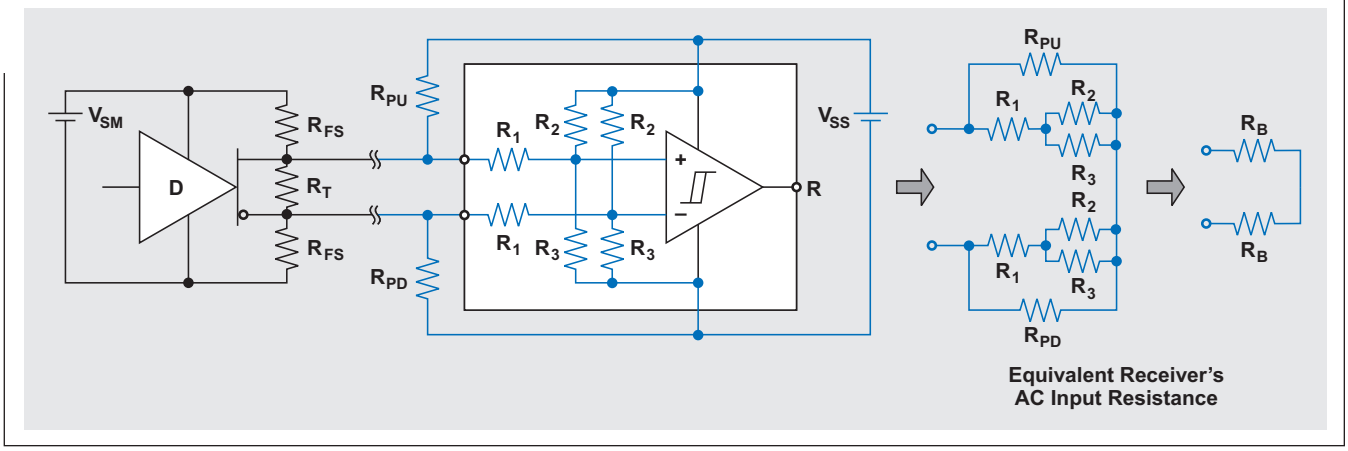


Figure 6. Simplified data link



Bus loading

To determine the maximum number of slave nodes the master can drive, two load conditions are evaluated—dynamic or AC loading, and static or DC loading.

AC loading

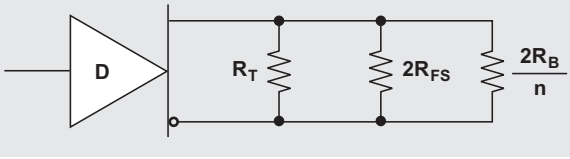
AC loading exists during data transmission when the master commands a slave to send data and the slave responds to this request. During this normal operation, signal transients occur on the bus that are affected by the capacitances of the bus cable, node connectors, transceiver inputs, and power supplies. To minimize the effect of capacitive reactance on the signal, e-metering networks operate at low data rates of 300 bps to 20 kbps. Therefore, the following discussion considers only resistive loads.

Figure 6 shows a simplified data link between a master, its failsafe-biasing network, and a remotely located slave receiver. Due to their large capacitance, the voltage supplies of the master (V_{SM}) and the slave (V_{SS}) can be seen as short circuits for AC signals. Hence, for the master node, the two failsafe resistors (R_{FS}) are connected in series and lie parallel to the termination resistor (R_T). The slave nodes are connected in a similar way. Here the internal DC-bias resistors (R_2 and R_3) are in parallel to one another, and their combined resistance is in series to a typical high-impedance R_1. Occasionally external pull-up/pull-down resistors (R_{PU} and R_{PD}, respectively) are used to further bias the node input. These resistors do nothing but load the bus because they lie in parallel to the internal resistance network of the receiver.

Note that when R_{FS} is kept between 1 and 2 kΩ, it is sufficient to bias the entire bus with a low-impedance biasing network at the master without further biasing at the slave nodes.

The resulting equivalent AC circuit is shown in Figure 7. Here $2R_B/n$ represents the input resistance of multiple (n) transceivers. Because the EIA-485 standard specifies a maximum differential driver load of R_L = 54 Ω, the parallel

Figure 7. Equivalent AC network



combination of all resistances on the bus must not exceed this value. This requirement is expressed in Equation 1:

$$\frac{1}{R_L} = \frac{1}{R_T} + \frac{1}{2R_{FS}} + \frac{n}{2R_B} \quad (1)$$

Solving for n yields Equation 2, which gives the maximum number of bus nodes that should be used under an AC-loading condition:

$$n = 2R_B \times \left(\frac{1}{R_L} - \frac{1}{R_T} - \frac{1}{2R_{FS}} \right) \quad (2)$$

Two commonly applied network designs are as follows:

1. The master uses a failsafe network with R_T =120 Ω and R_{FS} = 1 kΩ, while each slave is biased with external pull-up/pull-down resistors of $R_{PU} = R_{PD}$ = 20 kΩ, so that R_B ~ 18 kΩ. Under these conditions, the maximum number of potential nodes on the bus is limited to

$$n = 2 \times 18\ k\Omega \times \left(\frac{1}{54\ \Omega} - \frac{1}{120\ \Omega} - \frac{1}{2\ k\Omega} \right) = 348\ \text{nodes.} \quad (3)$$

2. The other scenario uses no termination resistor and rather high-impedance failsafe resistors of 10 kΩ. Also, the slave nodes operate without external biasing ($R_{PU} = R_{PD} = \infty$). In this case, R_B consists of only the receiver's internal resistance, which for the SN65HVD888 is 184 kΩ

per input. Due to this high-impedance loading, the theoretical number of bus nodes increases drastically to

$$n = 2 \times 184\ k\Omega \times \left(\frac{1}{54\ \Omega} - \frac{1}{40\ k\Omega} \right) = 6805 \text{ nodes.} \quad \textbf{(4)}$$

These two examples yield rather high numbers of bus nodes in comparison to the average e-metering network comprising only 40 to 60 nodes. The next section, "DC loading," shows that the AC-loading evaluation is misleading, as it does not consider the bus's leakage currents caused by the bus-node supplies.

DC loading

DC loading occurs during bus idling when no transceiver is actively driving the bus. In this state, the supply of the master (V_{SM}) drives current through the nearby failsafe network to establish a positive bus failsafe voltage (V_{FS}). This voltage determines the signal polarity for all slave nodes. Like the master supply, the slave supply (V_{SS}) drives current through its internal resistor network. Part of this current leaks through the input resistance (R_1) into the bus. The remaining current then flows through R_T and returns through R_1 of the opposite terminal (Figure 6).

Correctly wired nodes drive currents through R_T in the same direction as the master supply. However, cross-wired nodes drive current in the opposite direction through R_T. This reduces the combined current through R_T, and with it the failsafe voltage (V_{FS}). At a certain number of cross-wired nodes, V_{FS} can become so small that it falls within the receiver's input sensitivity, causing all bus nodes to assume indeterminate output states. To avoid this condition, the failsafe network at the master must be dimensioned so that even if all slaves are cross-wired, a positive V_{FS} is still maintained.

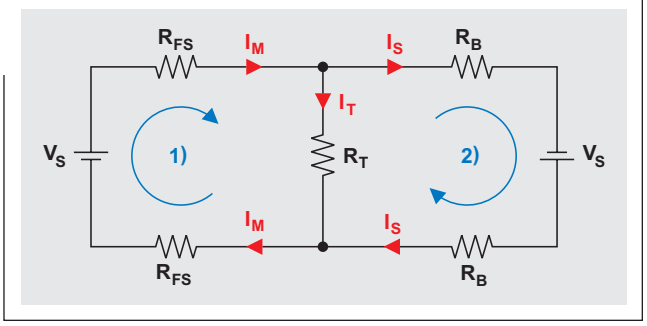
Figure 8 illustrates this scenario for only one slave node in order to simplify the mathematical derivations of the voltage and current relations within the network. Because V_{SM} equals V_{SS}, both supplies are simplified to V_S.

Equations 5 and 6 describe the two existing voltage loops, while Equation 7 expresses the current in the upper summing node:

$$-V_S + I_M \times 2R_{FS} + I_T \times R_T = 0 \quad \textbf{(5)}$$

$$-V_S + I_S \times 2R_B - I_T \times R_T = 0 \quad \textbf{(6)}$$

Figure 8. Equivalent DC network



$$I_T = I_M - n \times I_S \quad \textbf{(7)}$$

Note that in Equation 7, the slave current (I_S) is multiplied by a factor n, indicating multiple slave nodes.

The master and slave currents are determined by solving Equation 5 for I_M and Equation 6 for I_S, yielding Equations 8 and 9, respectively:

$$I_M = \frac{V_S - I_T \times R_T}{2R_{FS}} \quad \textbf{(8)}$$

$$I_S = \frac{V_S + I_T \times R_T}{2R_B} \quad \textbf{(9)}$$

Inserting the equations for I_M and I_S into Equation 7 and substituting I_T with V_{FS}/R_T gives

$$\frac{V_{FS}}{R_T} = \frac{V_S \times (R_B - R_{FS} \times n)}{R_B \times (2R_{FS} + R_T) + R_{FS} \times R_T \times n}. \quad \textbf{(10)}$$

Solving Equation 10 for R_{FS} provides the failsafe resistor value necessary to keep V_{FS} positive:

$$R_{FS} = \frac{V_S - V_{FS}}{2V_{FS}/R_T + n \times (V_S + V_{FS})/R_B}. \quad \textbf{(11)}$$

For applications without a termination resistor ($R_T = \infty$), Equation 11 simplifies to

$$R_{FS} = \frac{R_B \times (V_S - V_{FS})}{n \times (V_S + V_{FS})}. \quad \textbf{(12)}$$

Figure 9 shows the values of R_{FS} and the master supply current (I_M) as functions of bus-node count. Figure 9a was created by using Equation 11, assuming a termination resistor of 120 Ω. Figure 9b was created by using Equation 12, assuming no termination. Both figures were created for a failsafe voltage of 110 mV.

Figure 9c shows the master supply current (I_M) for both cases. Despite the low-impedance load of 120 Ω, I_M in the failsafe network with termination is merely 1 mA larger than I_M in the network without termination.

Conclusion

The SN65HVD888 POLCOR transceiver provides polarity correction for cross-wired bus cables by means of debounce filtering. The filter's minimum debounce time ($t_{FS(min)}$) determines the maximum duration of consecutive bits of equal polarity, while its maximum debounce time ($t_{FS(max)}$) determines the minimum bus-idle time for a complete signal-polarity correction.

The SN65HVD888 requires polarity correction only after a power-up sequence. Once completed, the polarity status is stored within the transceiver and consistently applied to both receive and transmit data. Switching the transceiver between transmit and receive mode does not alter the polarity status.

The transceiver supports DL/T645 data rates well below 300 bps. The recommended failsafe-biasing network uses a 120-Ω termination resistor and two 1.1-kΩ failsafe-biasing resistors.

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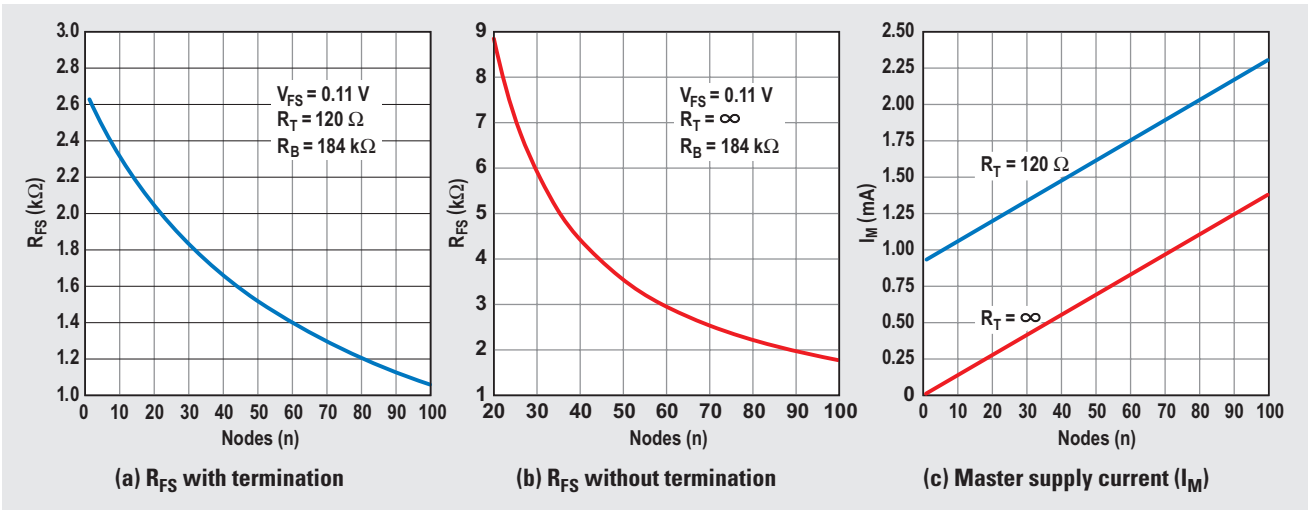
Figure 9. Effects of failsafe resistance (R_{FS}) with and without termination



Designing active analog filters in minutes

By Bonnie Baker
Senior WEBENCH® Applications Engineer

Introduction

Active analog filters can be found in almost every electronic circuit. Audio systems use filters for frequency-band limiting and equalization. Designers of communication systems use filters for tuning specific frequencies and eliminating others. To attenuate high-frequency signals, every data-acquisition system has either an anti-aliasing (low-pass) filter before the analog-to-digital converter (ADC) or an anti-imaging (low-pass) filter after the digital-to-analog converter (DAC). This analog filtering can also remove higher-frequency noise superimposed on the signal before it reaches the ADC or after it leaves the DAC. If an input signal to an ADC is beyond half of the converter's sampling frequency, the magnitude of that signal is converted reliably; but the frequency is modified as it aliases back into the digital output.

A low-pass, high-pass, band-pass, or band-stop filter can be efficiently designed with the WEBENCH® Filter Designer software from Texas Instruments (TI). This application replaces TI's FilterPro™ and the former National Semiconductor's WEBENCH Active Filter Designer software. It uses the approach of these programs and formulas verbatim when generating active filters. But it goes beyond these two programs by allowing in-depth adjustments to filter variables, optimizing the filter, finding appropriate TI operational amplifiers (op amps) for the filter circuits, and providing SPICE simulation capability.

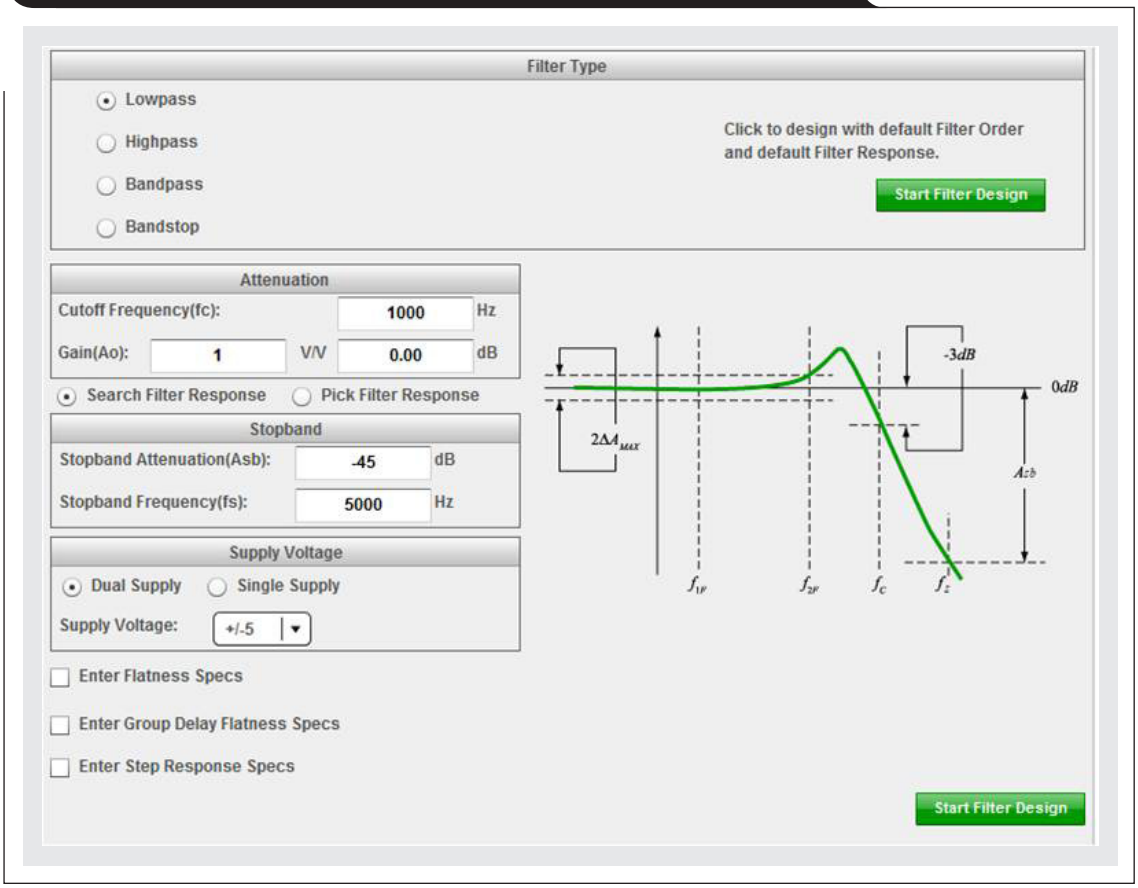
Key design parameters for a low-pass analog filter

The frequency-domain specifications of a low-pass analog filter include four fundamental parameters:

- fc, the filter's –3-dB cutoff frequency
- Ao, the gain of the filter
- Asb, the stop-band attenuation
- fs, the frequency of the intercept to the stop-band attenuation

These parameters are shown in WEBENCH Filter Designer's Filter Type window in Figure 1. The frequency span from DC to the cutoff frequency (fc) is the pass-band

Figure 1. WEBENCH® Filter Designer's key analog-filter parameters

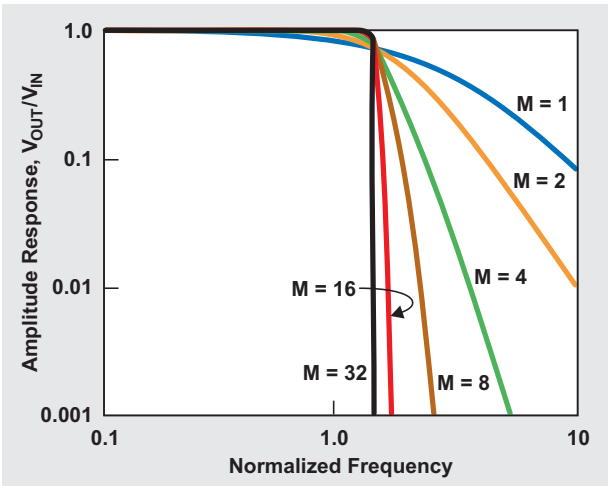


region. The magnitude of the response in the pass band is Ao in Figure 1. The response in the pass band can be flat with no ripple, as it is with a Butterworth or Bessel filter. Conversely, a Chebyshev filter has a ripple up to the cutoff frequency. The magnitude of the ripple error of a Chebyshev filter is $2\Delta A_{MAX}$.

As the response of the filter goes beyond fc, it falls through the transition band to the stop-band region. The filter approximation (Butterworth, Chebyshev, Bessel, etc.) determines the bandwidth of the transition band and the order (M) of the filter. The number of poles in the transfer function determines the filter order. For instance, if a filter has three poles in its transfer function, it is a third-order filter.

Generally, the transition band becomes smaller when more poles are used to implement the filter design, as shown in Figure 2 for a Butterworth low-pass filter. Ideally, a low-pass, anti-aliasing filter should perform with a "brick-wall" style of response, with an extremely small transition band. Practically speaking, this is not the best approach for an anti-aliasing solution. With active-filter design, every two poles require an op amp. For instance, a 32nd-order filter requires 16 op amps, 32 capacitors, and up to 48 resistors.

Figure 2. Increased number of poles in Butterworth filter creates sharper rolloff



Analog filter-approximation types

Figure 3 shows the low-pass-filter types available in the Solutions window from the WEBENCH Filter Designer's Visualizer screen. This screen appears after the user clicks on the Start Filter Design button shown in Figure 1.

The more popular filter-approximation types are the Butterworth, Chebyshev, and Bessel. Filters can be identified by examining amplitude versus frequency domain and amplitude versus time domain.

Butterworth filter

The transfer function of a Butterworth filter consists of all poles and no zeroes and is represented by

$$\frac{V_{OUT}}{V_{IN}} = \frac{Ao}{a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} \ldots a_{n-1} s^2 + a_n s + 1}.$$

Figure 3. Low-pass-filter types in WEBENCH® Filter Designer

Solutions

Solutions: (7 found)

Select	Filter Response	Color	Order	Max Q	Att (dB)	Passband Ripple (dB)	Group Delay (usec)	Group Delay Flatness (usec)	Settling Time (usec)	Step Response Overshoot (%)
Select	Transitional Gaussian to 6dB	Green	4	1.32	-47.59	0.380	367.676	9.147	1489.356	0.79
Select	Linear Phase 0.05°	Blue	4	1.07	-46.41	0.437	361.873	2.088	1490.866	1.06
Select	Butterworth	Black	4	1.31	-55.91	0.002	448.464	32.576	2717.626	10.82
Select	0.2dB Chebyshev	Yellow	4	2.435	-60.15	0.199	816.477	405.321	4215.482	15.20
Select	Linear Phase 0.5°	Magenta	4	1.34	-48.78	0.317	379.450	16.052	1529.731	1.78
Select	Bessel	Red	5	0.92	-49.26	0.446	385.154	1.83e-4	1169.675	0.77
Select	Transitional Gaussian to 12dB	Aqua	5	1.52	-52.56	0.562	400.004	13.012	1521.612	0.00

Figure 4 shows that the response of a fourth-order, low-pass Butterworth filter is flat in the pass-band portion. The technical term for this characteristic is *maximally flat*. Later it will be shown that the rate of attenuation in the transition band is not as good as with the Chebyshev filter.

Figure 5 shows that the step response of the same fourth-order Butterworth filter has some overshoot and ringing in the time domain. If the filter order were higher, this overshoot would also be higher. If this filter is used after a multiplexer, its settling time should be considered.

Figure 4. Frequency response of fourth-order, low-pass Butterworth filter

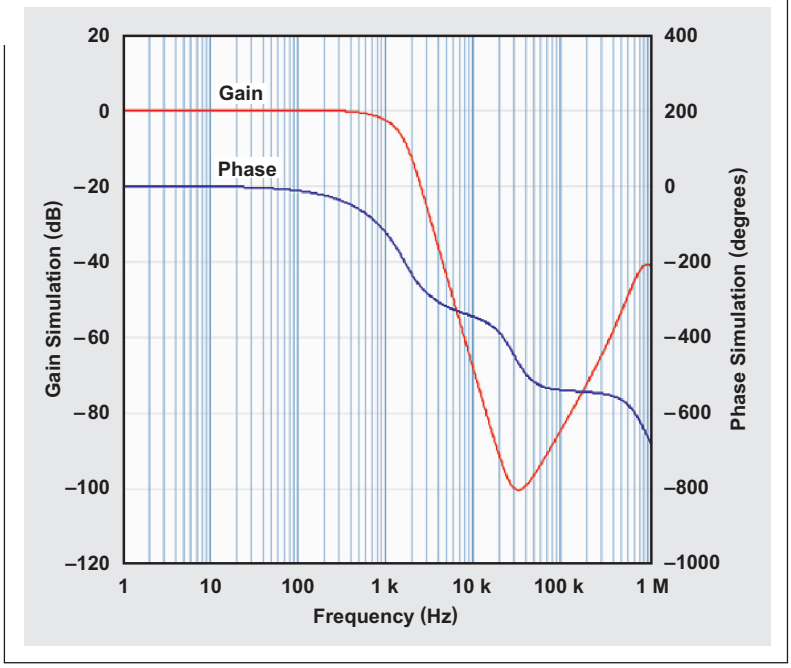
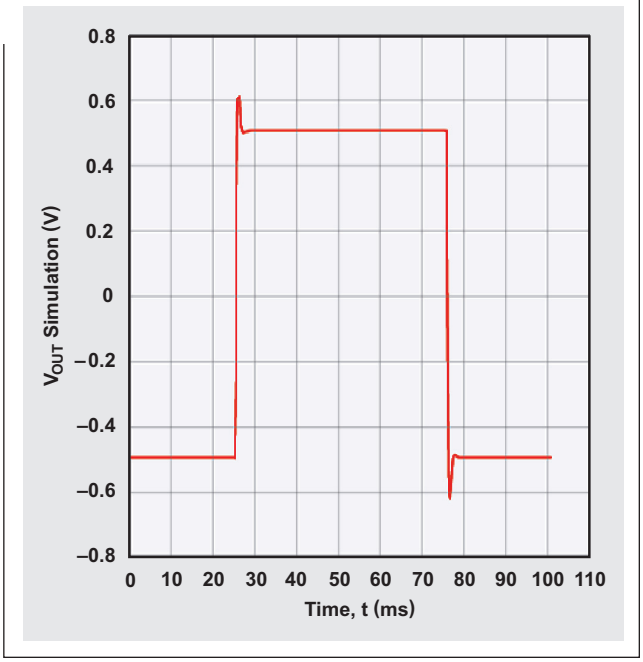


Figure 5. Step response of fourth-order, low-pass Butterworth filter



Chebyshev filter

The transfer function of the Chebyshev filter is similar to the Butterworth filter only in that it has all poles and no zeroes:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Ao}{a_0 + a_1 s + a_2 s^2 + \ldots a_{n-1} s^{n-1} + s_n}$$

Figure 6 shows that the frequency response of a fourth-order, low-pass Chebyshev filter has a 0.2-dB ripple in the pass-band region. The pole placement in the circuit design determines this ripple. In general, an increase in ripple magnitude lessens the width of the transition band.

The ripple magnitude of $2\Delta A_{MAX}$ (Figure 1) theoretically can be as large or as small as desired. A high-ripple magnitude generally results in more error in the pass-band region but a faster attenuation in the transition band.

The rate of attenuation in the transition band is steeper than for a Butterworth filter. For instance, to meet the transition bandwidth of a third-order Chebyshev with a 0.5-dB ripple, a fourth-order Butterworth filter is required. Although with the Chebyshev filter there is ringing in the pass-band region, the stop band is devoid of ringing.

The step response of a fourth-order, low-pass Chebyshev filter with a 0.2-dB ripple has a fair degree of overshoot and ringing (Figure 7).

The overshoot and ringing phenomena are a consequence of the phase response in the frequency domain. Recall that the Fourier analysis of a step response (or square wave) shows that a square wave can be constructed by adding odd harmonic sinusoidal signals. Consequently, the higher frequencies from the step input arrive at the output of the filter before the lower frequencies. This is called a *distortion group delay*. This group delay in seconds is calculated as

$$\frac{\text{Change in phase/Change in frequency}}{360}.$$

Figure 6. Frequency response of fourth-order, low-pass Chebyshev filter

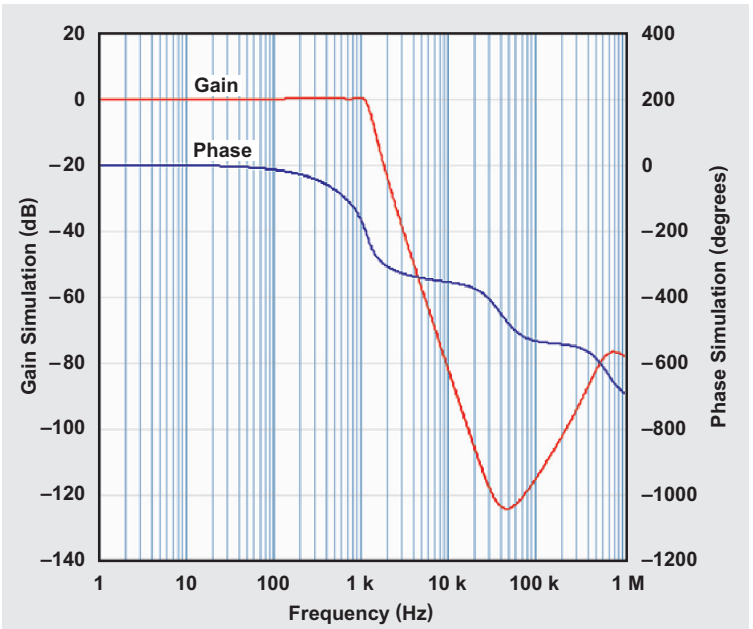
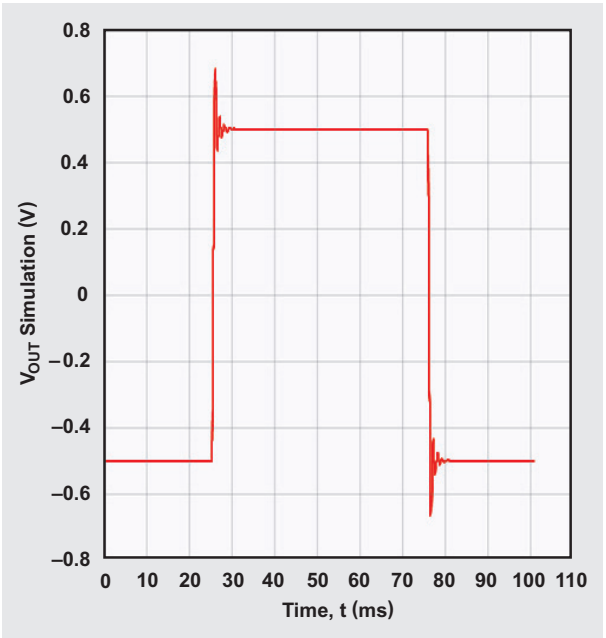


Figure 7. Step response of fourth-order, low-pass Chebyshev filter



Comparison of filter-approximation types

For low-pass filters, the type of filter approximation affects the frequency response before and beyond the filter's cut-off frequency. Since the inverse of frequency (in hertz) is seconds, the filter type inversely impacts the time domain. Table 1 compares low-pass Butterworth, Chebyshev, and Bessel filters in the frequency domain (pass-band and transition regions) and the time domain (step response).

Table 1. Comparison of filter-approximation types

FILTER TYPE	PASS BAND	TRANSITION REGION	STEP RESPONSE
Butterworth	Maximally flat magnitude response in the pass band	Steeper than Bessel, but not as good as Chebyshev filter	Some overshoot and ringing, but less than the Chebyshev filter
Chebyshev	Ripple in the pass band	Steeper than Butterworth and Bessel filters	Fair degree of overshoot and ringing
Bessel	Flat magnitude response in the pass band	Slower than Butterworth and Chebyshev filters	Very little overshoot or ringing as compared to Butterworth and Chebyshev filters

Getting started with WEBENCH Filter Designer

TI's Filter Designer lets engineers design, optimize, and simulate complete multistage active-filter solutions within minutes. Optimized filter designs can be created with a selection of TI op amps and passive components from TI's vendor partners.

The Filter Designer software can be accessed at www.ti.com/webenchfilters-aaj along with a quick tutorial. A filter can be selected from low-pass, high-pass, band-pass, and band-stop types. Performance constraints for attenuation, group delay, and step response can be specified if desired, and there are a variety of filter responses to choose from, such as Chebyshev, Butterworth, Bessel, linear phase, and transitional Gaussian. The filter response best suited for the design is determined by optimizing for pulse response, settling time, lowest cost, pass-band ripple, and stop-band attenuation.

Sallen-Key or multiple feedback topologies are design options for each filter stage, and the best op amps for the design are chosen by evaluating gain bandwidth versus current versus cost and other parameters. The resistor/capacitor tolerances can be specified as ideal, 0.5, 1, 2, 5, 10, or 20%. Experimenting with user-defined capacitor seed values adjusts the range of resistor values in the filter design. Filter topologies can also be optimized for sensitivity, lowest cost, and smallest footprint.

The design can then be analyzed by running SPICE electrical simulation with the option for a closed-loop frequency response, a step response, or a sine-wave response. The input conditions of these options can be adjusted in order to evaluate different output results.

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Driving solenoid coils efficiently in switchgear applications

By Sanjay Pithadia
Senior Analog Applications Engineer

Introduction

A primary objective of all power systems is to maintain a very high level of continuity of service and, when intolerable conditions occur, to minimize their extent and the outage time. Loss of power, voltage dips, overcurrents, and overvoltages will occur because it is impossible to avoid the consequences of natural events, physical accidents, equipment failure, or misoperation owing to human error. A combination of devices used to protect electrical equipment from these events is known as *switchgear*. Solenoids and relays are integral parts of any switchgear equipment, as they connect/disconnect the mains to/from the protected equipment through coil energization and contacts. This article touches upon the characteristics of solenoid coils typically found in relays, contactors, and valves. It also covers methods of driving them and explains a trend in efficient driving. This article also shows some example switchgear application circuits.

Overcurrent-protection devices, such as circuit breakers, are used to protect conductors from excessive current flow. These protective devices are designed to keep the flow of current in a circuit at a safe level to prevent the circuit conductors from overheating. Contactors are primarily used to make (connect) or break (disconnect) contact in the conducting element. They are used in systems where the break-and-make connection is either frequent or unchanged for long time periods.

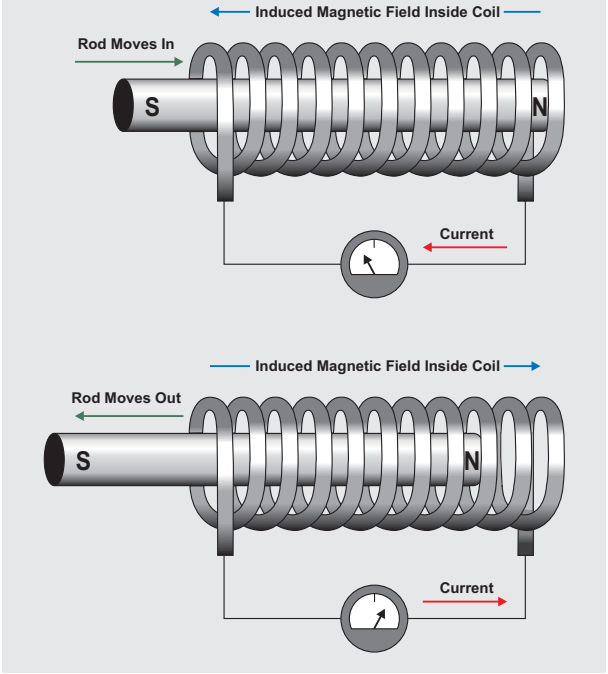
To protect a circuit against heavy currents, a protective device must determine when a fault condition develops and automatically disconnect the electrical equipment from the source. An overcurrent-protection device must be able to recognize the difference between overcurrents and short circuits and to respond in the proper way. Slight overcurrents can be allowed to continue for some period of time; but, as the current magnitude increases, the protection device must respond faster. For instance, short circuits must be interrupted instantaneously.

Characteristics of solenoid coils

Electromechanical solenoids consist of an electromagnetically inductive coil wound around a movable steel or iron slug termed the *armature*. The coil is shaped such that the armature can be moved in and out of its center, altering the coil's inductance and thereby becoming an electromagnet (Figure 1). The armature is used to provide a mechanical force to some mechanism.

A solenoid's main electrical characteristic is that of an inductor, in that it possesses inductance, which is the characteristic that opposes any change in current. This is why current does not immediately reach a maximum level when a solenoid is energized. Instead, the current rises at a steady rate until it is limited by the DC resistance of the solenoid. An inductor (in this case a solenoid) stores energy in the form of a concentrated magnetic field. Whenever current is present in a wire or conductor, a magnetic field, however small, is created around the wire. With many turns of wire wound into a coil, such as in a solenoid, the magnetic field becomes very concentrated. This electromagnet can be used to control a mechanical valve via an electrical signal. As soon as the solenoid is energized, the current increases, causing the magnetic field to expand until it becomes strong enough to move the armature. The armature movement increases the concentration of the magnetic field as the armature's own magnetic mass moves farther into the magnetic field. Remember, a magnetic field changing in the same direction of the current creating it induces an opposing voltage into the windings. Because the magnetic field quickly expands when the armature strokes, it causes a brief reduction in the current through the solenoid windings. After the armature strokes, the current continues on its normal upward path to its maximum level. The result is

Figure 1. Working of a solenoid



the current waveform in Figure 2. Notice the prominent dip in the rising portion of the current waveform.

Driving the solenoid coil: Voltage or current drive?

As mentioned earlier, the armature of a solenoid is used to provide a mechanical force to some mechanism. The force applied to the armature is proportional to the coil's change in inductance with respect to the armature's change in position. The same force is also proportional to the current flowing through the coil (based on Faraday's law of induction). Equation 1 determines the force that a solenoid electromagnet will exert on a passing charge:

$$\text{Force} = Q \times V \times (\text{Magnetic constant} \times N \times I), \quad (1)$$

where Q is the charge of the passing point charge; V is the velocity of the point charge; the magnetic constant is $4\pi \times 10^{-7}$; N is the number of turns in the solenoid coil; and I is the current running through the solenoid. This shows that the electromagnetic force of a solenoid is directly related to the current.

Traditionally, voltage drive is used to drive the solenoid coils; hence, a continuous power is consumed in the coil. A negative effect of this power consumption is the heating of the coil and, in turn, the entire relay. The coil temperature is a result of ambient temperature; self-heating due to the coil's power consumption of V × I; heating induced by the contact system; magnetization losses due to eddy currents; and other heat sources, such as components in the vicinity of the relay.

Due to coil heating, the coil resistance increases. The resistance at elevated temperature is expressed by Equation 2:

$$R_{Coil\_T°C} = R_{Coil\_20°C}\left[1 + k_{R\_T}(T°C - 20°C)\right], \quad (2)$$

where $R_{Coil\_20°C}$ is the 20°C value for resistance, and k_{R_T} is the thermal coefficient of copper, equal to 0.0034 per degree Celsius. Based on $R_{Coil\_20°C}$, typically given in the datasheet of a solenoid coil, the worst-case coil resistance at high temperature can be calculated. During circuit design, care has to be taken that the calculations are made for worst-case conditions, such as the highest possible coil temperature at the operating pick-up voltage.

Another point to note is that for a given coil, the pick-up current remains the same at any condition. The pick-up current depends on the pick-up voltage and the coil resistance ($I_{Pick\text{-}up} = V_{Pick\text{-}up}/R_{Coil}$). Most relay coils are made of copper wire. Due to the increase in coil temperature, the coil resistance increases as per Equation 2. Hence, the pick-up voltage for the hot coil should be higher to generate the required pick-up current. For example, if a 12-VDC relay's pick-up voltage is 9.6 VDC and the coil resistance is 400 Ω at 20°C, then $I_{Pick\text{-}up}$ = 24 mA. When the coil temperature is increased to 40°C, the coil resistance increases to 432 Ω. Hence the pick-up voltage will be 10.36 VDC. (The pick-up current remains the same.) In other words, an increase in temperature by 20°C increases the pick-up voltage by 0.76 VDC. In relays operating with higher duty cycles, the pick-up voltage may increase slightly for each successive cycle due to the coil's temperature rise. Figure 3 shows that the user may have to overdesign the coil if voltage drive is used.

Figure 2. Solenoid current

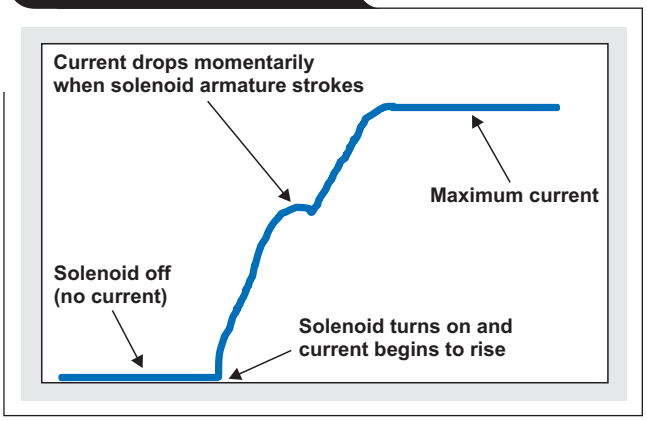
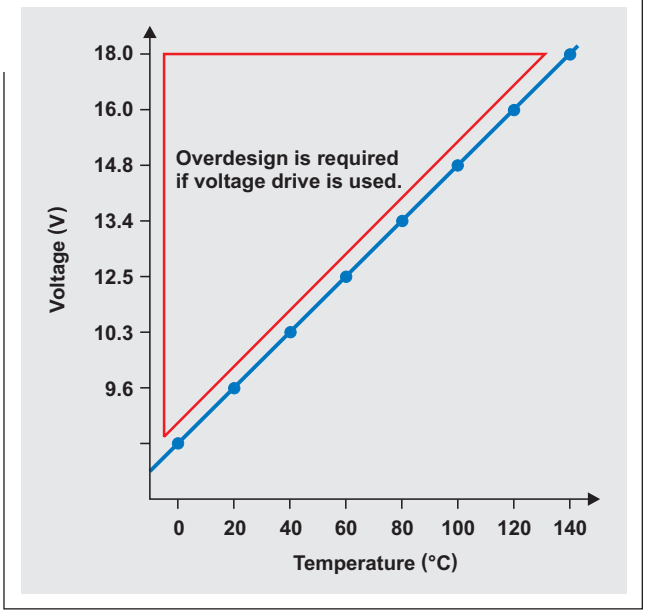


Figure 3. Overdesign for solenoid voltage drive



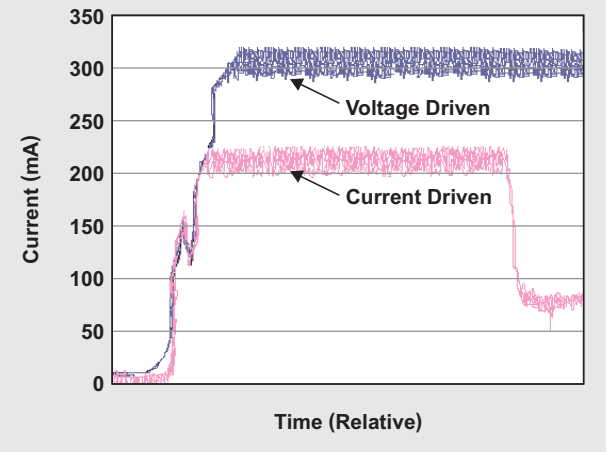
In short, voltage drive forces overdesign because current varies with variations in coil resistance, temperature, supply voltage, and the like. So using current drive is optimal for many devices with solenoids.

Optimizing power consumption

Closing a relay or valve requires a lot of energy. The instantaneous current that activates the solenoid actuator, called the *peak current* (I_{Peak}), can be high. However, once the relay or valve is closed, the current required to keep it in that condition, called the *hold current* (I_{Hold}), is significantly less than the peak current. Typically, the hold current is less than the peak current: $I_{Hold} << I_{Peak}$.

When voltage drive is used, the current flowing through the solenoid coil is continuous and higher than when current drive is used (Figure 4). Unlike voltage drive, current drive requires no margin for parameter changes caused by temperature or solenoid-resistance variations. The design requires separate values for peak current, which may be in the range of amperes, and steady-state hold current, which may be only 1/20 of the peak-current value.

Figure 4. Solenoid current with voltage drive and current drive



Current-control implementations for driving a solenoid coil

Traditionally, the solenoid coil is driven directly through the general-purpose inputs/outputs (GPIOs) of the microcontroller (MCU) (Figure 5a). The coil is activated via a switch controlled by a GPIO from the MCU. A new driving system has been developed that uses pulse-width modulation (PWM) of the waveform (Figure 5b). The coil is activated via a switch controlled by a PWM from the MCU, and the duty cycle determines the average current through the coil. For this article, the Texas Instruments DRV110, a power-saving solenoid controller with integrated supply regulation, was used (Figure 5c). This DRV110-based system was designed to regulate the current with a well-controlled waveform to reduce power dissipation. After the initial ramping, the solenoid current is kept at a peak value to ensure correct operation, after which it is reduced to a lower hold level to avoid thermal problems and reduce

Figure 5. Coil-driving methods

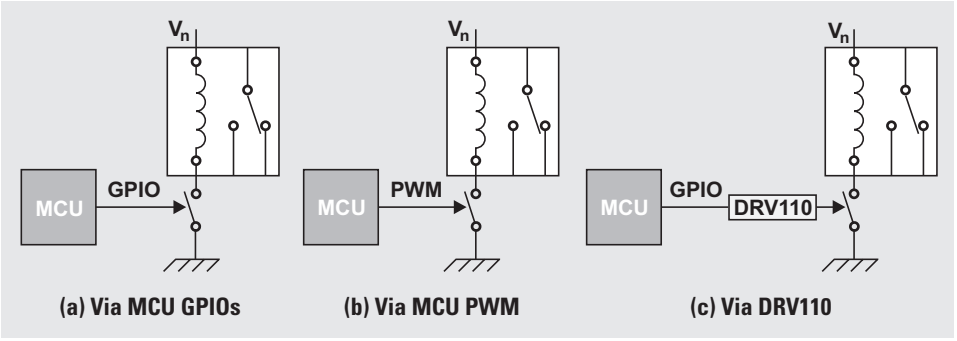
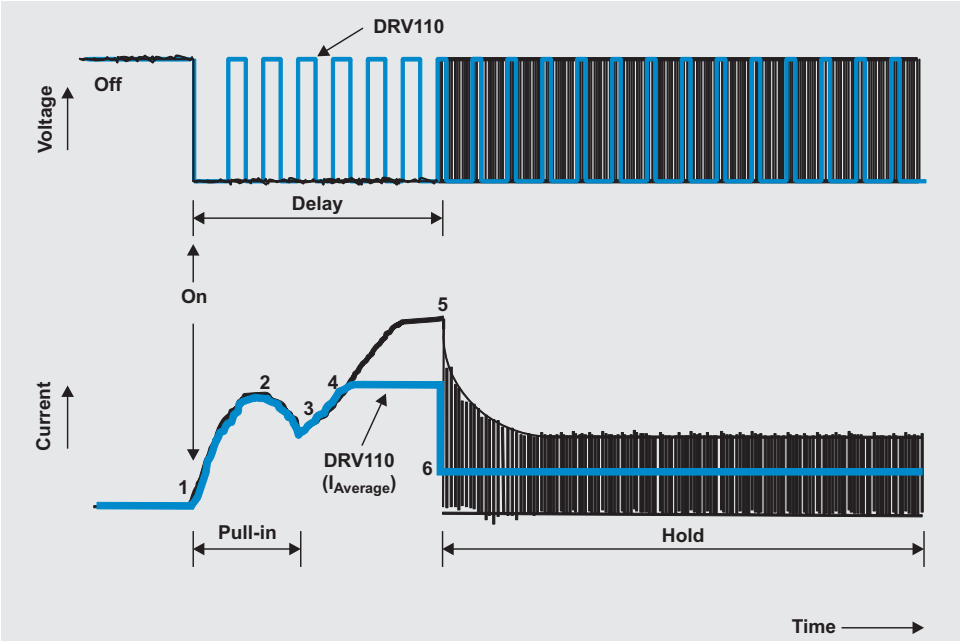


Figure 6. Operation of conventional driver versus DRV110



Step 1: Relay driver is enabled.

Step 2: Start of mechanical movement. This movement generates a back-EMF that counters the solenoid flux, reducing current.

Step 3: End of mechanical movement. (Current increases again.)

Step 4: DRV110 limits pull-in current, saving power.

Steps 5 and 6: Hold mode is entered after a delay. The DRV110's hold-current value is the lowest possible.

power dissipation. The graphs given in Figure 6 compare the operation of a conventional driver with that of the DRV110. Note that other methods reduce voltage but need to have an overhead to guarantee that the hold current is always maintained across temperature.

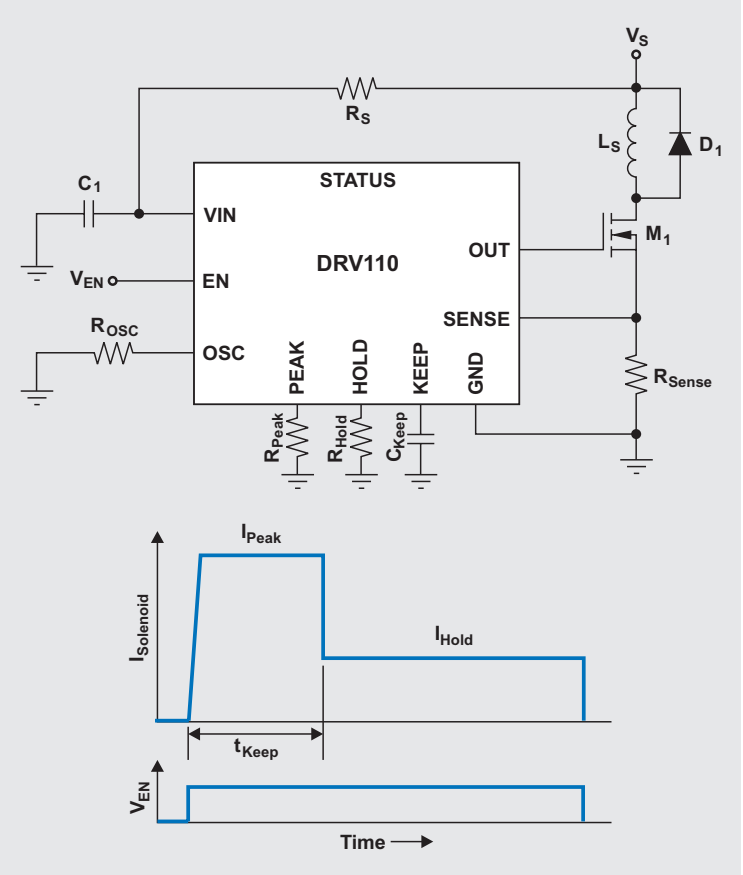
A typical application circuit based on the DRV110 is shown in Figure 7. The DRV110 controls the current through the solenoid (L_S), also shown in Figure 7. Activation starts when the EN pin voltage is pulled high, either internally or by an external driver. In the beginning of activation, the DRV110 allows the load current to ramp up to the peak value (I_{Peak}) and regulates it there for time t_{Keep} before reducing it to I_{Hold}. The load current is regulated at the hold value as long as the EN pin is kept high. The initial current ramp-up time depends on the inductance and resistance of the solenoid. Once the EN pin is driven to GND, the DRV110 allows the solenoid current to decay to zero.

Determining I_{Peak} and I_{Hold} of the DRV110

The activation (peak) current of the DRV110 is determined by the coil's ON resistance and the pick-up voltage required by the relay. This resistance value at maximum temperature ($R_{Coil\_T(max)}$) and the relay nominal operating voltage (V_{nom}) can be used to calculate the I_{Peak} value required at maximum temperature:

$$I_{Peak} = \frac{V_{nom}}{R_{Coil\_T(max)}} \quad (3)$$

Figure 7. Typical application circuit for DRV110 and solenoid's current waveform



The hold current of the DRV110 is determined by the ON resistance of the coil and by the voltage required to keep the relay from dropping out. To keep a relay from dropping out, manufacturers give recommended voltage values in their datasheets; however, some margin for vibration and other contingencies should be added to these. Many relay manufacturers give 35% of the nominal voltage as a safe limit. Assuming this to be enough, the $R_{Coil\_T(max)}$ value and the relay nominal operating voltage (V_{nom}) can be used to calculate the I_{Hold} value that works over the temperature:

$$I_{Hold} = \frac{0.35 \times V_{nom}}{R_{Coil\_T(max)}} = 0.35 \times I_{Peak} \quad (4)$$

Examples of switchgear applications

Overload protection will cause a device to break the circuit connection if the load current exceeds the rated current of the device for a specified duration. The protection circuit implemented in Figure 8 derives the enable (EN) signal by measuring current as well as voltage. (To simplify Figures 8–10, the DRV110 pin connections for OSC, PEAK, HOLD, and KEEP are not shown.)

A magnetic contactor needs a current to be passed through the coil to move the contacts into a closed or open position. Figure 9 shows the implementation of an RMS-voltage-sensing circuit in a contactor system that uses the DRV110.

Figure 8. Overload protection

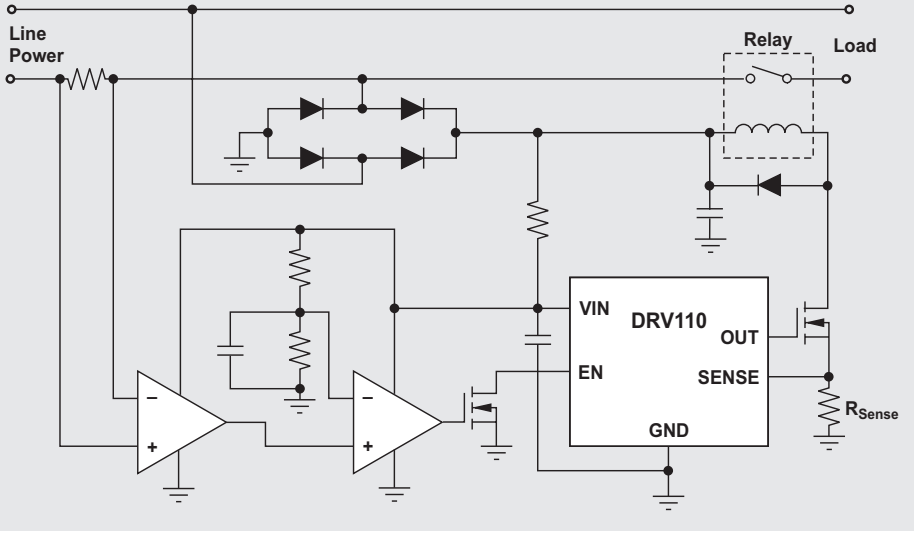


Figure 9. Magnetic-contactor system with RMS-voltage sensing

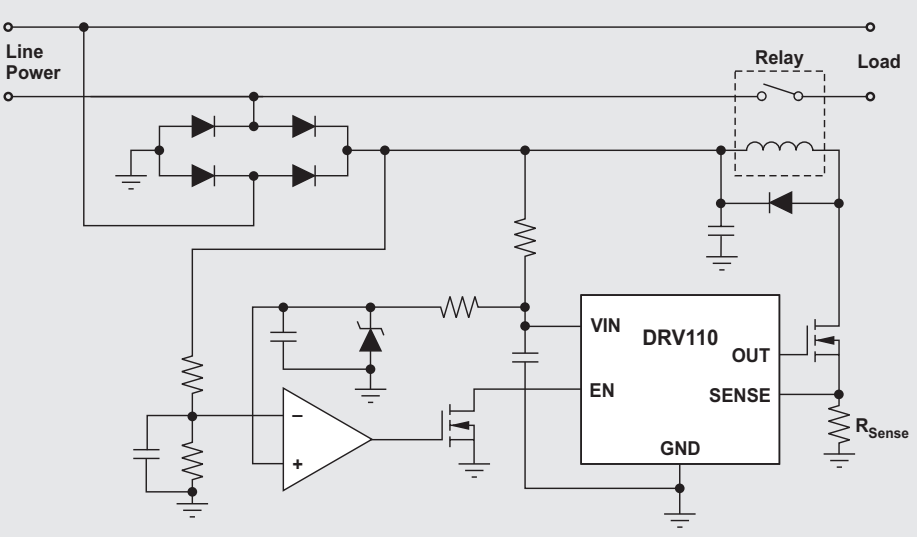
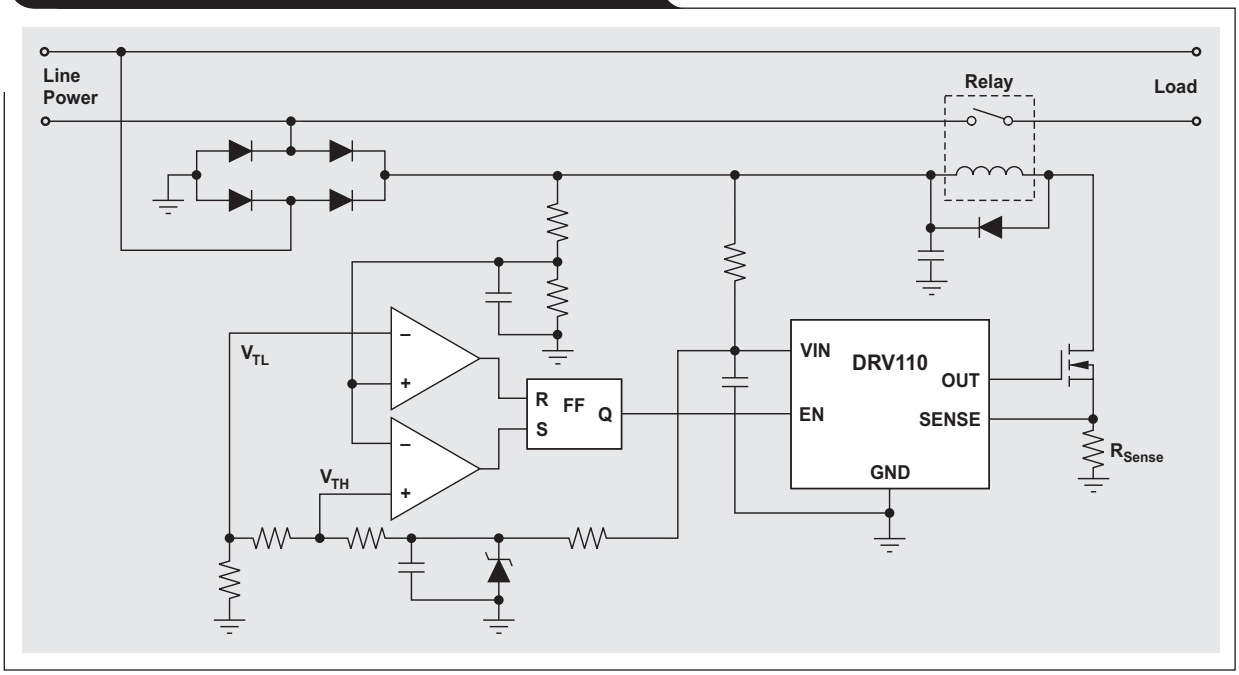


Figure 10. Undervoltage and overvoltage protection



Undervoltage and overvoltage protection also can be implemented by using the DRV110 (Figure 10). Two comparators are used to measure the high and low threshold voltages. Based on the outputs of each comparator, the SR flip-flop sends an enable (EN) signal to the DRV110.

Conclusion

There are many benefits to using a power-saving solenoid controller with integrated supply regulation. To achieve energy savings, current regulation is the most accurate way of controlling actuator force. No margin needs to be added because the system is immune to variations in coil resistance, supply voltage, and temperature. System reliability is also improved because the solenoid action is repeatedly optimal. Finally, system cost is optimized. With energy accurately controlled, coils can be overdriven to get acceptable performance from a smaller, cheaper coil.

Reference

1. "Power saving solenoid controller with integrated supply regulation," DRV110 Datasheet. Available: www.ti.com/slvsba8-aaj

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