

# When is the JESD204B interface the right choice?

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## Introduction

Anyone involved in high-speed data-capture designs that use an FPGA has probably heard the buzzword for the new JEDEC standard: JESD204B. Recently a lot of engineers have contacted Texas Instruments requesting information on the JESD204B interface, including how it works with an FPGA and how it will make their designs easier to execute. So what is the JESD204B interface all about? This article discusses the evolution of the JESD204B standard and what it means to a systems design engineer.

## What led to the JESD204B standard?

About ten years ago, designers of high-speed data converters switched from using the traditional single-ended CMOS interface to using a differential LVDS interface because the latter enabled higher data rates. (The CMOS interface is limited to about 200 Mbps.) The LVDS interface also improved noise coupling on signal lines and power supplies. The drawback of this interface was higher power consumption at lower sampling speeds. This gave the CMOS interface a reason for existence, and it is still being used today.

But with the evolution of analog-to-digital converters (ADCs) requiring faster sampling rates and higher channel density, the industry was demanding a faster, more power-efficient digital interface than parallel LVDS. In order to overcome this challenge, a true serial interface called JESD204 was developed and approved by JEDEC in April 2006. The JESD204 interface is defined as a single-lane, high-speed serial link connecting single or multiple data converters to a digital logic device with data rates of up to 3.125 Gbps. It needs a common frame clock sent to the converter and the FPGA to synchronize the frames.

Supporting only one lane and one serial link, JESD204 was soon viewed as not quite as useful as initially hoped, so in April 2008 the standard was revised to JESD204A. JESD204A extended support for multiple aligned lanes and multipoint links, but the maximum speed was still limited to 3.125 Gbps. This drove the development in July 2011 of JESD204B, which promises to address several different system-design challenges. Besides drastically increasing the supported data rates from 3.125 Gbps to 12.5 Gbps, it also greatly simplifies multichannel synchronization by adding the deterministic latency feature.

## What is the JESD204B standard?

JESD204B supports interface speeds of up to 12.5 Gbps, uses a device clock instead of the previously used frame clock, and has three different subclasses. Subclass 0 is backward-compatible with JESD204A except with higher speeds, and it does not support deterministic latency. Furthermore, the SYNC signal has special timing requirements for error reporting (Figure 1). Subclass 1 uses synchronization signal SYSREF to initiate and align the local multiframe clocks across devices (Figure 2). This

Figure 1. JESD204B Subclass 0 interface

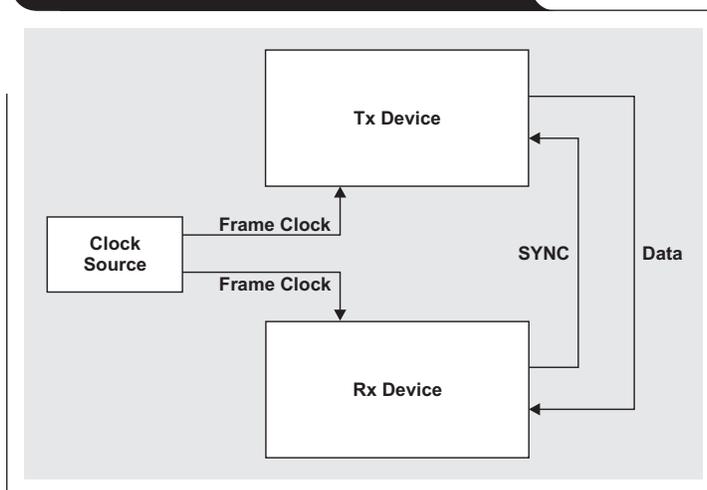
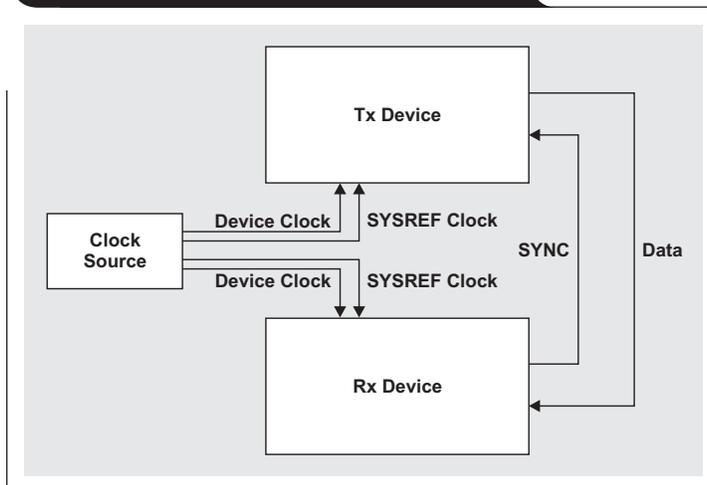


Figure 2. JESD204B Subclass 1 interface



synchronizes data transmission and achieves a known, deterministic latency across the digital link. Subclass 2 uses the SYNC signal for that same purpose (Figure 3). Due to SYNC timing constraints, Subclass 2 typically is employed for data rates lower than 500 MSPS. For speeds higher than 500 MSPS, Subclass 1 with an external SYSREF clock is commonly preferred.

JESD204B-compliant receivers are outfitted with an elastic buffer that is used to compensate for skew across serializer/deserializer (SerDes) lanes, which simplifies board layout. This elastic buffer stores the data until the data from the slowest lane arrives. It then releases the data from all lanes simultaneously for digital processing. This skew management is possible because the data clock is embedded in the serial data stream.

### Why care about the JESD204B interface?

Since JESD204B-compliant data converters serialize and transmit output data at a much higher rate than with previous interfaces, the number of pins required on the data converters as well as on processors or FPGAs is drastically reduced, translating to smaller package sizes and lower cost. However, the biggest benefits from the reduced pin count may be a much simpler layout on the printed circuit board (PCB) and easier routing because there are much fewer lanes on the board.

Layout and routing are further simplified by the reduced need for skew management, which is made possible by the data clock now being embedded in the data stream and the presence of the elastic buffer in the receiver. Hence, the need for trace squiggles to match lengths is eliminated. The JESD204B standard also allows longer transmission distances. Relaxed skew requirements enable logic devices to be placed much farther from data converters to avoid any impact on sensitive analog parts.

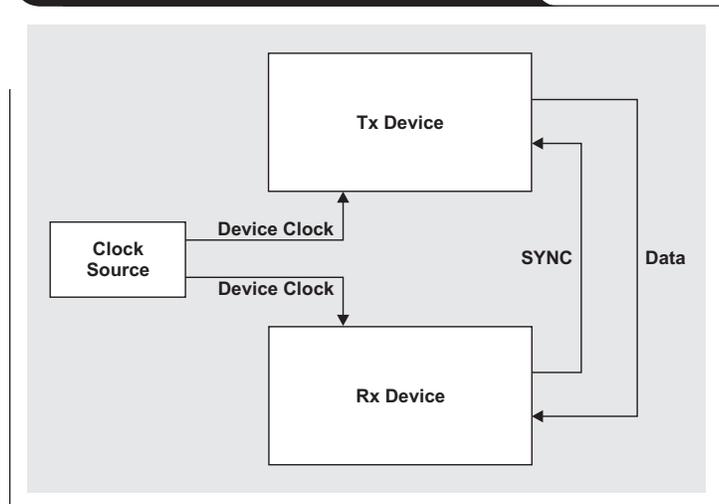
Additionally, the JESD204B interface is adaptable to different resolutions of data converters. This removes the need for physical redesign of transceiver/receiver (Tx/Rx) boards (logic devices) for future ADCs and digital-to-analog converters (DACs).

### Does this mean the end for the LVDS interface?

The CMOS interface provides lower power consumption for data converters with lower data rates, while the JESD204B interface offers a few benefits over the traditional LVDS interface. So does the LVDS interface have any chance of survival?

The simple answer is yes. While the JESD204B standard has simplified multichannel synchronization by using

**Figure 3. JESD204B Subclass 2 interface**



deterministic latency, there are applications that require minimal latency (and, in an ideal world, no latency). These applications (for example, aerospace applications like radar) need an immediate response to an action or detection. Any possible delay must be minimized. For these applications, the LVDS interface should be considered, since the JESD204B-compliant data converter's delay in serializing the data is omitted.

### Conclusion

This article has discussed the evolution of the JEDEC JESD204B standard and has explained the many benefits of using this type of interface, including faster data rates, simplified PCB layout, smaller package sizes, and lower cost. It is hoped that the reader now understands the JESD204B-based system a little better.

### References

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