Analog Applications Journal

First Quarter, 2016

Contents

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Introduction

The *Analog Applications Journal* (AAJ) is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they relate to the following applications:

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Using op amps to reduce near-field EMI on PCBs

By Todd Toporski
Analog Applications

Introduction

Automotive, industrial, medical, and many other applications use sensitive analog circuits that must perform their function while remaining immune to noise disturbances in their local environment. Many of these disturbances occur on nearby "noisy" circuits located on the same printed circuit board (PCB), while other interference can be picked up by cable interfaces that couple noise onto the PCB and its circuits.

One of the best ways to reduce electromagnetic interference (EMI) on PCB designs is through intelligent use of operational amplifiers (op amps). Unfortunately, op amps are often overlooked as a tool for reducing EMI in many applications. This may be due to the perception that op amps are susceptible to EMI and that extra steps must be taken to enhance their immunity to noise. While this is true of many older devices, designers may not be aware that newer op amps often have superior immunity performance over previous generations. Designers also may not understand or consider the key benefits that an op amp circuit can provide for reducing noise in their system and PCB designs. This article reviews sources of EMI and discusses op amp characteristics that aid in mitigating near-field EMI on sensitive PCB designs.

EMI sources, victim circuits, and coupling mechanisms

EMI is a disturbance caused by a source of electrical noise that impacts a second electrical circuit in an unintentional and often undesirable manner. In all cases, an interfering noise signal is either a voltage, a current, electromagnetic radiation, or some combination of these three coupled from a noise source to a victim circuit.

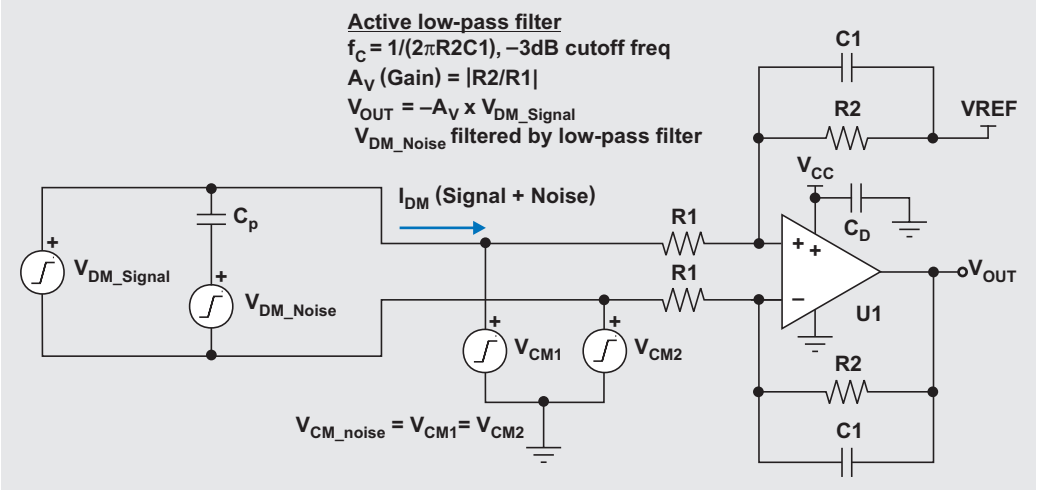
EMI is not limited to radio frequency interference (RFI). Strong sources of EMI exist below radio bands in "lower" frequency ranges, sources such as switching regulators, LED circuits, and motor drivers operating in the tens to hundreds of kilohertz range. A 60-Hz line noise is another example. Sources transfer noise to victim circuits through one or more of four possible coupling mechanisms. Three of the four are considered near-field coupling, including conducted coupling, electric-field coupling, and magnetic-field coupling. The fourth mechanism is far-field radiated coupling, in which electromagnetic energy is radiated over multiple wavelengths.

Active filtering of differential-mode noise

Active op amp filters can significantly reduce EMI and noise on a PCB within the bandwidth of the circuit, but they are underutilized in many designs. The desired differential-mode (DM) signal can be band-limited while unwanted DM noise is filtered out. Figure 1 demonstrates DM noise coupled into an input signal through parasitic capacitance (C_P). The combined signal and noise is received by a first-order active low-pass filter. The differential op amp circuit has its low-pass cutoff frequency set just above the desired signal bandwidth by R2 and C1. Higher frequencies are attenuated by 20 dB per decade. Higher-order active filters (for example, –40 or –60 dB/decade) can be implemented if more attenuation is needed.

Resistor tolerances of one percent or lower are recommended. Likewise, capacitors having very good temperature coefficient (NPO, COG) and tolerances of 5% or lower are preferred for best filter performance.

Figure 1. DM and CM input noise applied to active op amp filter



Reducing input common-mode noise

In Figure 1, common-mode (CM) noise sources also present noise at the circuit's input. CM noise can be described as a noise voltage that is common (or the same) at both op amp inputs, and is not part of the intended differential mode signal that the op amp is trying to measure or condition. CM noise can occur in a number of ways. One example is a system where the ground reference of one circuit is at a different voltage potential than a second circuit to which it is interfacing. The difference in "ground" voltages may be in millivolts or many volts, and can also occur at many different frequencies. These differences in voltages cause unintended voltage drops and flow of currents that can interfere with the connected circuitry. Cars, aircraft, and large buildings with many circuits are often susceptible to this type of interference.

A key advantage of op amps is their differential input stage architecture, and their ability to reject CM noise when configured as a differential amplifier. Common-mode rejection ratio (CMRR) is specified for every op amp, but total CMRR of the circuit must also include the effects of input and feedback resistors. Resistor variation strongly impacts CMRR. Therefore, matched resistors with tolerances 0.1%, 0.01% or better, are needed to achieve a desired CMRR for the application. While good performance is achievable using external resistors, use of instrumentation or differential amplifiers with internally-trimmed resistors is another option. For example, the INA188 is an instrumentation amp with internally trimmed resistors and high CMRR of 104 dB.

In Figure 1 the CM noise ($V_{CM\_noise} = V_{CM1} = V_{CM2}$) can be rejected by CMRR of the op amp circuit if the noise is within the active bandwidth of the circuit. The level of rejection depends on accurately-matched resistors to be chosen for R2/R1. Equation 1 can be used to determine $CMRR_{TOTAL}$, which includes the effects of resistor tolerance (R_{TOL}) and op amp CMRR as specified in the data sheet. For example, if the op amp data sheet specifies its CMRR(dB) = 90 dB, then ($1/CMRR_{AMP}$) = 0.00003. In many circuits, resistor tolerance will be the main limiting factor to achieve a target $CMRR_{TOTAL}$.

Equation 1 is derived from an equation in Reference 1 for CMRR of an ideal op amp, in which the $CMRR_{AMP}$ term is assumed to be very large (infinity). For an ideal op amp, the ($1/CMRR_{AMP}$) term is zero and $CMRR_{TOTAL}$ is based only on resistors and A_V. $CMRR_{TOTAL}$ can be converted to dB using Equation 2.

$$CMRR_{TOTAL} = \frac{\frac{1}{2}\left(1 + A_V\right)}{\frac{1}{2}\left(1 + A_V\right)\left(\frac{1}{CMRR_{AMP}}\right) + 2\left(\frac{R_{TOL}}{100}\right)} \quad (1)$$

$$CMRR_{TOTAL}\ (dB) = 20\log_{10}\left(CMRR_{TOTAL}\right) \quad (2)$$

where A_V = closed-loop gain of the op amp, R_{TOL} = % tolerance of R1 and R2 (for example, 0.1%, 0.01%, 0.001%), and $CMRR_{AMP}$ = data-sheet specification for CMRR in decimal form (not dB).

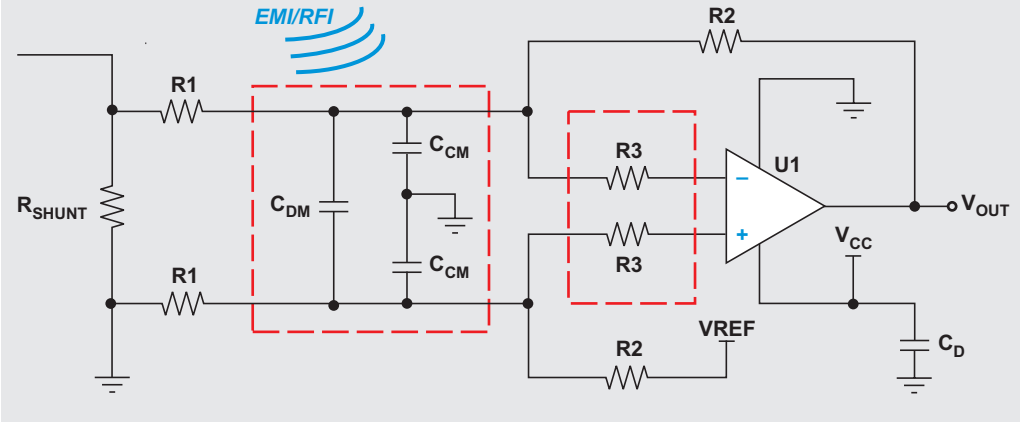
Enhancing immunity to RFI and other high-frequency EMI

As shown in previous sections, active filtering and CMRR can reliably reduce circuit noise in the device's band-limited range, including DM and CM EMI up into the MHz range. However, exposure to RFI noise above the intended operating frequency range may cause non-linear behavior in the device. Op amps are most susceptible to RFI on their high-impedance differential input stage because DM and CM RFI noise can be rectified by internal diodes (formed by p-n junctions on the silicon). This rectification creates a small DC voltage or offset that is amplified and may appear as an erroneous DC offset at the output. Depending on the accuracy and sensitivity of the system, this may create undesirable circuit performance or behavior.

Fortunately, enhancing op amp immunity (or reducing susceptibility) to RFI can be achieved using one of two methods. The first and best option is to use an EMI-hardened op amp that includes internal input filtering to reject noise in the range of tens of megahertz up to gigahertz. More than 80 TI devices exist today and can be found by searching "EMI Hardened" devices on the TI op amp parametric search engine. More details on EMI-hardened op amps can be found in References 2 and 3.

The second option is to add external EMI/RFI filters to the input of the op amp. This may be the only option if a design requires using a device that does not include internal EMI filters. Figure 2 shows a standard difference-amplifier configuration using external DM and CM filters that are targeted at higher EMI frequencies. Without input filters, the circuit gain is |R2/R1|. If passive input filters are added, R3 resistors are typically needed to prevent the C_{DM} capacitor from reducing the phase margin of the amplifier. The DM low-pass filter consists of both R1 resistors, C_{DM}, and both C_{CM} capacitors. The CM low-pass filter uses both R1 resistors and both C_{CM} capacitors.

Figure 2. Passive EMI/RFI input filters improve high frequency immunity

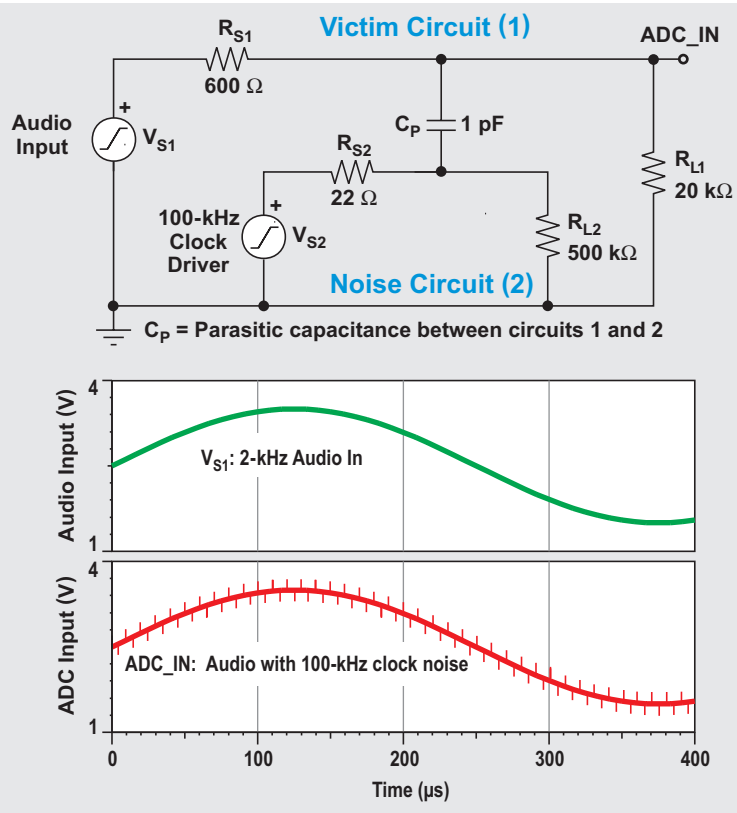


Equations for the –3-dB cutoff frequencies of the DM and CM filters (f_{C_DM} and f_{C_CM}) are shown below. f_{C_DM} is set at a frequency above the desired bandwidth of the op amp circuit, and C_{DM} is typically determined first. C_{CM} capacitors are then chosen to be at least ten times smaller than C_{DM} to minimize their impact on f_{C_DM}, and because C_{CM} capacitors are targeting higher frequencies. As a result, f_{C_CM} will be set to a frequency higher than f_{C_DM}. Note that an EMI-hardened device can be used to eliminate the components boxed in red and simplify the design.

$$f_{C\_DM} = \frac{1}{2\pi(2R1)(2C_{DM} + 2C_{CM})} \quad (3)$$

$$f_{C\_CM} = \frac{1}{2\pi(R1)(C_{CM})} \quad (4)$$

Figure 3. Clock noise source and audio victim circuit



Low output impedance reduces interference

Another important characteristic of op amps is their very-low output impedance, typically a few ohms or less in most configurations. To understand how this is beneficial for reducing EMI, consider how EMI impacts low- and high-impedance circuits.

The diagram in Figure 3 represents two circuits. The first is an audio circuit that represents the input of an analog-to-digital converter (ADC) is comprised of a 1-V_{P-P}, 2-kHz sinusoid (V_{S1}), 600-Ω source impedance (R_{S1}), and a 20-kΩ load impedance (R_{L1}). Source impedances like 600 Ω are common in audio applications for sources such as microphones and high-input impedances like 20 kΩ are common for audio ADCs. The second circuit is a 100-kHz clock source driving a 3.3-V clock signal (V_{S2}) with a series-termination resistor of 22 Ω (R_{S2}) and load impedance of 500 kΩ (R_{L2}). The high-impedance load represents the digital input of another device.

In a real system, I^2C serial bus clocks in the 100- to 400-kHz range are common around audio ADCs and circuits. Although I^2C clocks are typically driven in bursts

(not continuously), this simulation shows the possible impact during the time the clock is driving. A clock routed near a sensitive audio trace is a real possibility on high-density audio and infotainment PCB designs. For capacitive coupling to occur, it takes only a few picofarads of parasitic PCB capacitance to inject clock noise current into the victim audio signal. This is simulated using only 1 pF of parasitic capacitance, as shown in Figure 3.

How can noise be reduced in the audio circuit? As it turns out, reducing the impedance of a victim circuit is one way to reduce its susceptibility to coupled noise. For circuits with relatively high source impedance (> 50 Ω) coupled-noise can be reduced by minimizing the source impedance seen by the circuit load. In Figure 4, a non-inverting configuration of the OPA350 is added to the circuit to buffer the signal and isolate the source impedance from the load. Compared to 600 Ω, the output impedance of the op amp is very low, which significantly reduces the clock noise.

Don't forget the importance of decoupling

Adding decoupling capacitors to power supply pins is extremely beneficial in filtering high-frequency EMI noise and enhancing the immunity of the op amp circuit. All figures in this article show decoupling capacitor C_D as part of the circuit. While the subject of decoupling can get complex very quickly, a few good "rules of thumb" apply to any design. In particular, select capacitors with the following characteristics:

(a) Very-good temperature coefficient, such as X7R, NPO, or COG

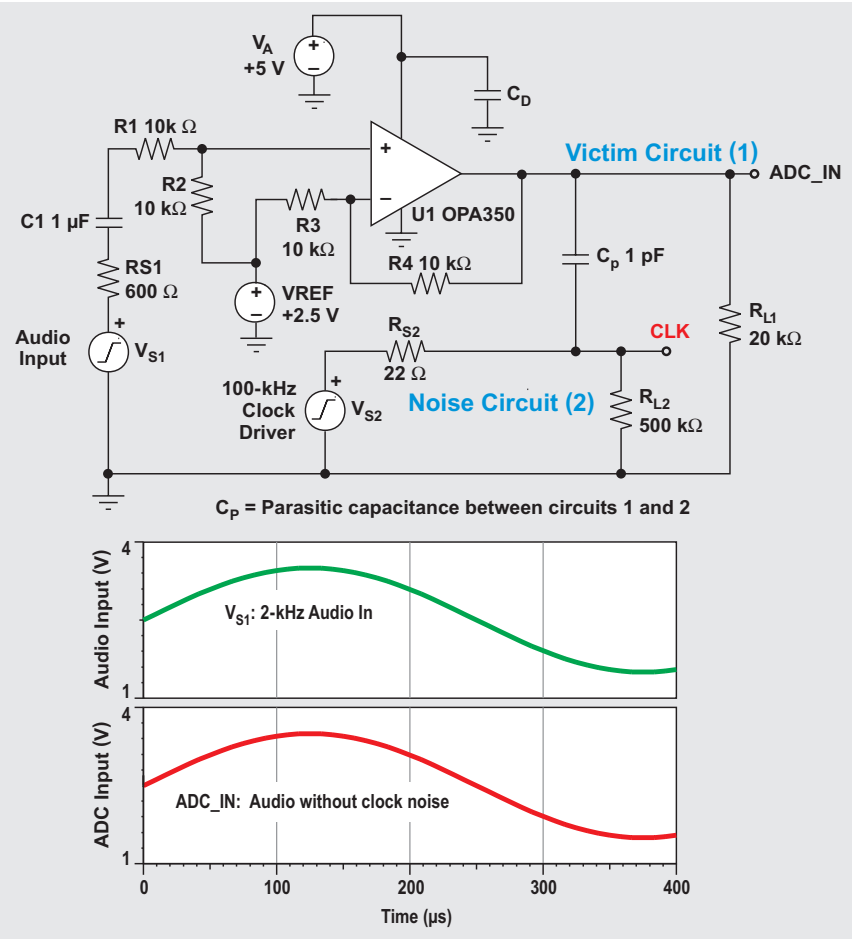
(b) Very-low equivalent series inductance (ESL)

(c) Lowest possible impedance over the desired frequency spectrum

(d) Capacitor values in the 1- to 100-nF range usually work well, but criteria (b) and (c) above are more critical than the capacitor value.

Placement and connections are just as critical as the selected capacitor. Place capacitor as close to the supply pins as possible. Connections to PCB supply/ground should be as short as possible with short traces or via connections.

Figure 4. Op amp circuit reduces EMI from clock source



Conclusion

Op amps can help to reduce near-field EMI on a PCB and enhance the system design. Here are some key points to consider for any design:

- Reduce input DM noise from cables/circuits using a well-chosen active filter configuration (Figure 1).
- Reduce input CM noise from cables/circuits by selecting an op amp with high CMRR and using precision matched resistors (Figure 1, Equations 1, 2).
- Further enhance immunity to high-frequency EMI or RFI (both DM/CM noise) by selecting an EMI-hardened device, or by using external passive EMI/RFI filters (Figure 2).
- Use the low impedance of the op amp output to reduce coupled noise when driving the signal to other circuits on the PCB.
- Finally, reduce supply noise by using a proper decoupling strategy for the op amp and all other circuits.

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Design considerations for resolver-to-digital converters in electric vehicles

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Anand Chellamuthu, *Design Engineer, Mixed Signal Automotive*

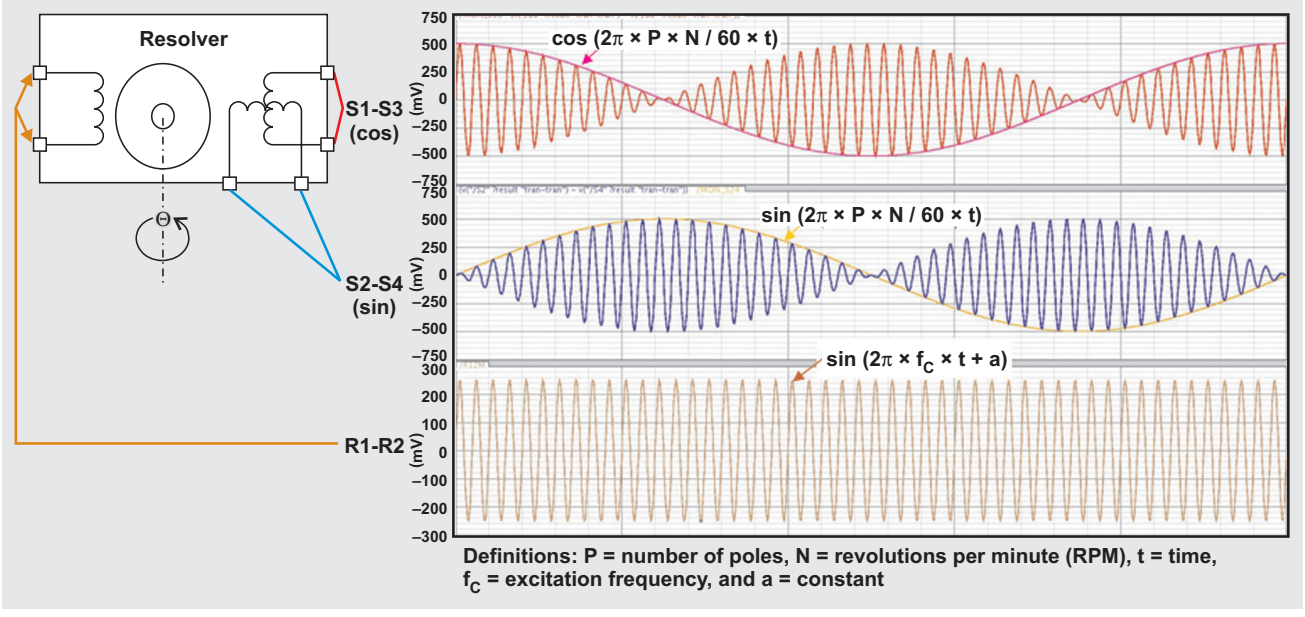
Introduction

A resolver is an angular position sensor that is commonly used in harsh, rugged environments. A fully electric vehicle (EV) may use multiple resolvers for a variety of control systems that perform rotary motion and additional resolvers may be required to create system redundancy for safety.[1] A resolver-to-digital converter (RDC) interface processes the analog output of the resolver sensor and communicates it in digital format to the engine control unit (ECU) in an EV. When designing an RDC interface, it is important to select the right RDC architecture to ensure that the circuit operates consistently under stringent conditions (such as vehicle acceleration). This article presents an overview for the architecture of a RDC interface circuit. The PGA411-Q1 is an example of the RDC interface circuit described.[2] Included is a review of the basic principles involved in designing an RDC interface, a discussion of RDC architecture that is based on a digital tracking loop, and special design considerations are covered for an EV application. Also included is a performance comparison of the PGA411-Q1 with RDC architecture versus a 19-bit optical encoder.

Resolver-to-digital conversion principle

As shown in Figure 1, a resolver sensor has one rotor winding (R1-R2) with the exciter sine wave that is AC-coupled to two stator windings. The stator windings, a sine coil (S2-S4) and a cosine coil (S1-S3), are mechanically positioned 90 degrees out-of-phase. As the rotor spins, the rotor position angle (Θ) changes with respect to the stator windings. The rotor and stator windings have a turns ratio in the order of 30%. The resulting amplitude-modulated signals shown in Figure 1 are typical resolver output signals. These signals must be gained, demodulated and post processed to extract angle and velocity information.

Figure 1. Representation of resolver signals: exciter, sine, and cosine



Definitions: P = number of poles, N = revolutions per minute (RPM), t = time, f_C = excitation frequency, and a = constant

RDC architecture

Figure 2 shows an RDC architecture that converts analog resolver signals into digital angle and velocity outputs. The analog front end (AFE) consists of programmable gain amplifiers and a comparator. The AFE block conditions the output signals of the resolver by removing noise, sets correct input DC bias, and appropriately gains up the AC signal to be used by the subsequent blocks. A digital feedback loop is the main part of the RDC conversion. It starts by assuming a digital angle, phi. This angle is digitally processed using the sine and cosine lookup tables stored in memory. This in turn is fed to the corresponding sine and cosine digital-to-analog converters (DACs). The DAC outputs are multiplied with the amplitude-modulated resolver signals (Equations 1 and 2), which are the sine and cosine inputs to the RDC.

$$\text{Resolver sensor sine signal} = \sin\Theta \times \sin\omega t \quad (1)$$

$$\text{Resolver sensor cosine signal} = \cos\Theta \times \sin\omega t \quad (2)$$

where Θ = resolver shaft angle and ω = excitation frequency applied at R1-R2.

The main objective of the RDC architecture is to calculate the rotation angle (Θ) and the velocity of the resolver shaft. As shown in Figure 1, angular position information is extracted from the envelope or voltage peaks of the input sine and cosine signals. In order to calculate the angle, sine Θ is multiplied by a feedback signal (cosine φ), where φ is the assumed angle resulting from the lookup table in the memory. Similarly, cosine Θ is multiplied by the feedback signal (sine φ). The purpose of this multiplication is to solve the general formula:
(sin A × cos B) – (sin B × cos A) and create sin (A – B).

$$\begin{aligned}\varepsilon_{pulse} &= \sin(A - B), \text{ or} \\ &= (K \times \sin\Theta \times \sin\omega t \times \cos\varphi) \\ &\quad - (K \times \cos\Theta \times \sin\omega t \times \sin\varphi) \quad (3)\\ \varepsilon_{pulse} &\equiv K \times \sin\omega t \times (\sin\Theta \times \cos\varphi - \cos\Theta \times \sin\varphi) \\ &= K \times \sin\omega t \times \sin(\Theta - \varphi)\end{aligned}$$

where φ = approximation of the resolver angle and K = a constant.

The output of the differential comparator is in digital form and is directly fed into the digital blocks to eliminate the carrier wave or the sin ωt component with a synchronous detection circuit. This synchronous detection block uses the exciter feedback signal as the reference. The resulting output, $V_{\varphi ERR}$, goes into the digital tracking control loop to generate the desired angle output.

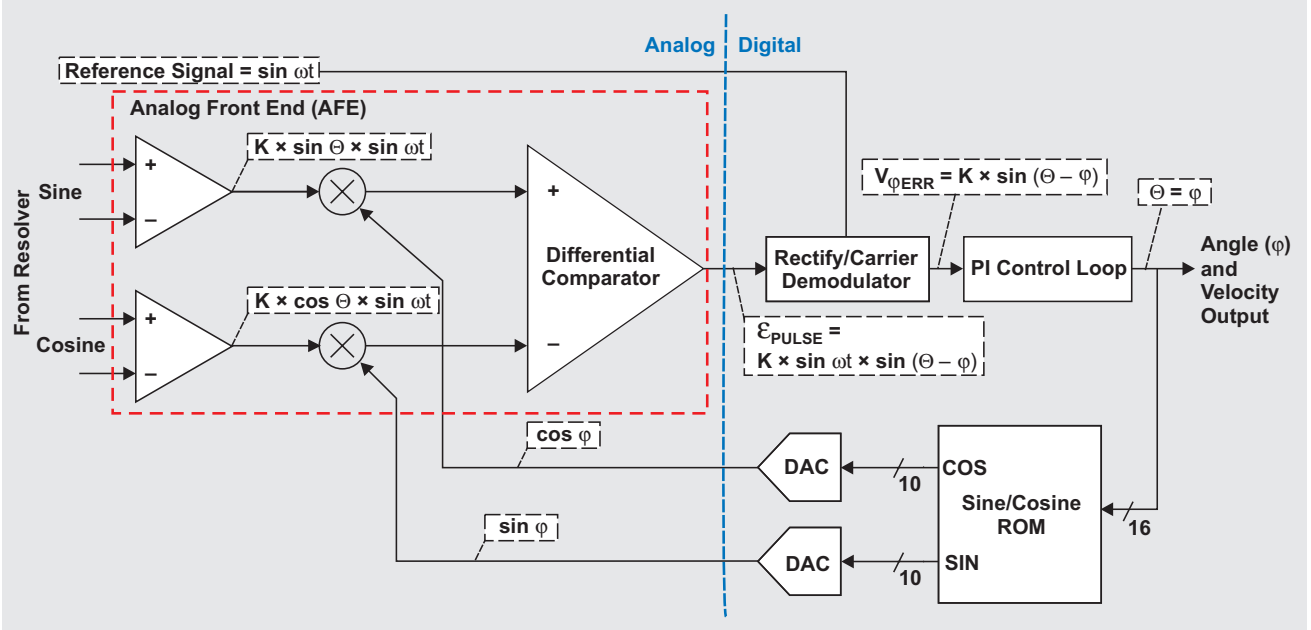
$$V_{\varphi ERR} = K \times \sin(\Theta - \varphi) \quad (4)$$

The negative feedback of the control-loop configuration employed in this RDC architecture helps to continuously reduce the $V_{\varphi ERR}$ signal to be very close to zero. For small values of $\Theta - \varphi$, $V_{\varphi ERR}$ is very near zero. Thus, the digital feedback loop continuously corrects itself, making the error close to zero so that the assumed RDC output angle (φ) is equal to the resolver shaft angle (Θ).

As shown in Figure 2, the $V_{\varphi ERR}$ signal is fed into a PI-control loop (Type II direct servo loop). Many control topologies for implementing loop tracking are possible.

One of the commonly used feedback control configurations is known as integral action.[3, 4] The advantage of this control configuration is its ability to reduce the steady-state tracking error to nearly zero. However, precautions must be taken because slightly excessive integral gain can cause oscillations in the system or even instability. This

Figure 2. Simplified resolver-to-digital converter (RDC) architecture



issue is addressed by adding another widely used proportional control known as proportional plus integral control (PI).

PI control is typically implemented as shown in Figure 3.[5] It helps bring steady-state error to zero and has improved transient response. Because of the added benefit of proportional control, it also does not cause any offset and leads to faster response than integral control alone.

Example application: Electric vehicle

Motor control action is an integral part of an EV. Communicating the motor position information accurately and quickly is essential. The resolver attached to a motor shaft tends to change its output very quickly. Hence, the RDC architecture must be designed to follow this change.

Typically, the most critical component of the RDC architecture that determines how fast this can happen is the digital tracking loop.

To determine the behavior of the tracking loop, it is important to understand a key term, settling time. When the resolver output signal changes rapidly, the converter's step response is determined by the phase margin and gain margin of the control loop.[3] Settling time is a quick performance indicator of the RDC's control system. Figure 4 shows a settling-time example of an RDC feedback control system with a step-input change shown in black. The blue signal shows normal-mode response for the circuit in Figure 3 and the red signal shows response during acceleration mode (rapid change in angle), which is described on the following page.

Figure 3. Example of a PI control loop

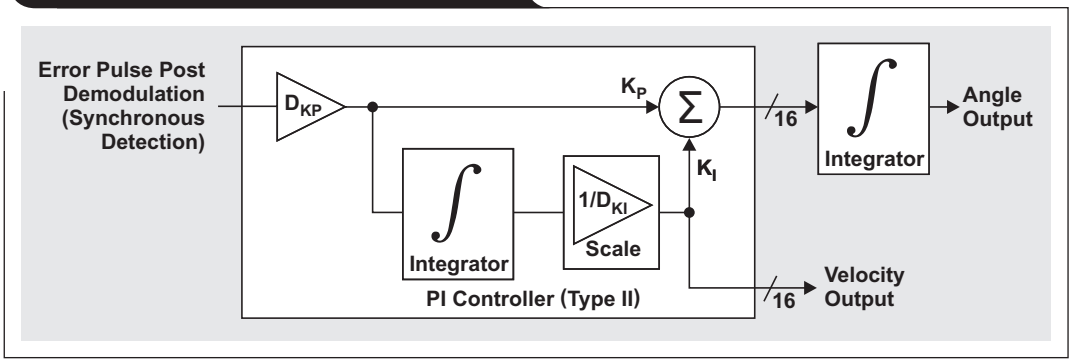
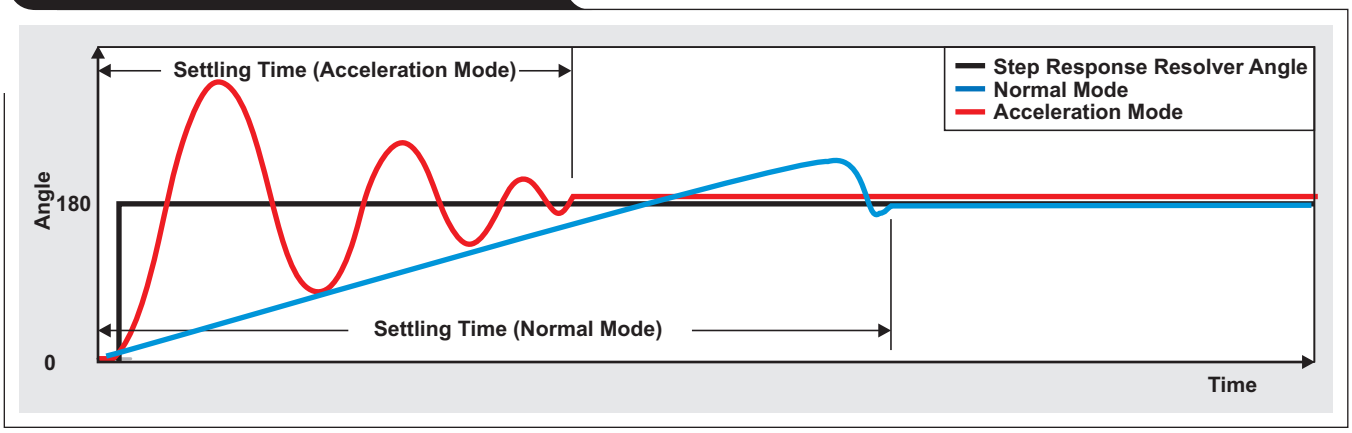


Figure 4. RDC step-response settling time



In order to follow the rotation angle under rapidly changing conditions, another loop-acceleration block is added in Figure 5 that can change the control-loop feedback gain. The higher-gain option helps the control loop to track a fast rotation angle much easier. In the acceleration mode (red signal in Figure 4), the proportional gain is increased by several times compared to the normal mode. Several diagnostic features are also added to alert the system if the signal integrity of the exciter and sine/cosine coils have been compromised.

Error sources that affect system accuracy

The errors can be categorized into three groups:

Group 1: Resolver sensor placement

- Sensor's mechanical construction: Static error is generated by manufacturing variations.
- Coil imbalance: The output voltages of the sine and cosine coils could be imbalanced and result in an error.
- Misalignment of resolver sensor: The resolver may be incorrectly mounted and lead to static error in the system.

Group 2: RDC architecture

The RDC architecture can cause static and dynamic errors in the system. The time delay from the input of the resolver signal to the output of the angle data also can cause errors in the system. For example, the input filter is used to decouple noise from the system. The delay caused by the filter circuit or the filter time constant may result in angular displacement during high-speed resolver operation. Therefore, be careful when selecting any common-mode capacitors that are added to the circuit to filter out noise. These common-mode capacitors can significantly affect phase relationship of the resolver signals and cause an imbalance between sine and cosine outputs, which can cause an error in the RDC output angle.

In addition, offset drifts in the AFE and linearity of the DACs can significantly affect the accuracy of the converted angle.

Group 3: Environmental factors

The external magnetic field from the motor-control circuit and high-voltage support in the EV can affect the resolver sensor's magnetic-coupling action and cause an error. Cable shielding is commonly used to prevent resolver signals from becoming affected, along with filter design at the input of the resolver converter to cut off any unwanted signals. The ability of the RDC architecture to reject common-mode noise is critical. Otherwise, the noise shows up on the signal-to-noise floor of the RDC, affecting the signal-to-noise ratio (SNR) and total harmonic distortion (THD) performance.

Figure 5. PI control with acceleration block

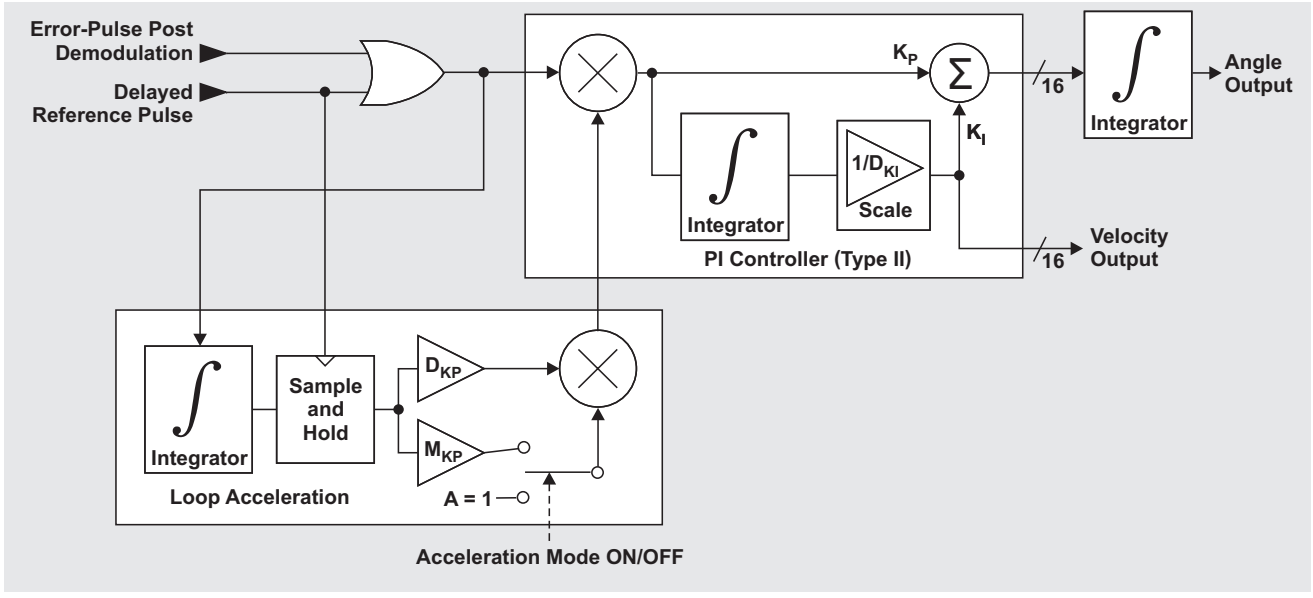
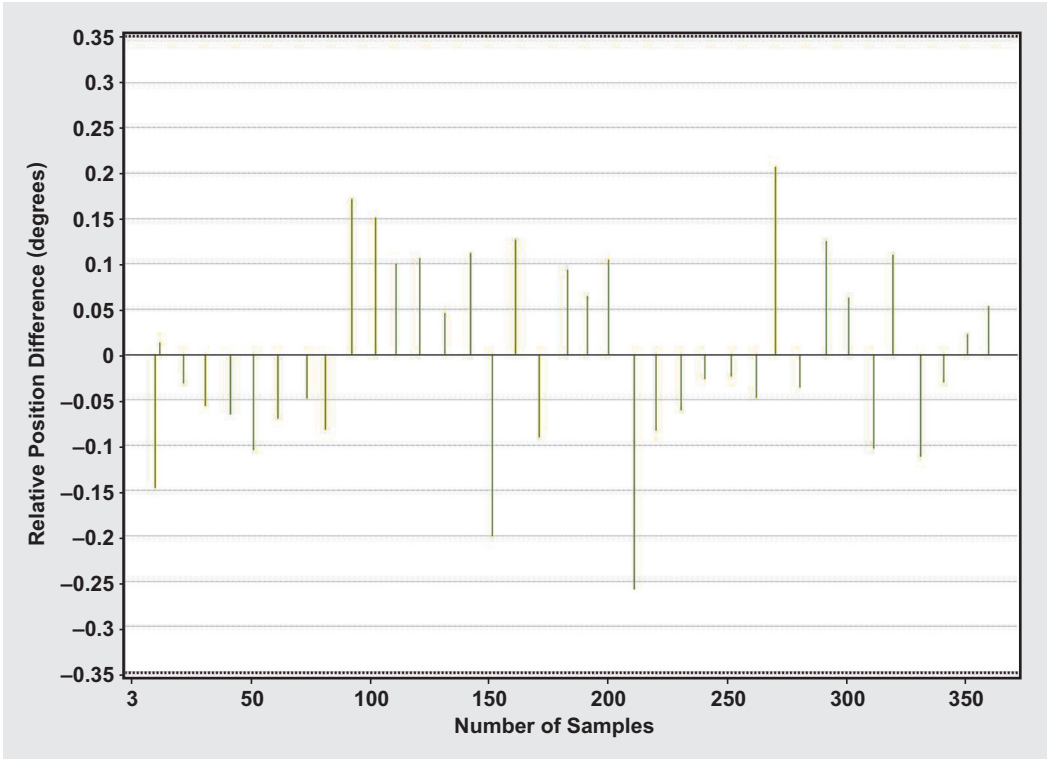


Figure 6. Measured RDC performance compared to a 19-bit optical encoder



RDC performance versus a 19-bit optical encoder

To better understand the performance of the resolver system, the results of a 12-bit RDC were compared to a 19-bit optical encoder. The mechanical set up included an example resolver and optical encoder mounted on the same shaft. Relative position difference was measured and plotted (Figure 6). The relative difference rules out any common-mode noise in the system that may cause the absolute values to misalign. The errors between the absolute angle deviation of the measured 16-bit RDC and the 19-bit optical encoder are less than ±0.25 degrees.

Acknowledgement

The authors would like to acknowledge Toru Tanaka from Texas Instruments for his initial work on RDC system definition.

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Product information:
PGA411-Q1
PGA411-Q1 Troubleshooting Guide (SLAA687)

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Automating amplifier circuit design

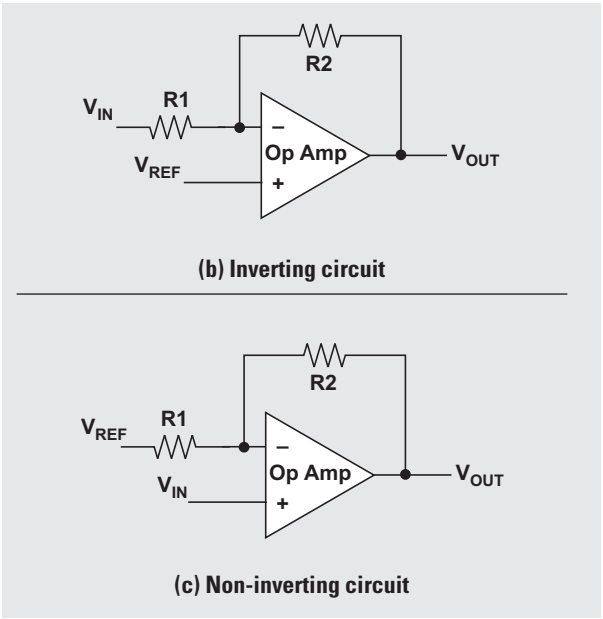
By Bonnie C. Baker
WEBENCH® Senior Applications Engineer

Introduction

The semi-expert techniques for automating amplifier circuit designs calls for a combination of hard specification requirements and judgement margins. A design tool must support these techniques to zero in on the appropriate operational amplifier (op amp) and external components. Figure 1 shows two fundamental circuit examples that implore this type of tool.

Yes, these are simple topologies – but the difficulty is in the detail when selecting amplifiers and external components to meet the performance criteria for the application.

Figure 1. WEBENCH® Amplifier Designer operational amplifier design circuits

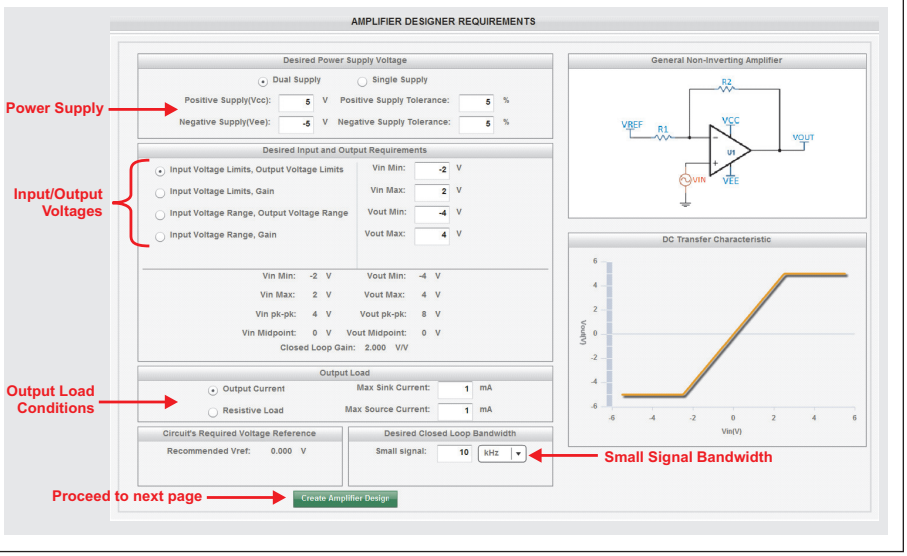


Requirements: Mapping from many to one

The ultimate task is to find the perfect op amp for an amplifier circuit. In the case of selecting amplifiers from Texas Instruments, this challenge requires the designer to sort through approximately 1300+ op amps. These amplifiers come with many variations on their electrical performance and specifications. The key specifications include power-supply ranges, bandwidth, input/output swing limits, and others. On top of these hard constraints, most amplifier choices use a series of overlapping issues, such as accuracy, noise, power, temperature drift, and/or IC cost.

Starting from ground zero, the first task is to sort amplifiers according to basic suitability for the final design. As step one, the designer identifies the basic-circuit operational values. These values can be entered using a web-based amplifier design tool, such as the WEBENCH® Amplifier Designer (Figure 2).

Figure 2. Amplifier Designer Requirements page for user's data-entry activities



On the Amplifier Designer Requirements page (Figure 2), fields that must be completed are:

- Power supply voltages
- Circuit input and output signals
- Output load conditions
- Small-signal output bandwidth

These design requirements allow the Amplifier Designer software to select an appropriate op amp for the amplifier circuit.

As a start, the provided power supply voltages can eliminate devices with supply voltages that are out-of-range. For example, the input values in Figure 2 may be for a dual-supply, ±5 V. From this information, the software eliminates op amps with maximum power-supply ranges below 10 V, and minimum power-supply ranges greater than 10 V. Additionally, the amplifier selection process removes amplifiers with excessively-high power-supply ranges.

As for the amplifier's input stage, the design tool ensures there is no violation to the op amp's common-mode range. With the output stage, the software makes sure that signals remain within the rail limits of the power supply, while taking a further step to ensure that the output swing is within the candidate-amplifier's linear region. To achieve this, the software uses the amplifier's output load conditions.

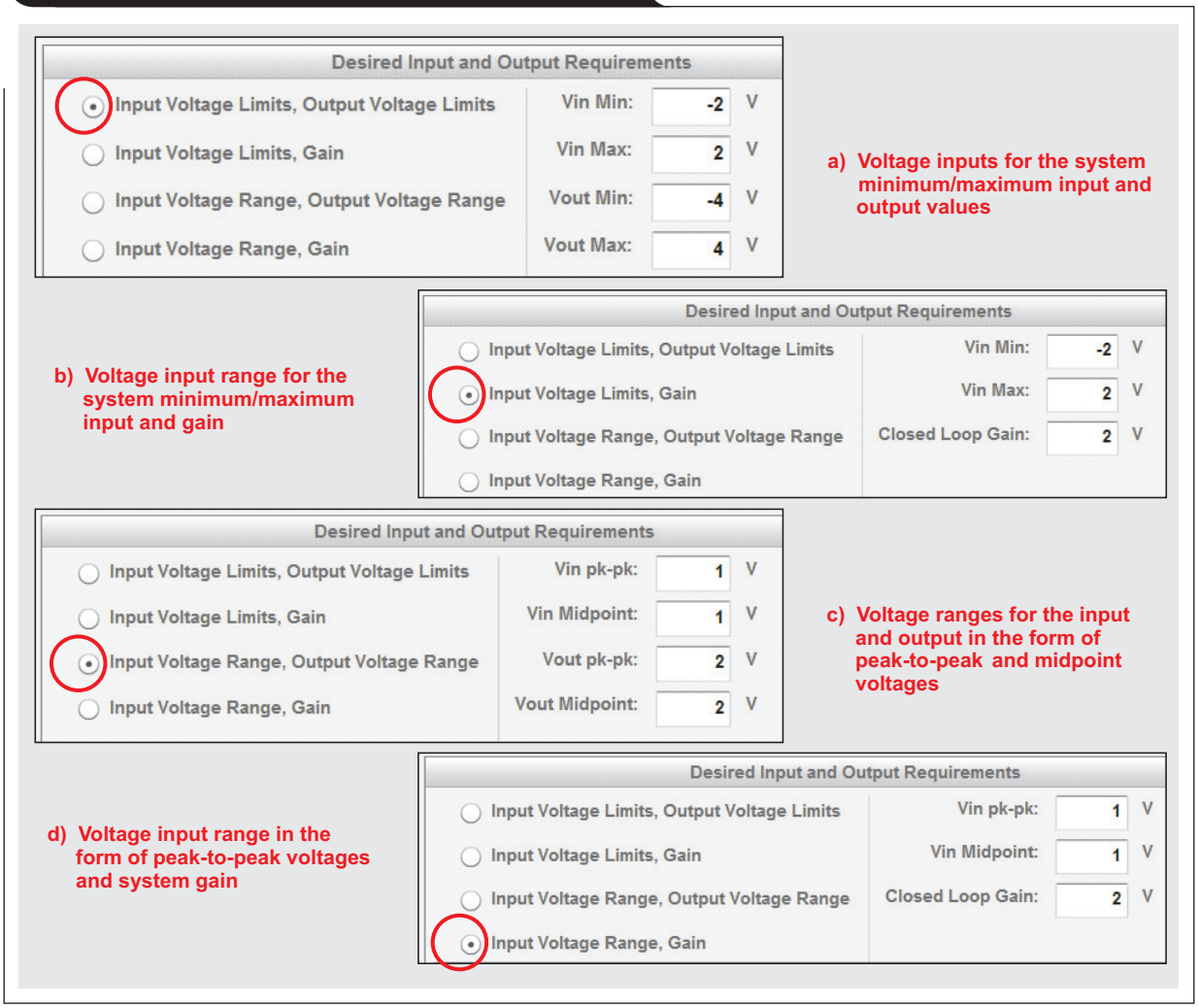
The tool offers four data entry styles for input voltages, output voltages, and gain. It also accommodates individual designer preferences as shown in Figure 3.

For the last data entry, the design tool uses the small-signal bandwidth to identify suitable amplifiers. In an effort to take the amplifier's process variations into account, the applied guard band for this specification is approximately 20 percent.

These data inputs were used for the discussion on the following pages:

V_{CC} = 12 V
V_{EE} = 0 V
V_{IN}Min = 5.5 V
V_{IN}Max = 6.5 V
V_{OUT}Min = 0.5 V
V_{OUT}Max = 11.5 V
I_{OUT} source/sink current = 1 mA
Small signal bandwidth = 500 kHz

Figure 3. Voltage input and voltage output styles



Screening op amps to target: Visualizer screen

The next design screen was obtained by clicking the Create Amplifier Design button.

During the transition from the view in Figure 2 to Figure 4, the software determines the resistor values in the target op amp circuit. It is easy to assign a generic feedback resistor (R2) value of 1 kΩ. However, a better general guide is to assign the values according to Table 1.

Table 1. Appropriate voltage-feedback amplifier (VFB) R2 resistance values

Gain bandwidth	R2
Gain bandwidth ≤ 0.01 MHz	1 MΩ
0.01 MHz < Gain bandwidth ≤ 0.1 MHz	100 kΩ
0.1 MHz < Gain bandwidth ≤ 10 MHz	10 kΩ
10 MHz < Gain bandwidth ≤100 MHz	1 kΩ
100 MHz < Gain bandwidth ≤ 1 GHz	500 Ω
1 GHz < Gain bandwidth ≤ 10 GHz	200 Ω

The algorithms that produce the Amplifier Designer Visualizer screen shown in Figure 4 create a reduced list of op amps. The order of the amplifiers listed depends on which optimizer parameters have been selected.

On the top left of Figure 4 is a list of input Design Criteria and to the right is the Optimizer box.

The Optimizer box has three pull-down menus with the following options to set design priorities:

- Precision
- Noise
- Temp Drift
- Supply Current
- Cost

The question to ask is, of these five characteristics in the Optimizer pull-down menus, which is the Very Important, Important, and Less Important? When the choice is completed, the Solution Table in Figures 4 shows updated results.

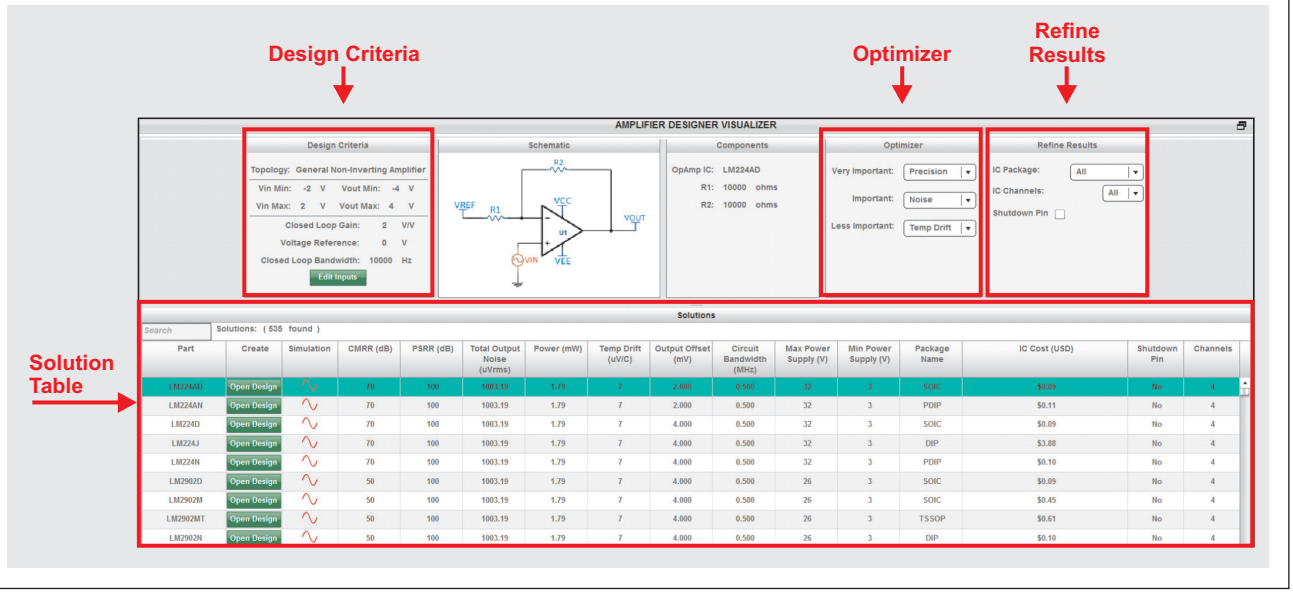
Additionally, further criteria refinements are possible with the menu in the upper right corner of Figure 4. The choices available in this area are:

- Package Group
- Number of Channels
- Shutdown Pin

The selections in this section are self-explanatory, however, these selections further reduce the list of amplifiers.

When the Optimizer menu options are changed such that Precision is selected as Very Important, Temp Drift as Important, and Supply Current as Less Important, the OPA140 should appear near the top of the list in the Solution Table.

Figure 4. Amplifier Designer Visualizer screen



Designer summary screen

The next step is to proceed on to the Amplifier Design Summary screen. For the following discussion, the Open Design button was selected for the OPA140 in the Solution Table of the Visualizer screen.

At this point, the amplifier has been selected and the circuit fully defined. The Amplifier Designer Summary screen (Figure 5) allows exploring the theoretical feasibility of the design.

The center bar in Figure 5 shows selection tabs for viewing Calculated Performance Analysis, Calculated Performance Values, and the Bill of Materials.

The Calculated Performance Analysis segment produces input/output graphs as shown in Figure 5. There are menu selections to view AC, sine and square-wave graphical responses. These curves are not a result of a simulation; rather the page shows calculated theoretical graphs. The intent is to provide a quick look at the circuit's behavior before proceeding any further.

The Calculated Performance Values tab allows viewing circuit characteristics in seven categories:

1. Design criteria
2. Operating frequency values
3. Power requirements
4. V_{OS}/I_b error
5. V_{OUT} gain versus resistor tolerance
6. Error over temperature
7. Total output noise

Within these seven categories, there are calculated performance values. For instance, the operating frequency values (#2 above) provides the amplifier bandwidth, amplifier slew rate, closed-loop bandwidth, and full-power bandwidth (FPBW).

Figure 5. Amplifier Designer Summary screen

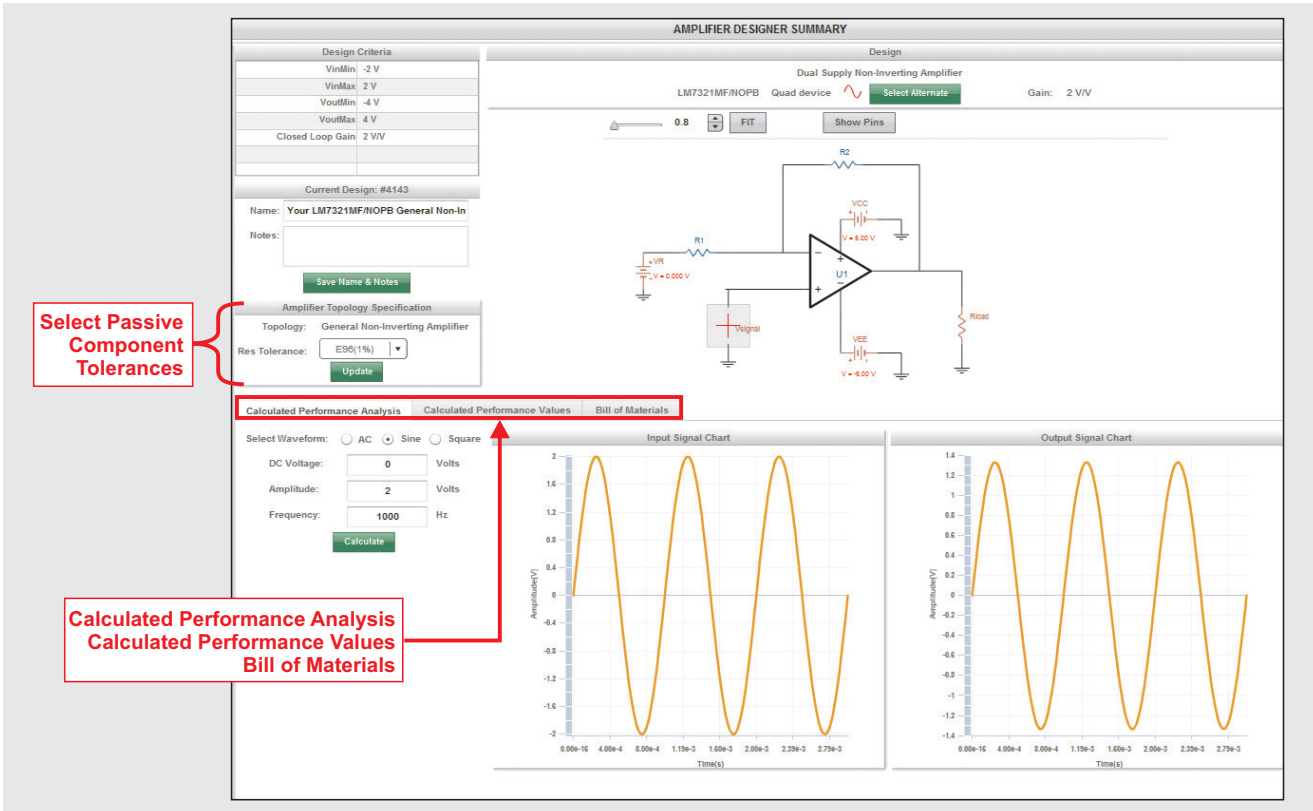
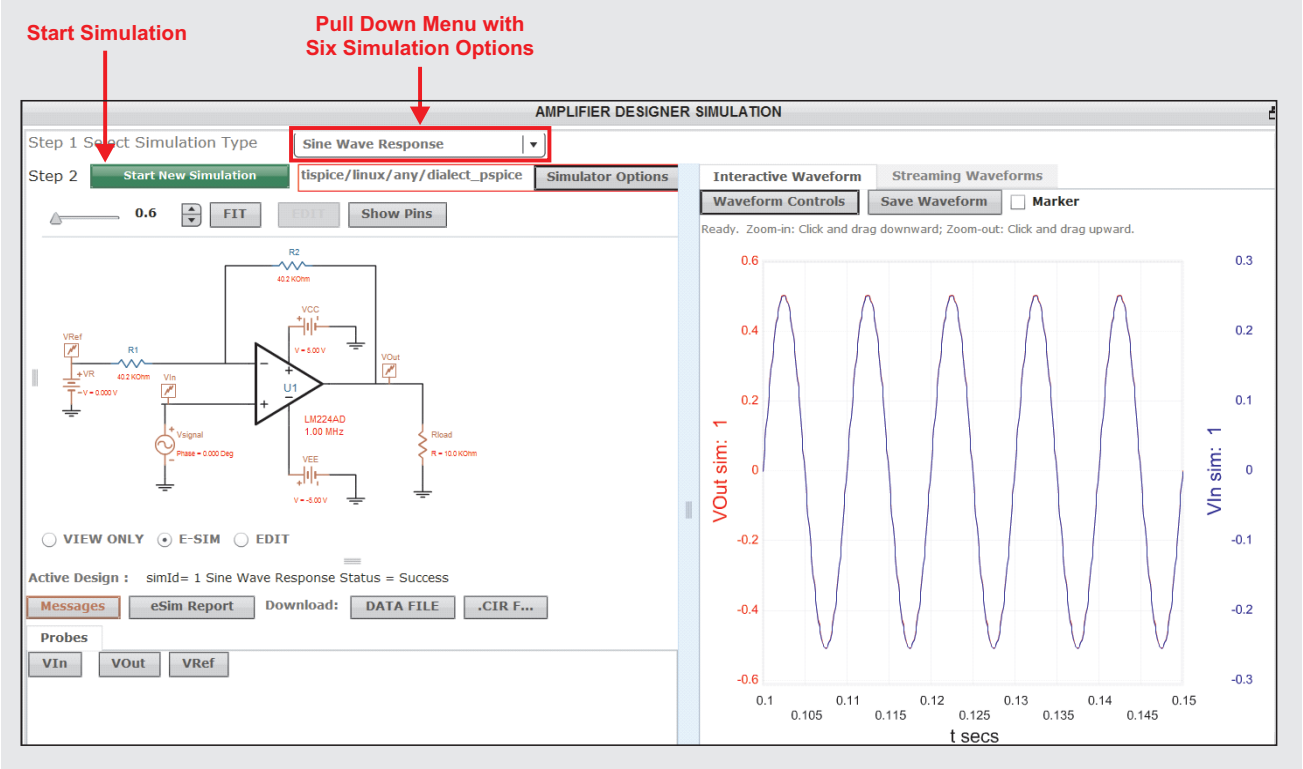


Figure 6. Amplifier Designer Simulation screen



Amplifier designer simulation

To proceed to the TI SPICE simulation screen, click on the Sim button at the top of the screen (not shown in Figure 5).

The Amplifier Designer ports the complete circuit to the simulation screen. The Amplifier Simulation environment (Figure 6) uses Texas Instruments PSPICE® models while providing six simulation options:

1. Sine wave
2. Step response
3. Closed loop response
4. DC sweep
5. Total noise
6. Group delay

With all of these simulation options, the Amplifier Designer provides the appropriate signal sources. There are options to modify the magnitudes, frequency, and timing of these sources.

If this simulation environment is not suitable, it is possible to download the circuit into a TINA-TI™ environment. WEBENCH® Amplifier Designer offers this export option by clicking on the Sim Export button at the top of the simulation screen (not shown in Figure 6).

Conclusion

The WEBENCH Amplifier Designer tool automatically performs the basic analysis and product-selection activities that designers would normally perform in their circuit design activities—but it takes the process a step further. It offers a comprehensive evaluation of the new circuit, making it easy to fit the amplifier design into the rest of the system design.

Related Web sites

Design tools:
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Product information:
OPA140

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JESD204B over optical fiber enables new architecture for phased-array radars

By Matt Guibord
System Engineer, High-Speed Data Converters

Electronically controlling the beam direction of a phased-array antenna has been in use since the mid-twentieth century. However, most antennas still rely on analog methods to steer the beam.[1] The next step for phased-array radar is to achieve full digital control of the beam, often called a "digital phased-array radar." A digital phased array requires every antenna element to have its own data converters. Analog phase-shifting is no longer performed between the antenna and data converters in this architecture. Instead, phase-shifting and beamforming are performed using purely digital functions.

Digital phase shifting and beamforming enables the formation of multiple beams and can allow multiple frequency bands to be used for multi-target tracking or simultaneous missions. Aside from flexibility, there are also performance reasons to move toward digital arrays. For one, the imperfect analog phase shifters and beamforming elements are replaced by precise digital phase-shifting and beamforming for improved sidelobe rejection. Additionally, clutter rejection is improved because of decorrelated analog-to-digital (ADC) and digital-to-analog (DAC) converter noise and distortion at every antenna element.[2]

The biggest roadblocks for building digital arrays are size, power, and processing ability. Each element, including data converters and other analog components, must be small enough to allow elements to sit half a wavelength from each other (Table 1). Such tight spacing raises thermal concerns, creating a requirement for low power consumption. Lastly, the required processing power for digital beamforming is significantly higher than analog beamforming, due in part to digital phase shifting and beamforming, but also due to the significantly higher amount of data from the ADCs.

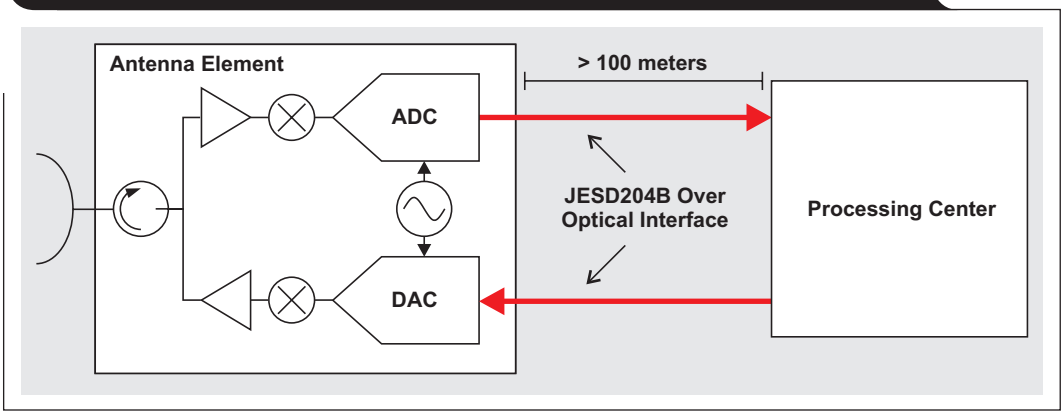
There are a number of potential architectures that could be used in digital phased-array radars. For instance, discrete data converters can be connected to FPGAs, all sitting at the antenna array. However, FPGAs are large, power hungry and noisy, especially with increased processing requirements. So it is undesirable to have one sitting at the array near sensitive analog components. Depending on usage, an FPGA can consume up to tens of watts of power, creating thermal issues and likely requiring bulky heat sinks or other advanced cooling methods. Instead, a preferred architecture moves the FPGA off the array and connects to the data converters directly through optical fiber. This architecture has recently become possible due to the adoption of the JESD204B interface in data converters (Figure 1).

JESD204B is a serialized data-converter interface that can operate at up to 12.5 Gbps over multiple current-mode logic (CML) lanes. The physical interface used is similar to that used by gigabit Ethernet protocols and, thus, lends itself well to use with optical transceivers. Using optical transceivers can extend the reach of the otherwise short-reach interface to greater than 100 meters. It is clear that placing an optical transceiver at the array to connect to the data converters and another at the FPGA can enable digital phased-array radar without the need for an FPGA at the antenna array.

Table 1. Antenna element spacing versus operating band

Radar Operating Band	Maximum Antenna-Element Spacing
L-band	150 mm
S-band	75 mm
C-band	37.5 mm
X-band	18.75 mm

Figure 1. Phased-array antenna element with optical JESD204B interface



A simplistic board placement shown in Figure 2 demonstrates the feasibility of this architecture in digital L-band, S-band, and potentially C-band radars. The RF paths shown are fairly narrow, however, using both the top and bottom of the board enables more room for placement and routing. This example uses commercially available components and is drawn to scale.

A 1-Gsps, 16-bit dual-channel ADC (ADS54J60) enables high performance for signal bandwidths of greater than 250 MHz. Likewise, a 2.5-Gsps, 16-bit dual-channel DAC (DAC38J82) enables similar transmit performance. For data rates of 1 Gsps, each data converter is capable of using two serializer/deserializer (SerDes) lanes per channel at 10 Gbps. The optical transceivers contain twelve channels allowing six ADC channels and six DAC channels to be used per set of transmitter and receiver. Total optical transceiver power at the antenna array is about 380 mW per antenna element, lower than an equivalent architecture with an FPGA directly interfaced to the data converters. Ideally, the optical transceiver size and power would be reduced even further.

The challenge with this architecture is not so much related to the SerDes interface itself as it is to the other signals required for JESD204B. Other than data, there are three main signals required when using the subclass 1 variant of JESD204B: device clock, SYSREF and SYNC.

Device clock is analogous to the data converter sampling clock and has the same low-jitter performance requirement. The skew between device clocks for multiple data converters ultimately determines the phase accuracy of the sampling instant, a key requirement for phased-array radar. However, it is possible that digital techniques can be used to compensate for device clock skew. The only additional concern added by the optical architecture is that both ends of the optical link must be frequency synchronized for the synchronous serialized link to function properly.

SYSREF is a low-frequency timing reference used for all JESD204B devices in order to obtain deterministic latency. For multi-device synchronization, SYSREF must be captured by the same device clock cycle at every data converter, or at least exactly an integer number of SYSREF periods later. This places a setup-and-hold timing requirement on SYSREF relative to the device clock. Additionally, the FPGA must also receive SYSREF at a deterministic time relative to the data converters in order to achieve deterministic latency. Thus, the phase of SYSREF at each end of the optical link must be well controlled.

SYNC does not have any specified timing requirements for subclass 0 or subclass 1 implementations of JESD204B. For most purposes, it is a binary DC signal that is used only during link initialization to align the character clocks within the SerDes transmitter and receiver. The receiver must toggle SYNC low on start up to tell the transmitter to start the code group synchronization process. Since this is a DC signal, an optical implementation requires encoding before transmission. Due to the large number of data converters that could be used in the system, and therefore large number of SYNC signals, a likely implementation

Figure 2. Example board placement using JESD204B over optical (to scale)

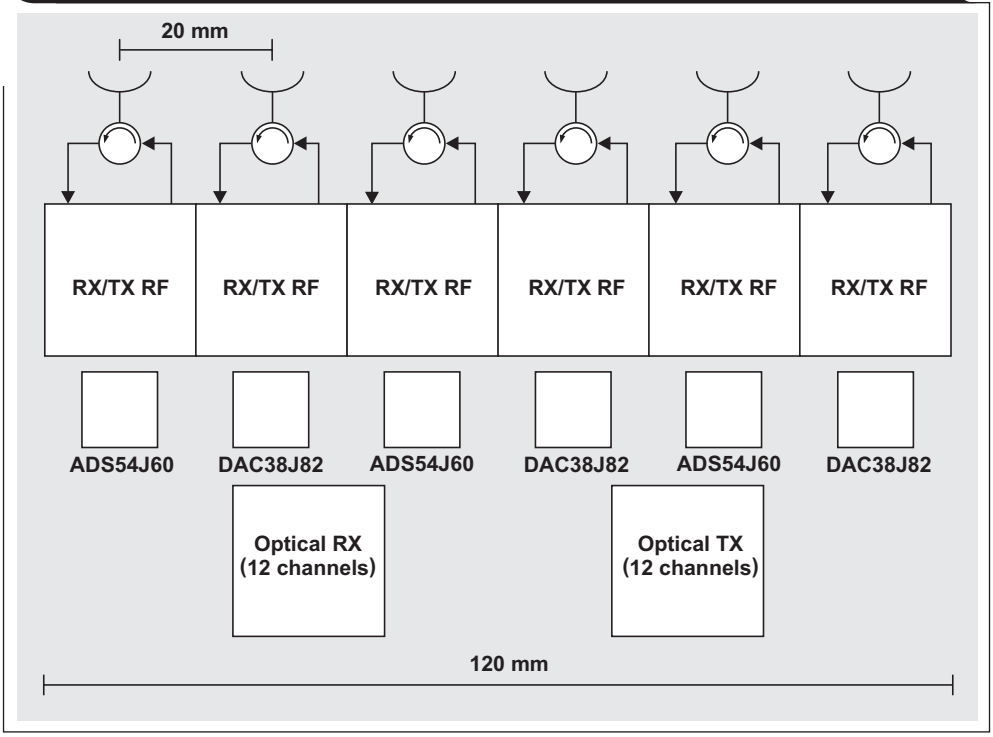
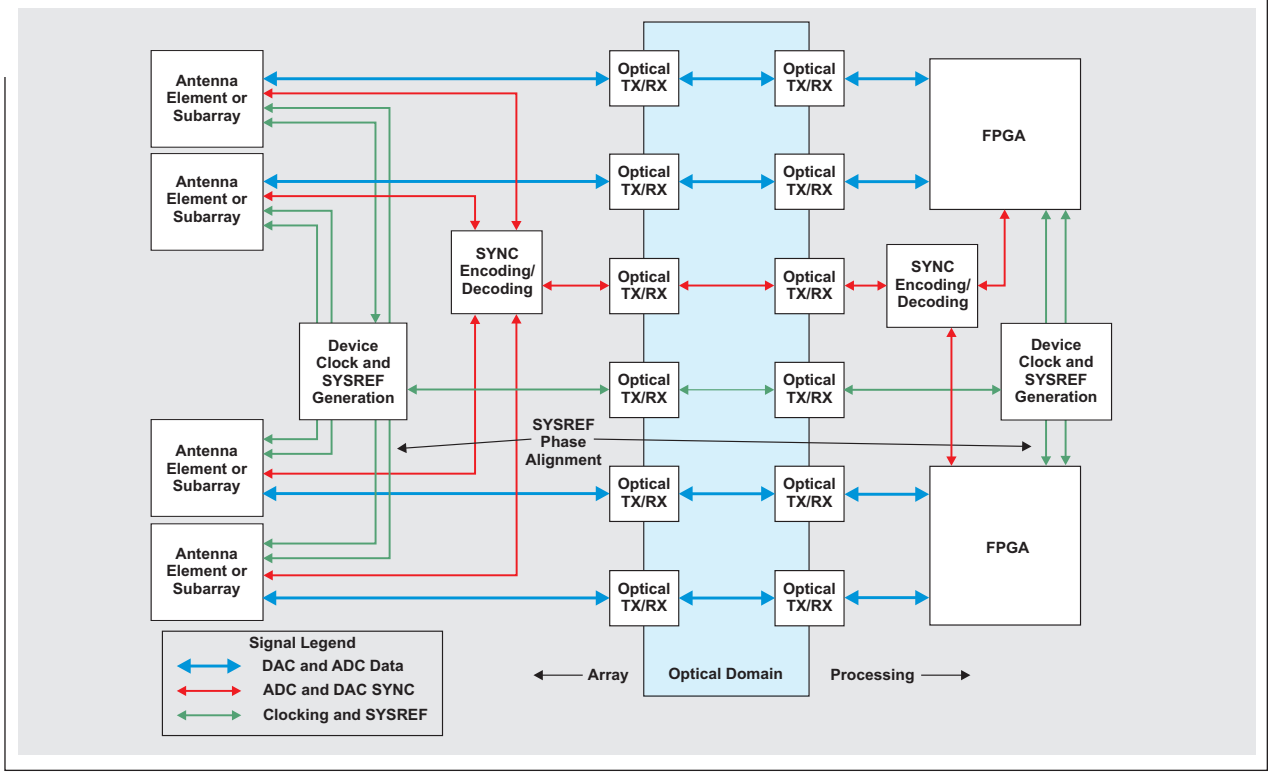


Figure 3. High-level phased-array radar system diagram using optical fiber in the JESD204B link



uses SYNC signal aggregation. A designer can do this by ANDing signals together to limit the total number of SYNC signals transmitted over the optical link. Note that SYNC can have timing requirements for subclass 1 implementations when numerically-controlled oscillators (NCOs) are used as part of digital up or down converters within the data converters.[3]

Figure 3 shows a high-level system block diagram of phased-array radar using an optical implementation of JESD204B. It is assumed that both the device clocks and SYSREF signals are generated at a single location at the array and distributed through traditional means to each antenna element to maintain high performance and phase alignment. The SYNC signals for each element can be aggregated at the subarray level (N SYNC signals in each direction for N subarrays in the system). An alternative is to aggregate each element at the system level before being encoded for transmission across optical to limit the number of signals.

Note that the clocks, including SYSREF and SYNC signals, can be sent over a copper interface such as coax cables, rather than over an optical link. The feasibility is dependent on the distance between the antenna elements and the FPGAs. A copper implementation of those signals is likely simpler, eliminating the encoding problem for SYNC and simplifying phase alignment of SYSREF.

Conclusion

There is little doubt that phased-array radars will continue to move toward the concept of digital phased-array radars, however, the optimal architecture is still debatable. The architecture discussed here, making use of JESD204B over optical, may enable entirely digital arrays for L-band, S-band, and C-band radars. This architecture reduces the total power and thermal requirements at each antenna element by eliminating the requirement for an FPGA to be near the data converters. Further reductions in optical transceiver size and power would make this architecture even more compelling.

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MOSFET power losses and how they affect power-supply efficiency

By George Lakkas
Product Marketing Manager, Power Management

Power-supply efficiency is a critical criterion for today's cloud-infrastructure hardware. The efficiency of the chosen power solutions relates to system power loss and the thermal performance of integrated circuits (ICs), printed circuit boards (PCBs), and other components, which determines the power-usage effectiveness of a data center.

This article revisits some of the basic principles of power supplies and then addresses how MOSFETs—the power stage of any switching-voltage regulator—affect efficiency. For the linear regulator shown in Figure 1, power loss and efficiency are defined by Equations 1 and 2.

$$\text{Power Loss} = (V_{IN} - V_{OUT}) \times I_L \quad (1)$$

$$\text{Efficiency} = \frac{V_{OUT} \times I_L}{V_{IN} \times I_L} = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In the ideal switching regulator shown in Figure 2, the current is zero when the switch is open and the power loss is zero, thus V_{IN} is being chopped. When the switch is closed, the voltage across it is zero and the power loss is also zero. An ideal switch implies zero losses, thus offering 100% efficiency. However, components are not ideal, as is illustrated in the following examples.

An efficient switching regulator results in less heat dissipation, which reduces system cost and size for elements such as heat sinks, fans and their assembly. In battery-operated systems, less power loss means that these devices can use the same battery for a longer run time because the device pulls less current from the battery.

To consider the various factors that contribute to efficiency, the focus of this article is on the step-down (buck) DC/DC converter topology, which is the most popular switching-regulator topology in today's cloud infrastructure systems. Figure 3 shows the key power-loss contributors in a buck converter: conduction losses, switching losses, and static (quiescent) losses.

MOSFETs have a finite switching time, therefore, switching losses come from the dynamic voltages and currents the MOSFETs must handle during the time it takes to turn on or off.

Switching losses in the inductor come from the core and core losses. Gate-drive losses are also switching losses because they are required to turn the FETs on and off. For the control circuit, the quiescent current contributes to power loss; the faster the comparator, the higher the bias current. For the feedback circuit, the voltage divider, error amplifier and comparator bias currents contribute to power loss. Megaohm resistors cannot be used to reduce

Figure 1. Typical linear regulator

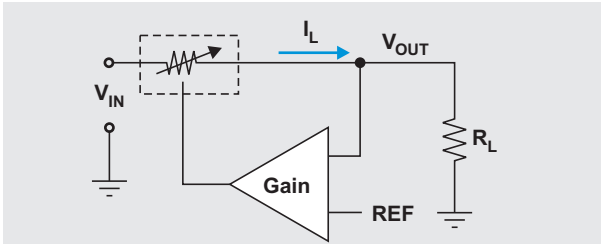


Figure 2. Ideal switching regulator with the switch open

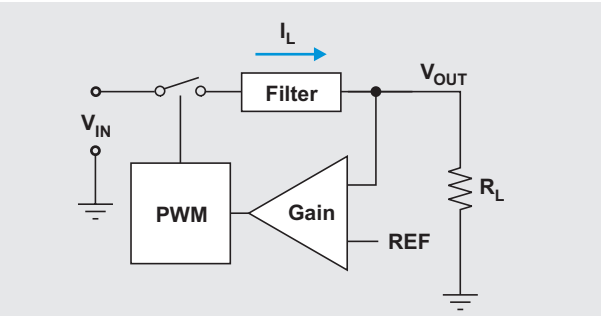
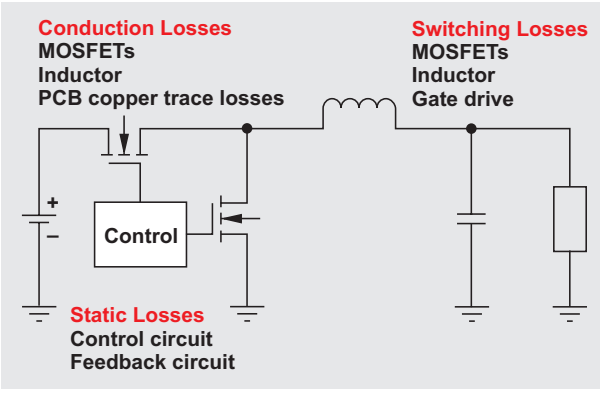


Figure 3. Power-loss contributors in a buck switching regulator



power loss because of the bias current into the feedback circuit. Figure 4 shows a basic switching circuit and Equation 3 is used to calculate conduction losses for Q1 or Q2.

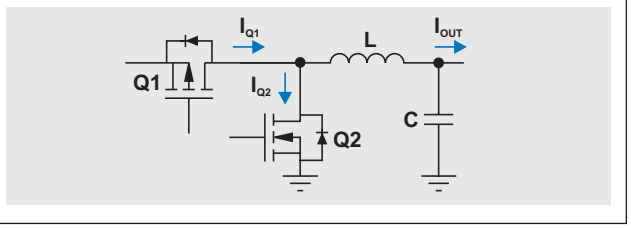
$$P_{CON} = R_{DS(on)} \times I^2_{QSW(RMS)}$$
$$= R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left(I^2_{OUT} + \frac{I^2_{RIPPLE}}{12} \right) \quad (3)$$

Note that R is the $R_{DS(on)}$ of the selected MOSFET, I is the root-mean-square (RMS) current through the MOSFET, and that neither of these is a function of switching frequency. In general, a higher switching frequency and higher input voltage require a lower QG (gate charge) to cut down the switching losses in the switch MOSFET (Q1).

For a rectifier MOSFET (Q2), low $R_{DS(on)}$ is most important, but don't ignore the gate power. Also, changing the MOSFET $R_{DS(on)}$ changes the duty cycle (D), which effects RMS currents and losses elsewhere. The inductor current also affects MOSFET conduction loss.

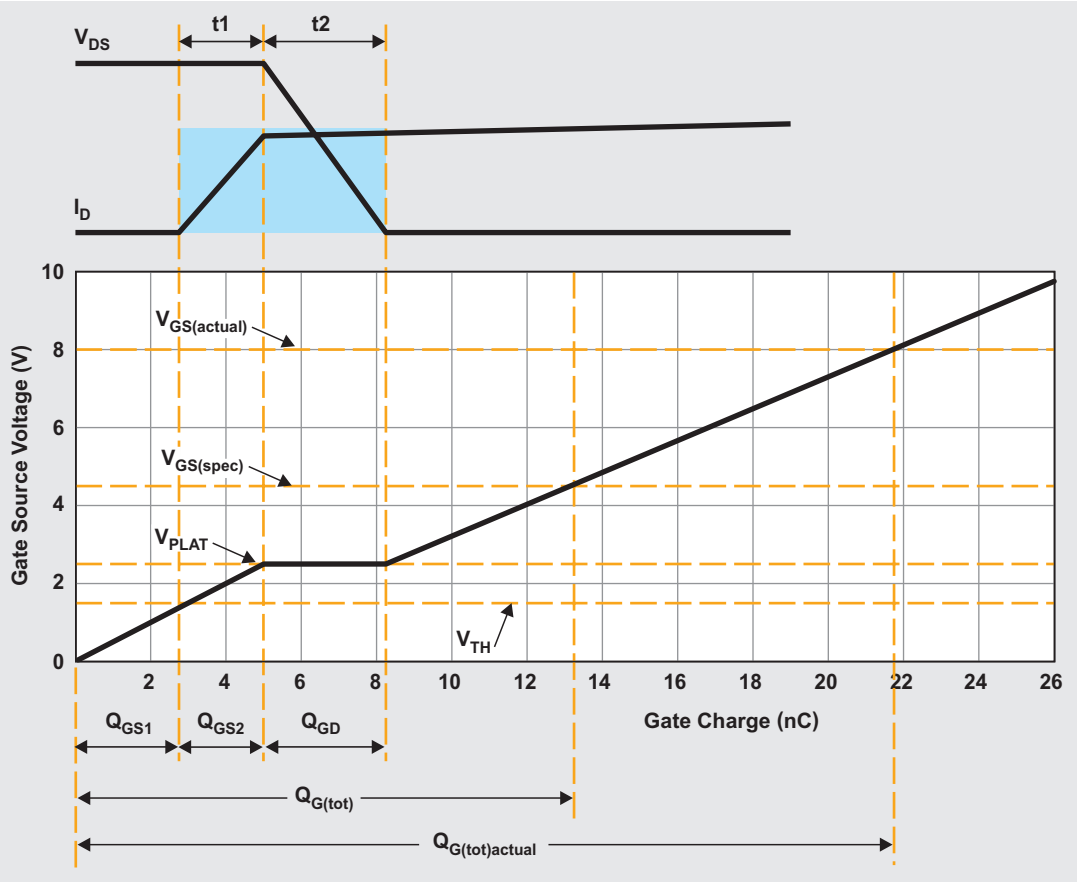
The high-side MOSFET (Q1) switching losses are evaluated first in Figure 5 because they are more complex.

Figure 4. MOSFET conduction losses



Relationships for Figure 5 to derive loss equation:
$E_{t1} = (V_{DS} \times I_D/2) \times t1$,
$E_{t2} = (V_{DS}/2 \times I_D) \times t2$,
$P_{SW} = 2 \times (E_{t1} + E_{t2}) \times f_{SW}$,
$t1 = Q_{GS2}/I_G$,
$t2 = Q_{GD}/I_G$,
V_{PLAT} = Miller plateau,
V_{TH} = Gate-to-source threshold voltage,
$I_G = Cdv/dt$,
$Q = C \times V$,
dt = t1 or t2, and
$V_{GS(actual)}$ is the actual gate-to-source drive voltage driving the MOSFET.

Figure 5. MOSFET switching losses



MOSFET switching losses are a function of load current and the power supply's switching frequency as shown by Equation 4.

$$P_{SW} = V_{IN} \times I_{OUT} \times f_{SW} \times \frac{(Q_{GS2} + Q_{GD})}{I_G} \quad (4)$$

where $V_{IN} = V_{DS}$ (drain-to-source voltage), $I_{OUT} = I_D$ (drain current), f_{SW} is the switching frequency, Q_{GS2} and Q_{GD} depend on the time the driver takes to charge the FET, and I_G is the gate current.

Switch-MOSFET gate losses can be caused by the energy required to charge the MOSFET gate. That is, the $Q_{G(TOT)}$ at the gate voltage of the circuit. These are both turn-on and turn-off gate losses.

Most of the power is in the MOSFET gate driver. Gate-drive losses are frequency dependent and are also a function of the gate capacitance of the MOSFETs. When turning the MOSFET on and off, the higher the switching frequency, the higher the gate-drive losses. This is another reason why efficiency goes down as the switching frequency goes up.

Larger MOSFETs with lower $R_{DS(on)}$ provide lower conduction losses at the cost of higher gate capacitances, which results in higher gate-drive losses. These losses can be significant for power-supply controllers (with external MOSFETs) at very high switching frequencies in the multiple-megahertz region. There is no known method for calculating a "best" Q_G and $R_{DS(on)}$ in a given situation, although figure-of-merit (FOM) numbers are typically mentioned in data sheets as (FOM = $R_{DS(on)} \times Q_G$).

For the switch MOSFET shown in Figure 6, a lower gate charge (Q_G) in Equation 5 enables lower power loss and a faster switching time; however, this contributes to more parasitic turn-on of the rectifier MOSFET. A happy medium can be obtained in the design to accommodate these trade-offs.

$$P_{GATE} = Q_{G(TOT)} \times V_G \times f_{SW} \quad (5)$$

There are also general gate losses as shown in Figure 7. The MOSFET effect on the gate-driver IC, or a pulse-width modulation (PWM) controller with an integrated gate driver, add to the power-dissipation losses.

As shown by Equation 6, gate-drive losses do not all occur on the MOSFET.

$$P_{DRV} = \frac{V_{G\_DRV} \times Q_{G(tot)} \times f_S}{2} \times \left(\frac{R_{GHI}}{R_{GHI} + R_G + R_{GI}} + \frac{R_{GLO}}{R_{GLO} + R_G + R_{GI}} \right) \quad (6)$$

where:

- P_{DRV} is the total gate drive loss divided to calculate the driver loss,
- R_{GHI} is turn on of the driver,
- R_{GLO} is the turn off of the driver,
- replacing R_{GHI} with R_G is the loss in the gate resistor,
- replacing R_{GHI} with R_{GI} is the switching FET loss,
- higher Q_G increases driver dissipation, and
- adding external R_G reduces internal driver dissipation because it reduces the overall resistance path to the MOSFET gate.

Figure 6. Switch MOSFET gate losses

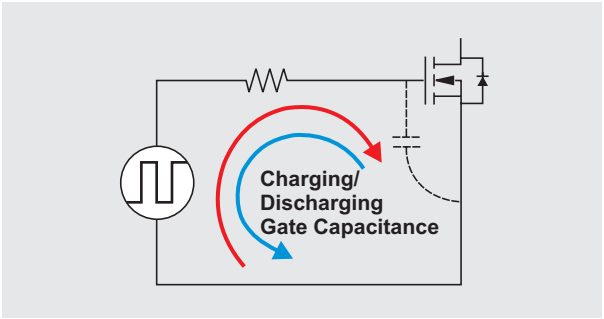


Figure 7. General gate losses

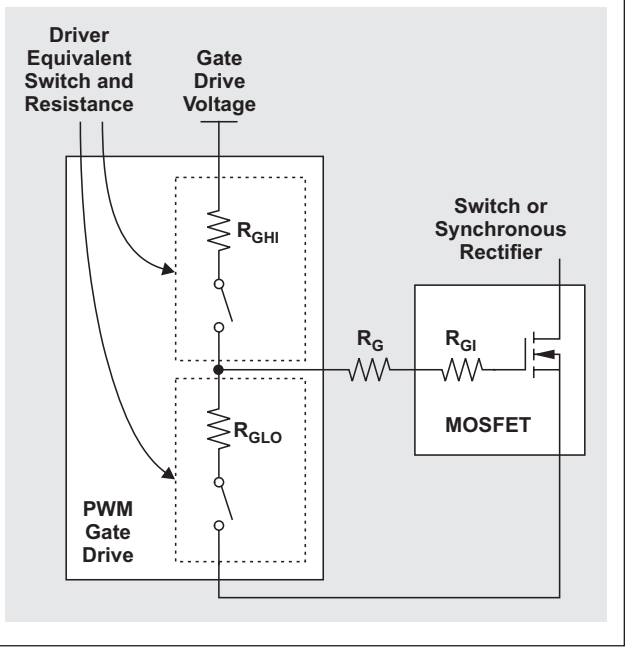


Figure 8 shows the various contributors that affect total switch MOSFET losses.

Now consider the rectifier (synchronous) MOSFET total and conduction losses. Power loss in a rectifier MOSFET consists of conduction losses (P_{CON}), body-diode conduction losses (P_{BD}), and gate losses (P_{GATE}).

There are no switching losses because of the body diode. The body diode conducts and the voltage across the FET is the diode voltage, which is zero. The body diode ensures zero-voltage switching per Equation 7.

$$P_{QSR} = P_{CON} + P_{BD} + P_{GATE} \quad (7)$$

Conduction losses are simple I^2R losses when the MOSFET channel conducts per Equation 8.

$$P_{CON} = R_{DS(on)} \times \left[1 - \frac{V_{OUT}}{V_{IN}} - \left(t_{DLYUpLo} + t_{DLYLoUp}\right) \times f_{SW}\right] \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}\right) \quad (8)$$

where:

- R is the $R_{DS(on)}$ of the selected MOSFET,
- I is the RMS current through the MOSFET,
- $t_{DLYUpLo}$ is the delay between the upper MOSFET turning off and the lower MOSFET turning on, and
- $t_{DLYLoUp}$ is the delay between the lower MOSFET turning off and the upper MOSFET turning on.

The rectifier MOSFET also has body-diode losses. The average body-diode current can be calculated during dead time.

The blue waveform in Figure 9 shows the dead time, which is the time between when the high-side FET turns off and the low-side FET (rectifier FET) turns on. We want the average current in the switching cycle. The output inductor (L) dictates the slope of the dotted line, I_{BD1}, I_{BD2}, I_{BD3}. This slope is the average current through the body diode.

Equations 9a through 9e can be used to determine the body-diode current:

$$I_{BD(1)} = I_{BD(PK)} - \frac{V_O \times t_{DLYUpLo}}{L} \quad (9a)$$

$$I_{BD(2)} = I_{BD(PK)} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{L} \quad (9b)$$

$$I_{AVGUpLo} = I_{BD(PK)} - \frac{V_O \times t_{DLYUpLo}}{2 \times L} \quad (9c)$$

$$I_{AVGLoUp} = I_{BD(PK)} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{2 \times L} \quad (9d)$$

$$I_{BD(AVG)} = \left[\left(I_{BD(PK)} - \frac{V_O \times t_{DLYUpLo}}{2 \times L}\right) \times t_{DLYUpLo} + \left(I_{BD(PK)} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{2 \times L}\right) \times t_{DLYLoUp}\right] \times f_{SW} \quad (9e)$$

Figure 8. Total switch MOSFET losses

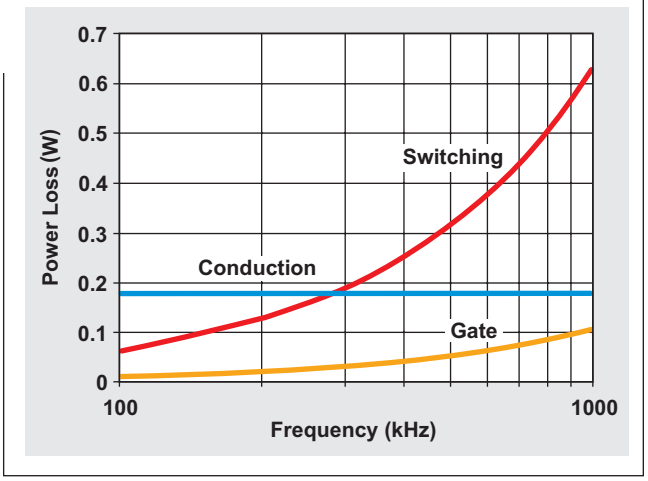
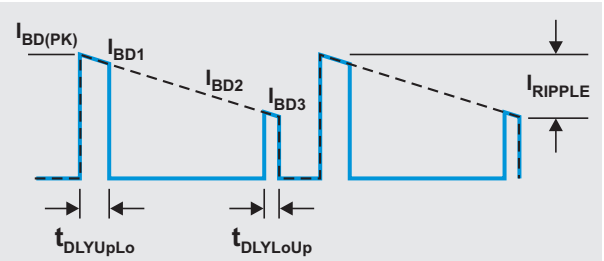


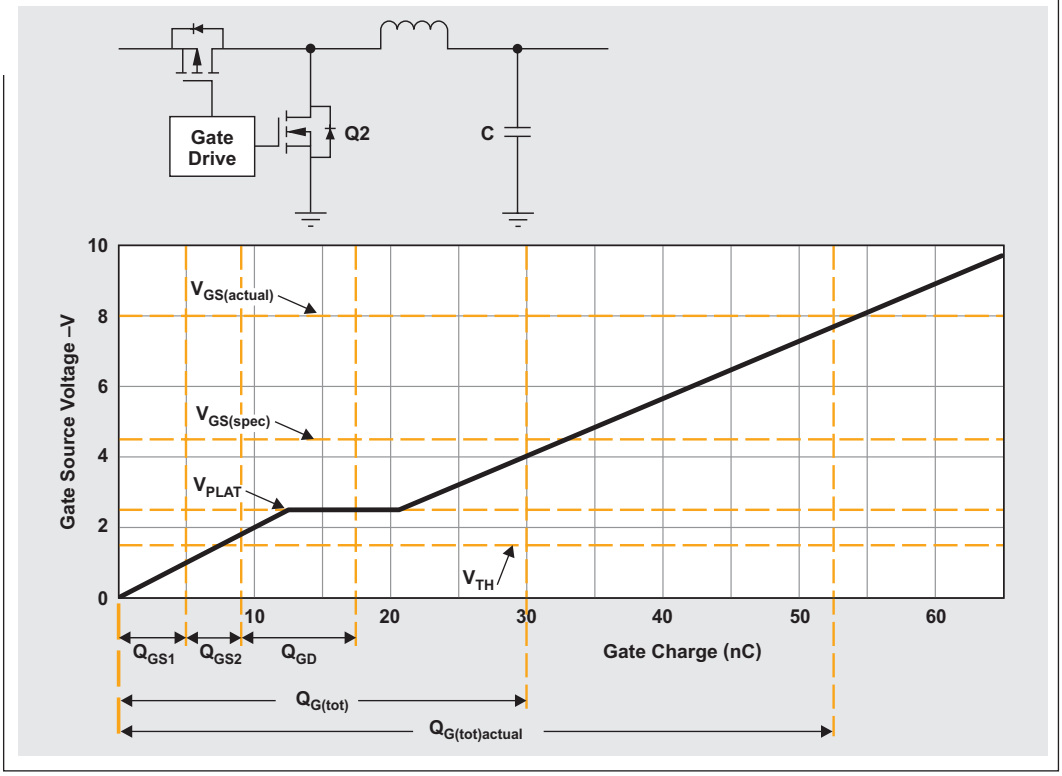
Figure 9. Rectifier MOSFET body-diode current



Equation 10 can be used to approximate the body-diode power loss.

$$P_{BD} \approx V_F \times I_{OUT} \times \left(t_{DLYUpLo} + t_{DLYLoUp}\right) \times f_{SW} \quad (10)$$

Figure 10. Rectifier MOSFET gate driver and losses



The final consideration in Figure 10 is for the gate losses of the rectifier MOSFET (Q2). Gate losses are calculated in the same manner as with the switch MOSFET. Losses can be significant because of a higher gate charge.

Figure 11 shows the various contributors that affect total losses attributed to the rectifier MOSFET.

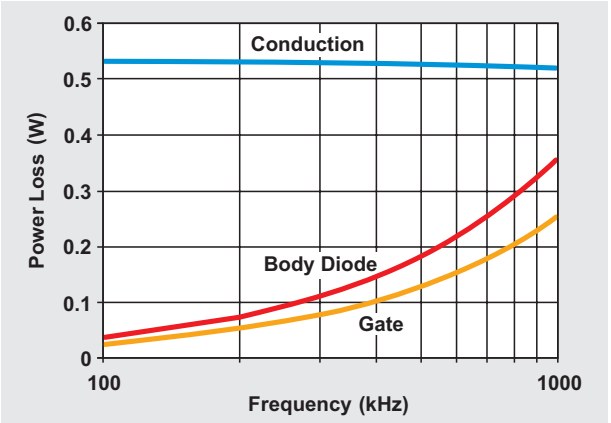
Conclusion

The efficiency of a synchronous step-down power converter with integrated or external MOSFETs can be optimized when the designer understands the parameters that affect efficiency and the specifications to look for in data sheets.

In the absence of an ideal power converter, the designer has to make trade-offs and optimize the parameters that affect power-supply efficiency.

A wide portfolio of discrete MOSFETs is available from Texas Instruments, including power blocks (dual-MOSFETs in one package) and power stages (gate driver and dual-MOSFETs in one package). Power supply control ICs that use MOSFETs are buck PWM controllers and SWIFT™ integrated MOSFET buck converters (both analog and PMBus™). An example of a PWM controller is the TPS40428 dual-output/dual-phase, PMBus, driverless PWM controller that is paired with the CSD95378B NexFET™ smart power stage An example of a SWIFT integrated-FET converter is the TPS544C25, a 30-A PMBus buck converter with frequency synchronization.

Figure 11. Total rectifier MOSFET losses



This device includes integrated MOSFETs where all the design equations of this article may be applied.

Related Web sites

Product information:
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Agency requirements for stand-by power consumption of offline and POL converters for consumer applications

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Brian King, *Applications Engineer, Senior Member of the Group Technical Staff*

Introduction

Trying to meet ENERGY STAR® requirements to maintain energy efficiency is a constant design challenge. As the number of consumer devices in homes increases and when taking energy from the grid, designers want to improve light-load efficiency without increasing cost or complexity. Reducing the product's power consumption by one watt can save megawatts from the grid, especially with high-volume consumer applications such as the set-top box. The semiconductor industry has developed new offline AC/DC and point-of-load (POL) DC/DC solutions that greatly improve efficiency at lower stand-by power levels. This article highlights new techniques used by new flyback and secondary-side controllers, and compares two complete POL architectures with and without the light-load efficiency feature. Also covered is the energy-saving advantage gained when selecting a POL solution with light-load efficiency features.

ENERGY STAR requirements for set-top boxes

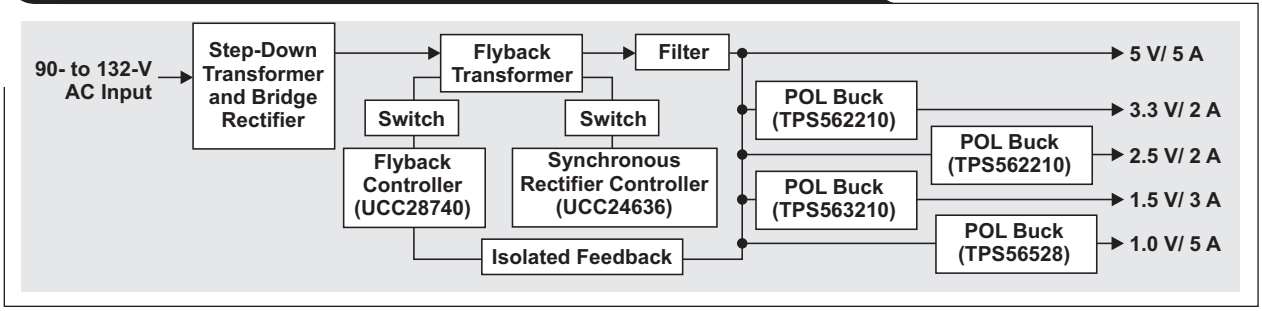
The final ENERGY STAR version 4.1 specification for set-top boxes was announced on April 4, 2014 and took effect on December 19, 2014. Version 4.1 accommodates new technology such as deep sleep functionality, multi-room configurations, displayless gateways, high-efficiency video processing, and ultra-high definition video.[1] If all set-top boxes sold in the United States (US) were ENERGY STAR compliant, the savings would be more than $1.8 billion per year, and more than 24-billion pounds of greenhouse gas emissions per year would be prevented. Investigating every avenue to reduce power consumption in a power-management design will improve the ability to meet the evolving ENERGY STAR requirements.

Power-management architecture

A power architecture for the US market was chosen for a design example that consists of an offline power supply that accepts a 90- to 132-VAC input from the mains. Since 5 V is the highest voltage required in most low-power set-top boxes, a 5-V intermediate bus was chosen over a 12-V bus to improve overall efficiency. The 5-V intermediate bus provides around 5 A, or 25 W, and the total power capability required depends on the additional functionalities integrated into the box, such as a removable media player, additional tuners, or an integrated digital video recorder. From the 5-V bus, typical POL voltages are 3.3 V, 2.5 V, 1.5 V, and 1.0 V, which are common in many POL architectures. The output currents of each POL voltage are usually less than 3 A, but requirements for the low-voltage rails have increased over time due to the added functionality of the main processor, which can require up to 5-A peak.

For this demonstration, an isolated AC/DC power supply (Figure 1) was constructed using a constant-current, constant-voltage flyback controller (UCC28740) along with a synchronous rectifier controller (UCC24636). The POL section on the secondary-side uses 2-A (TPS562210), 3-A (TPS563210), and 5-A (TPS56528) step-down buck converters to generate the four voltages from the 5-V bus. Each POL converter uses an advanced Eco-mode™ for high light-load efficiency. A reference design is available for download featuring both sections of the power supply and includes a schematic, bill of materials, test report and design files.[2]

Figure 1. Isolated AC/DC power supply with Eco-mode™ technology



AC/DC Conversion

The flyback converter can be used for set-top box AC/DC applications because it provides an inexpensive, isolated output and uses few external components. Operation of the flyback converter in discontinuous conduction mode (DCM) is especially attractive because it eliminates reverse recovery losses in the output rectifier to improve the efficiency. The simplified schematic in Figure 2 uses a flyback controller that uses DCM with valley switching to further reduce switching losses. The controller has a maximum frequency of 100 kHz to provide a high-density design and it also maintains control of the peak primary current in the transformer. The controller has a minimum switching frequency of 170 Hz to minimize the no-load power consumption to less than 60 mW when using a standard shunt regulator and optocoupler. Lower standby power can be achieved when using an optocoupler with a high-current transfer ratio and a lower-power regulator instead of a low-voltage shunt regulator.

To achieve higher full-load and light-load efficiency, a traditional diode solution used by the flyback topology can be replaced with a synchronous rectifier controller (UCC24636) and a power MOSFET. This near-ideal diode-rectifier solution reduces power dissipation of the rectifier and minimizes body-diode conduction time of the power MOSFET. A synchronous rectifier controller also reduces primary-side losses, simply due to the efficiency gains of the total power solution.

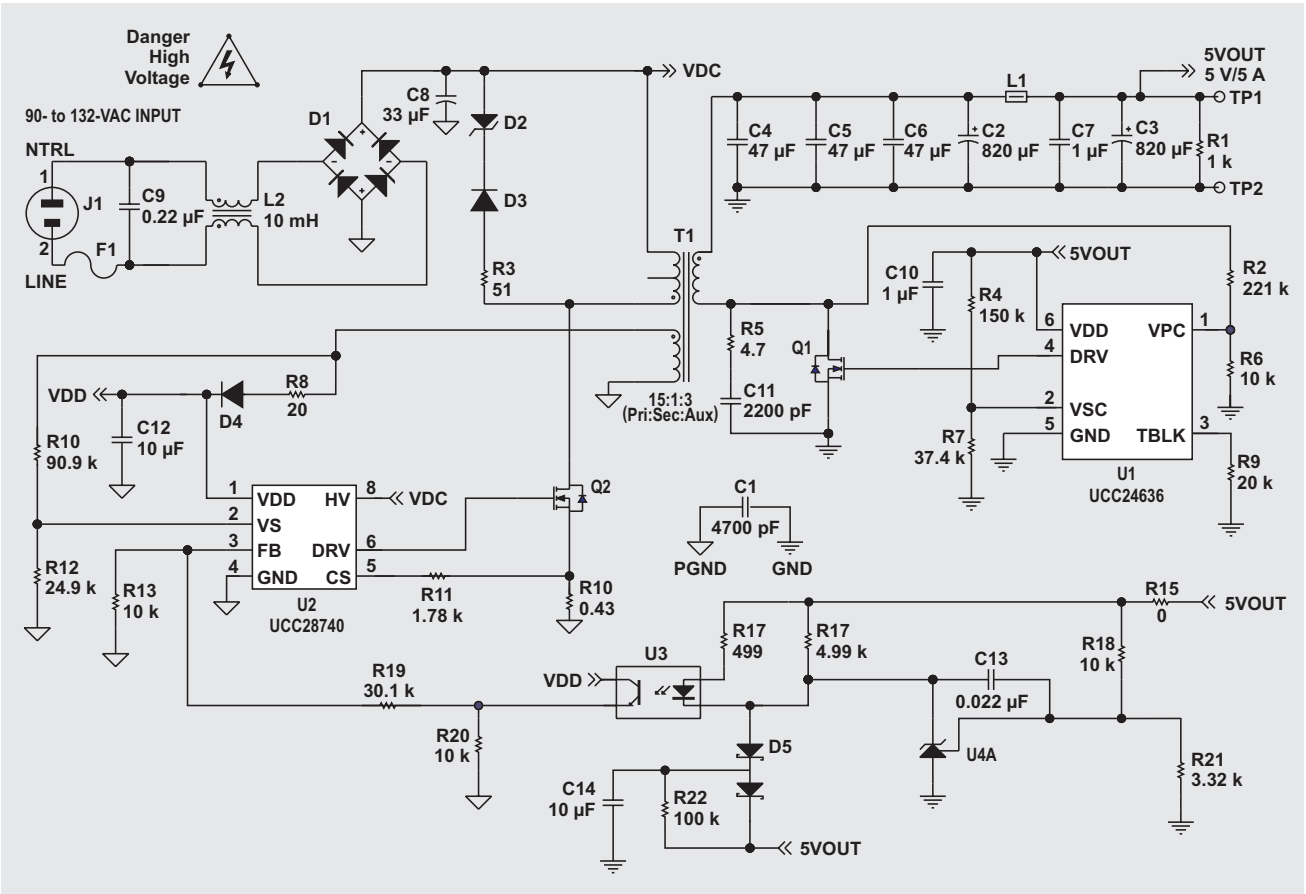
The four-point average efficiency of the offline supply is 85.1%, with a peak efficiency of 85.45% occurring at 25% rated load. Offline supply efficiency is shown in Table 1 with all other supplies disabled during the test. The no-load power dissipation is 61 mW.

Table 1. Offline power supply efficiency

Load	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	Efficiency
10%	2.97	4.98	4.99	83.81%
25%	7.3	4.98	1.252	85.45%
50%	14.64	4.98	2.503	85.14%
75%	21.94	4.97	3.75	84.95%
100%	29.27	4.97	4.999	84.88%

For set-top boxes using an external power supply (EPS), the external supply must also be ENERGY STAR qualified or meet the no-load and active-mode efficiency levels provided. Without using any energy-saving techniques, a traditional fixed-frequency pulse-width modulator (PWM) flyback converter can easily dissipate too much

Figure 2. Simplified schematic for a flyback and synchronous rectifier controller



energy and prevent a product from achieving ENERGY STAR compliance. To save energy throughout all load levels, a green-mode flyback and synchronous rectifier controller employs numerous loss-reducing techniques, including valley switching, variable frequency control, and pulse-skipping at light loads.

Point-of-load conversion

The POL regulators generating low voltages from the 5-V intermediate bus employ an energy-saving pulse-skipping technique with Eco-mode™ technology. Similar operation modes have traditionally been used in applications that are powered by batteries, such as cell phones and notebook PCs. However, DC/DC converters with such operating modes are becoming more prevalent in the market for non-portable applications due to ENERGY STAR requirements. See Figure 3 for one of these POL converter schematics.

The inductor current in a synchronous buck converter is a triangle wave. As the output current decreases from a heavy-load condition, the inductor current is reduced and the rippled valley of the triangle wave eventually touches the zero level at the boundary between continuous conduction mode (CCM) and DCM. With the pulse-skipping feature, the rectifying MOSFET is turned off when the converter detects zero current in the inductor. As the load current further decreases, the on time is held nearly constant so that the off time is extended and the switching frequency is reduced to maintain regulation. As a result, the power MOSFETs and inductor are idle for longer time periods and conduction losses are greatly reduced. The point at which the DC/DC converter enters the light-load efficiency mode is shown in Equation 1.

$$I_{OUT(LL)} = \frac{L \times f_{SW}}{2} = \left(V_{IN} - V_{OUT}\right) \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

POL efficiency comparison

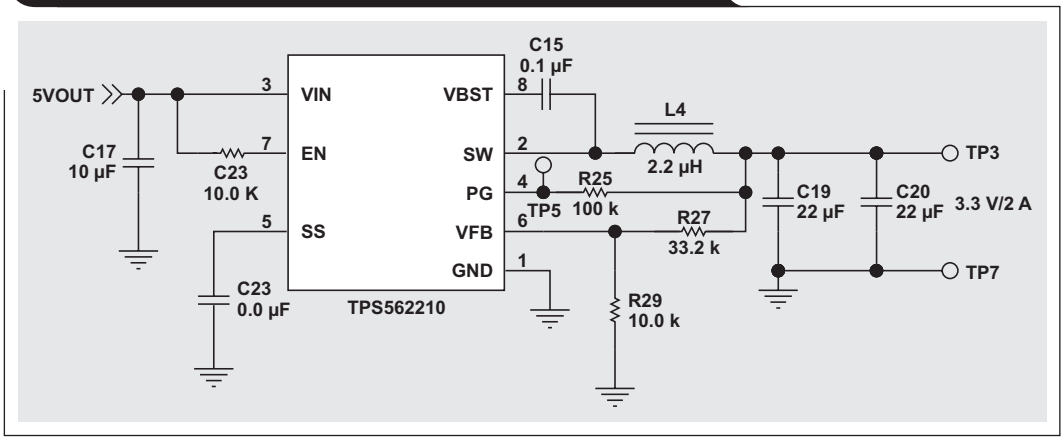
The efficiency measurements for each POL converter were taken with the demonstration board from no-load to full-load and summarized in Table 2. Many designers will inspect an efficiency curve to verify performance. In this case, however, it is advantageous to inspect the actual power dissipation in watts to verify whether excessive power dissipation precludes meeting an agency approval's specification. Note that the total power dissipation for all four converters, while enabled and switching, is only 29 mW at no-load and 36 mA at 10 mA. The low power-loss performance is due to pulse-skipping and low operating quiescent current of each device.

Table 2. Power dissipation with Eco-mode™ converters

Load	Power Dissipation (W)				Total Dissipation (W)
	POL 1 V/5 A	POL 1.5 V/3 A	POL 2.5 V/2 A	POL 3.3 V/2 A	
No load	0.008	0.006	0.007	0.008	0.029
10 mA	0.008	0.007	0.01	0.011	0.036
100 mA	0.027	0.03	0.036	0.037	0.13
25% full load	0.03	0.14	0.11	0.1	0.38
50% full load	0.23	0.32	0.26	0.26	1.07
100% full load	3.23	1.15	0.97	1.09	6.44

To illustrate the effectiveness of pulse-skipping, the devices in the POL design were replaced with traditional DC/DC converters operating in CCM without a pulse-skipping feature. The task to replace the components in the design was not difficult since the devices are footprint

Figure 3. DC/DC converter with advanced Eco-mode™



compatible. Table 3 shows the total dissipation for all four converters at no load and 10 mA is 242 mW, which is almost 10 times the power dissipation of the pulse-skipping converters at no-load. Using advanced Eco-mode DC/DC converters translates to a 2.1-kWh/yr savings in the POL architecture alone when operating in the standby mode. For efficiency curves and more power-loss data, please see the test report of the PMP11180 reference design.[2]

Table 3. Power dissipation with CCM converters

Load	Power Dissipation (W)				Total Dissipation (W)
	POL 1 V/5 A	POL 1.5 V/3 A	POL 2.5 V/2 A	POL 3.3 V/2 A	
No load	0.08	0.062	0.054	0.046	0.242
10 mA	0.08	0.062	0.054	0.046	0.242
100 mA	0.083	0.066	0.059	0.05	0.258
25% full load	0.066	0.14	0.11	0.1	0.416
50% full load	0.26	0.32	0.26	0.26	1.1
100% full load	3.4	1.16	0.97	1.1	6.63

Trade-offs to light-load efficiency

When a DC/DC converter enters a pulse-skipping mode, the pulses of the PWM are further apart causing the peak-to-peak output ripple voltage to increase. In most cases, the set-top box is not sending or receiving data and the tuner circuitry is less likely to be affected by noise. However, the designer must pay special attention to the ripple voltage to be sure it does not hamper performance results.

Conclusion

When designers need to reduce power consumption for every component in their product, the offline and point-of-load architecture must not be overlooked. Selecting a high-efficiency flyback controller with a synchronous rectifier controller and synchronous DC/DC buck converters with advanced Eco-mode technology will save hundreds of milliwatts of dissipation under light-load conditions. This translates to a savings of several kWh/yr without sacrificing cost or performance. Please visit our TI AC/DC and isolated DC/DC or the non-isolated DC/DC converter E2E™ forum to ask questions about implementing energy-saving features in your application.

References

1. "ENERGY STAR® Program Requirements for Set-top Boxes," Partner Commitments (Version 4.1)
2. "High Light-Load Efficient 120VAC Input, 25W/5VDC Reference Design with 4 POL Outputs," Texas Instruments reference design (PMP11180.1)
3. "High-performance DC/DC power conversion for any application," Texas Instruments power management online product folder
4. "Products for Offline and Isolated DC/DC Controllers and Converters," Texas Instruments power management online product folder

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