

# Adjusting the soft-start time of an integrated power module

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## Introduction

With the shrinking amount of available board area and the trends for shorter design times, power modules are becoming increasingly common in the industrial market. Power modules in test and measurement devices, programmable logic controller (PLC) systems and optical modules can shorten design time by reducing design effort so that engineers have more time to devote to other design tasks.

A power module integrates much of the power-supply circuitry, including some components that are normally external to the power-management integrated circuit (IC). A power module may include one or both power MOSFETs, the control loop compensation, the power inductor, the input and output capacitors, and so on. The result of all this integration is that power modules do simplify the design. However, because of their small physical size and limited pin count, a power module may have fewer features than an equivalent discrete-IC power supply.

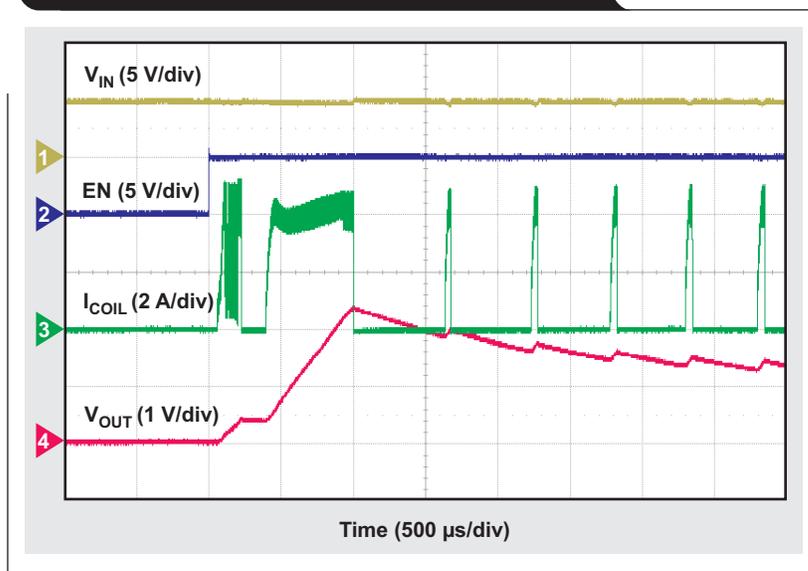
One example is the ability to adjust the soft-start time. This is fixed inside many power modules but may be configurable through a soft-start (SS) pin on a discrete-IC power supply. This fixed soft-start time, also known as output-voltage slew rate, may create unacceptable behaviors in certain applications—particularly in FPGAs, which have lots of output capacitance or may draw large currents during the soft-start time. Even with the integration of a power module, there are still several external circuits that can provide clean, acceptable soft-start times in such applications.

## The challenge: Soft-start time is too long or too short

When designing with a power module with a fixed soft-start time, it is possible that the soft-start time creates an output-voltage slew rate that is unacceptable for a particular load on the output bus. For example, an FPGA may require that its input voltage rise has a slew rate of 1 mV/ $\mu$ s  $\pm$ 50%. Since its input voltage is the output voltage of the power module, this dictates the power module's soft-start time, which may be either too long or too short for the FPGA specification.

A different scenario occurs when there is no specific slew-rate requirement, but certain application conditions

**Figure 1. Example of soft-start output into a 1-A load with two 470- $\mu$ F output capacitors**



converge to create a system-startup issue. Figure 1 shows the startup of a power module with a 5-V input voltage, the output voltage set to 2.5 V, and two 470- $\mu$ F capacitors added to the output.<sup>[1]</sup> With a 1-A resistive load added to the output, the output voltage never enters regulation because of current-limit and hiccup current-limit protection. Thus, the device remains in hiccup current-limit operation.

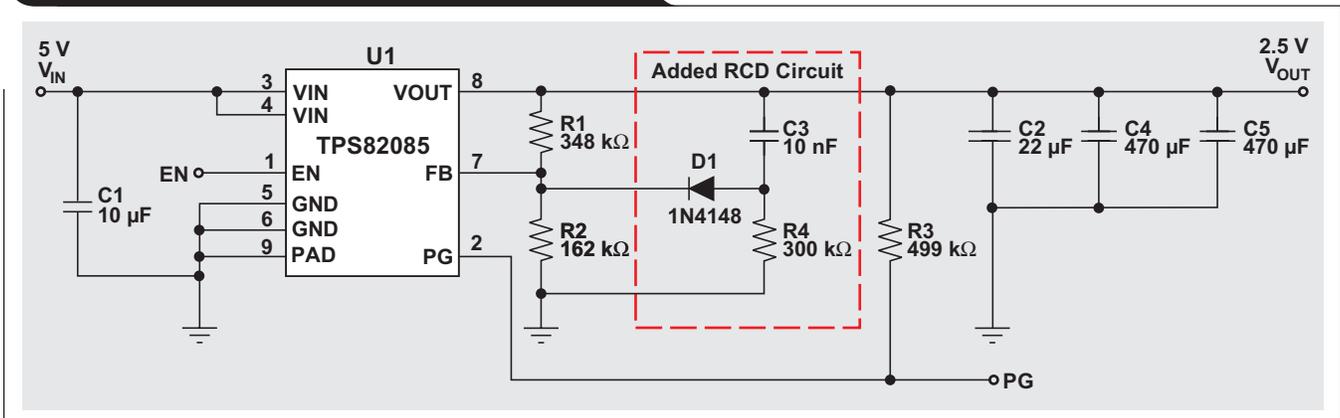
The device's internal soft-start time is fixed at 800  $\mu$ s. The device tries to ramp up the output voltage from 0 V to its set point in this time. This requires charging the output capacitance, which creates an output current shown by Equation 1.

$$I_{\text{OUT(Cap)}} = C_{\text{OUT}} \times \frac{dV}{dt} \quad (1)$$

where  $dV$  is the output voltage,  $dt$  is the soft-start time, and  $C_{\text{OUT}}$  is the total output capacitance. From the measured setup described above, the total  $C_{\text{OUT}}$  is 962  $\mu$ F (including the 22- $\mu$ F ceramic capacitor already on the output). Therefore, the output current into just the output capacitance is about 3 A.

The 1-A load current is added to this amount to obtain the entire output current of the power module. To determine the peak inductor current for the module's peak current-limit topology, half of the inductor ripple current must be added to the total output current. This value is

Figure 2. Power module with RCD circuit added



well above the 3.7-A minimum current-limit value specified in the data sheet and near the 4.6-A typical current-limit value. Figure 1 confirms this through the  $I_{COIL}$  waveform, which shows currents above 4 A. Clearly, this 3-A rated device is reaching its current limit.

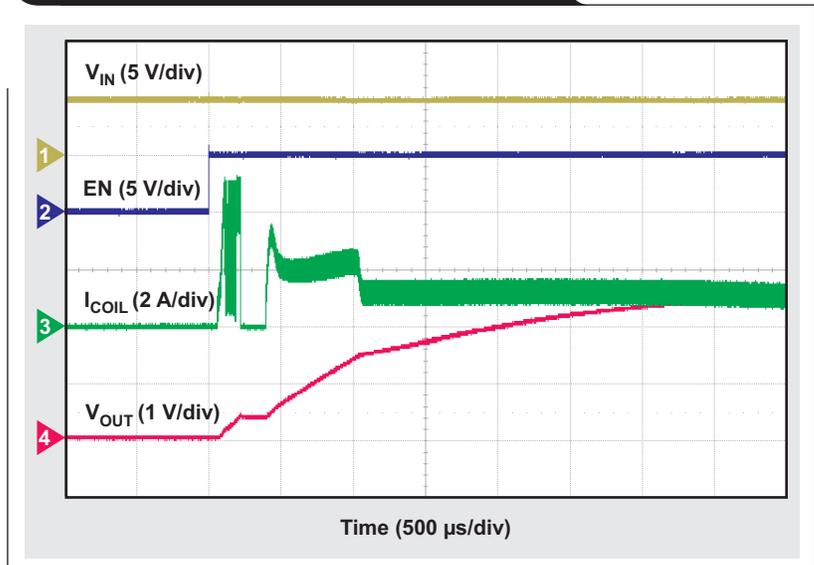
For some devices, reaching current limit during startup simply extends the soft-start time since the device operates in current limit instead of entering hiccup operation. The output voltage enters regulation for these devices. This power module behaves differently because it incorporates the hiccup current-limit protection. This type of protection turns off the device for a fixed time during a current-limit event, which limits the power dissipation and corresponding temperature rise. This keeps the overall system safer for the user in a severe fault condition. However, the fixed off-time of the hiccup current limit creates a problematic condition during startup such that the device gets stuck and the output voltage never enters regulation.

In summary, devices with hiccup current limit and a fixed soft-start time may have difficulty starting if there is a large amount of output capacitance or a heavy load present during startup.

### Solution #1: A resistor, capacitor, and diode extend the soft-start time

In applications where the soft-start time needs to be lengthened, a resistor, capacitor, and diode (RCD) circuit are added around the feedback (FB) pin in order to bias the FB pin higher and slow the startup.<sup>[2]</sup> The resistor and capacitor values are empirically tuned to lengthen the soft-start time enough for a specific application configuration. Figure 2 shows the tested schematic and Figure 3 shows the resulting startup waveform. The device enters regulation because the output-voltage slew rate and corresponding peak inductor current is reduced.

Figure 3. Soft-start with RCD circuit added



The advantage of this circuit is its simplicity, flexibility and low cost. Just three small, commodity components are required and the circuit is tunable for nearly any configuration. However, this circuit has three main disadvantages:

- This circuit only increases the soft-start time, but cannot reduce it.
- The power good (PG) output is activated before the output voltage is in regulation. Because the RCD circuit adds a voltage onto the FB pin, and this is where the PG threshold is measured. Thus, the FB and PG circuits see a voltage higher than the actual output voltage and react accordingly.
- The device still reaches its hiccup current limit, as shown by the flat part of the output-voltage ramp at around 500 mV. Since the diode does not conduct at such low voltages, the soft-start extension circuit has no effect until the output voltage is high enough. While the output voltage ramp is still mostly monotonic, this particular step may not be acceptable for all loads.

While this solution uses the same power module IC plus some extra circuitry, these disadvantages may not make it usable for every application.

### Solution #2: Use a power module with soft-start time control

The best technical solution for adjusting the soft-start time may be using a power module with an externally adjustable soft-start time. This allows adjusting the soft-start time slower or faster for almost any application configuration that specifies output-voltage slew rate. The TPS82130 is such a module that also delivers 3 A of current in the same size device. However, it is not pin-to-pin compatible due to the different feature set. Figure 4 shows its smooth startup into the same 1-A load with two 470- $\mu$ F output capacitors and a 6.8-nF soft-start capacitor.

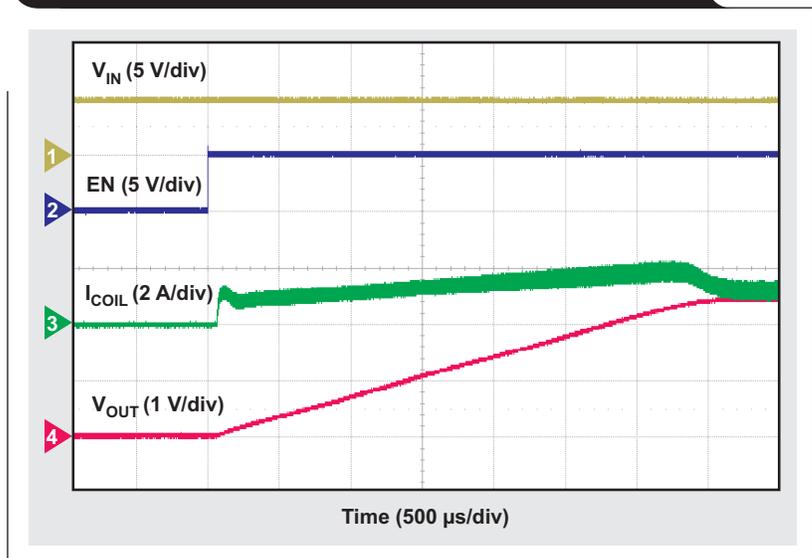
While a different power module IC addresses nearly all soft-start time concerns, there may be some disadvantages. Comparing the TPS82130 to the TPS82085, the extended input voltage range of the TPS82130 presents these downsides: lower efficiency, higher cost, taller height, and larger quiescent current ( $I_Q$ ).<sup>[3]</sup> These are the trade-offs made when selecting a different device.

Both of these power modules use the DCS-Control™ topology.<sup>[4]</sup> This topology, though internally compensated, is very tolerant of larger output capacitances.<sup>[5]</sup> Therefore, control-loop stability does not typically limit the performance with larger output capacitors. This is not always the case for other control topologies.

### Solution #3: Use a load switch to decouple loads and adjust soft-start time

A third solution uses a load switch to decouple the load from the power module. With this solution, the power

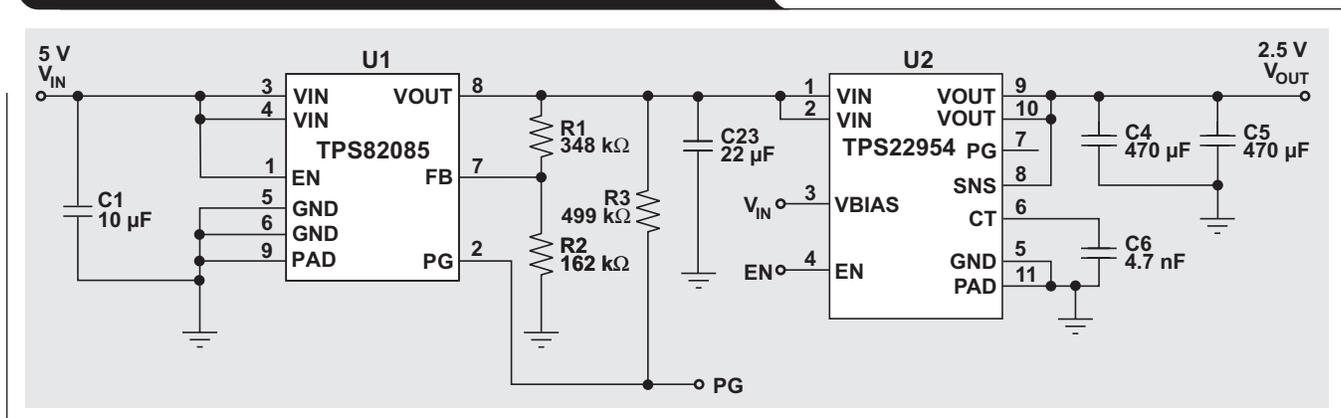
Figure 4. Power module with adjustable soft-start time



module can start up as usual without the heavy load current or the large amount of output capacitance. Alternatively, the power module can remain always on because the load switch will provide the soft-start function. Figure 5 shows an example implementation with an always on power module and the TPS22954 load switch.

A load switch with an adjustable soft-start time provides the same advantages as solution #2. Also, a load switch is useful for removing leakage currents of the load from the output voltage to reduce the standby power consumption of the system. The primary disadvantages are added cost and board area of another IC, reduced efficiency due to the conduction losses in the load switch, and decreased output voltage because of the voltage drop across the load switch. However, for systems late in the design phase and unable to make major changes to the power module device, a load switch is the simplest option to solve a soft-start issue.

Figure 5. A load switch decouples the load from the power module and adjusts the soft-start time



## Conclusion

Even with all the integration in modern power modules, engineers still have flexible solutions to overcome difficult soft-start problems found in many FPGA-based and other industrial systems with large capacitances or high startup currents. Simple and low-cost application circuits, other power-module ICs, and load switches are each able to address certain startup requirements. These options, in addition to others not listed here, are readily available to balance the trade-offs made in every design.

## References

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2. Chris Glaser, "Extending the soft start time in the TPS6107x family of boost converters," TI Application Report (SLVA307), February 2013
3. Chris Glaser, "I<sub>Q</sub>: What it is, what it isn't, and how to use it," TI Analog Application Journal (SLYT412), 2Q 2011
4. Chris Glaser, "High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions," TI Analog Application Journal (SLYT531), 2Q 2011
5. Matt Guibord, "Optimizing the TPS62130/40/50/60/70 output filter," TI Application Report (SLVA463), July 2015

## Related Web sites

Product information:

**TPS82085**

**TPS82130**

**TPS22954**

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