

Improving the thermal performance of a MicroSiP™ power module

By **Sandra Horton**, Semiconductor Packaging Group, Packaging Technology Development Engineer
Chris Glaser, Member Group Technical Staff, Senior Applications Engineer, Low Power DC DC

Introduction

Power modules are quickly gaining in popularity because of their high integration, which enables faster design time, ease of use and a smaller printed circuit board (PCB). These characteristics are important in the industrial market, but especially important in the communications equipment market (base stations, small cells, remote radio units and active antenna arrays), where channel count and data throughput increase constantly. Due to the increasing channels and data and their associated electronics, there is less available space for the power supply. Thus, a smaller power supply is required, while more time is needed to design the radio-frequency (RF) circuits instead of the power supply.

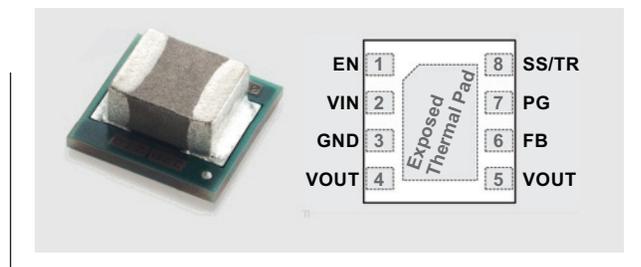
A common challenge with power modules, or any other device that must provide the same functionality in a smaller space, is thermal performance. Can a smaller power module deliver the required power in the application environment without overheating? Power-module data sheets usually state their thermal-performance properties, but they are frequently based on a Joint Electron Devices Engineering Council (JEDEC) standard PCB, which generally does not match what is possible in the actual application. This article explains JEDEC's PCB design and compares it to various real-world PCB designs that demonstrate the impact of PCB design on the thermal performance of a MicroSiP™ power module.

PCB design for thermal performance

Different power modules integrate different components, such as power MOSFETs, power inductors and loop compensation. Within the MicroSiP family of power modules, MicroSiL devices incorporate these three items. Some MicroSiPs even incorporate input and output capacitors to provide a single-component solution that requires no external components.

Figure 1 shows the TPS82130, a MicroSiL power module that accepts up to a 17-V input voltage and delivers up to 3 A of output current in a tiny 2.8- by 3-mm package that is only 1.5-mm tall. Such a wide input-voltage range is very useful for communications equipment, which often uses input voltages around 12 V, but also down to 5-V levels. MicroSiL power modules have an exposed thermal pad on their bottom side to improve thermal performance. Since this thermal pad is connected to ground potential, using vias to internal ground layers in the PCB removes heat and decreases the power-module temperature.

Figure 1. TPS82130 MicroSiL power module



Semiconductor packages, including the MicroSiP package for power modules, are designed to transfer heat to the PCB as a means of cooling the device. In most semiconductor packages, 80% to 95% of the heat transfers to the PCB as the primary way to cool the device. Only the remaining 5% to 20% of the heat dissipates directly into the ambient air. For this reason, good PCB thermal design is critical to the device's overall thermal performance. To improve PCB thermal design, you can connect copper to the device for cooling purposes by adding ground planes, increasing the copper area or growing the overall PCB size, but size constraints often make these options impossible. Thicker copper layers within the PCB also improve the thermal dissipation of the device with the same size board area.

A very effective way to improve the thermal performance of a device with an exposed thermal pad is to add thermal vias underneath the device, which tie the device's exposed thermal pad to buried layers within the PCB, as well as to the PCB's backside copper layer. The impact of adding thermal vias reaches diminishing returns after adding an optimum number of vias. Going from no thermal vias to a few thermal vias provides a very nice reduction in overall device temperature, but doubling the number of vias does not necessarily provide an additional reduction of the same magnitude. Paying careful attention to PCB layout, board construction and device mounting greatly affects the thermal performance of power applications.

The JEDEC standard

A semiconductor manufacturer has little control over the system in which their parts are used; however, the system in which the integrated circuit (IC) is mounted is critical to the device's performance. An industry-wide standard helps guide customers to understand how a particular device functions thermally and provides a normalized

point of comparison between various package types. Texas Instruments uses JEDEC thermal standards to define the thermal performance of a particular device.

JEDEC defines a certain PCB to use for thermal modeling in order to obtain the thermal metrics. The junction-to-ambient thermal resistance ($R_{\theta JA}$) is a common thermal metric, but often misused to estimate thermal performance of the device in every situation since the system's PCB is not the same as JEDEC's PCB. $R_{\theta JA}$ is a measure of the thermal performance of an IC mounted on a specific test PCB. But as stated, both the device itself and the PCB on which it is mounted impact device thermal performance. Therefore, you must have an accurate PCB design in order to estimate thermal performance in a specific application.

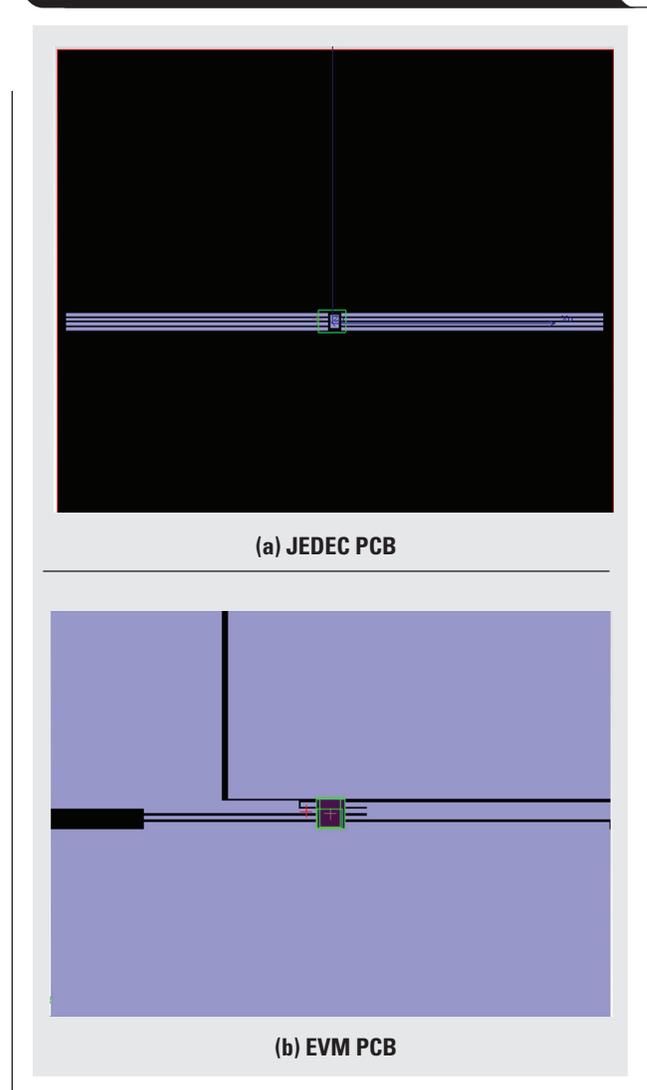
The JEDEC 51-7 PCB standard specifies the JEDEC thermal test PCB used to publish $R_{\theta JA}$ values, while JEDEC 51-5 gives details on thermal vias. To summarize, the JEDEC PCB's dimensions are $76 \times 114 \times 1.6$ mm. It has four layers, with an available copper area of 74.2×74.2 mm. Small traces connect to the power-module's pins on the top layer, layers two and three are 80% ground planes, and layer four is 20% ground plane. The copper thickness is 2 oz (0.072 mm) for the top and bottom layers and 1 oz (0.036 mm) for the interior layers. Thermal vias are located under the exposed pad with a 0.3-mm drilled via, plated with 0.025-mm thick copper and a 1.2-mm pitch between vias.

While the JEDEC PCB is a defined platform for comparing the relative thermal performance of different devices, it does not accurately represent the PCB design of communications equipment systems. TI's TPS82130 evaluation module (EVM) better represents the final application of such a system, with its dimensions of $55.8 \times 40.6 \times 1$ mm (smaller but thinner) and four copper layers occupying the entire layer. All layers use 2-oz copper and three vias that are located under the exposed thermal pad. Most importantly, the EVM's PCB uses power routing with wide planes connecting to the pins, compared to the thin traces used in the JEDEC PCB.

Figure 2 shows both the top copper layer of the JEDEC and EVM PCBs, which is used for thermal modeling. The purple elements represent copper planes on the top layer. The JEDEC PCB has much less copper on the top layer, which decreases the thermal performance.

In both the JEDEC and EVM PCBs, the three thermal vias are placed at a slightly smaller pitch in order to fit entirely beneath the exposed thermal pad. This design results in better thermal performance compared to a via spacing which pushes some of the vias under the solder mask.

Figure 2. Comparison of top copper routing for JEDEC and EVM PCBs (copper is purple color)



TPS82130 thermal performance

The TPS82130 data sheet has two sets of thermal values: one from the JEDEC PCB with thermal vias and the other from the EVM. The EVM is designed for good thermal performance and more closely matches the PCB design of typical end applications.

Table 1 compares the simulated thermal performance of various PCB designs. The EVM data in Table 1 refers to the TPS82130EVM-720 and its construction, as previously described. From this basic design and routing, modifying the vias, copper layers and airflow helps assess the thermal impact of each. Table 1 also shows the end goal of improving thermal performance: a lower operating temperature. The operating temperature is based on the TPS82130's 77% efficiency when operating at 12-V input, 1.8-V output and full 3-A load. Just through PCB design, the operating temperature drops more than 20°C compared to a JEDEC PCB that was not thermally optimized. Adding airflow enables an additional 25°C reduction.

Table 1. Thermal-performance comparison of different PCB designs

	JEDEC	EVM				
Vias	3	0	3	3	6	6
Layers	4	4	4	6	4	4
200 linear-feet-per-minute (LFM) airflow	No	No	No	No	No	Yes
θ_{JA} (°C/W)	58.2	51.4	46.1	44.6	43.8	28.3
Module temperature (°C) at full load	118.7	107.8	99.22	96.8	95.5	70.6

Table 1 shows a significant improvement when using thermal vias under the device, but a smaller improvement as the number of these vias increases from three to six. Additional copper layers beyond four, which are typically

present in 12- or 16-layer communications equipment PCBs, do not significantly improve thermal performance. Once the PCB design is optimized (with four layers and six vias), a 200-LFM airflow across the PCB dramatically improves the package's thermal capability by using the ambient air to dissipate excess heat.

TPS82130 derating

Figure 3 shows the TPS82130's derating curves for the same 12-V input, 1.8-V output system. The EVM design provides more current capability than the JEDEC PCB, and the addition of airflow dramatically increases the output current.

Conclusion

Good PCB design is critical to good thermal performance in an application. The use of thermal vias, additional copper layers and especially copper connected to the power module's pins improves thermal performance compared to the JEDEC reference PCB. A good thermal design in the application reduces temperature rise in a power module, enabling it to provide higher currents in the densest communications-equipment systems.

Related Web sites

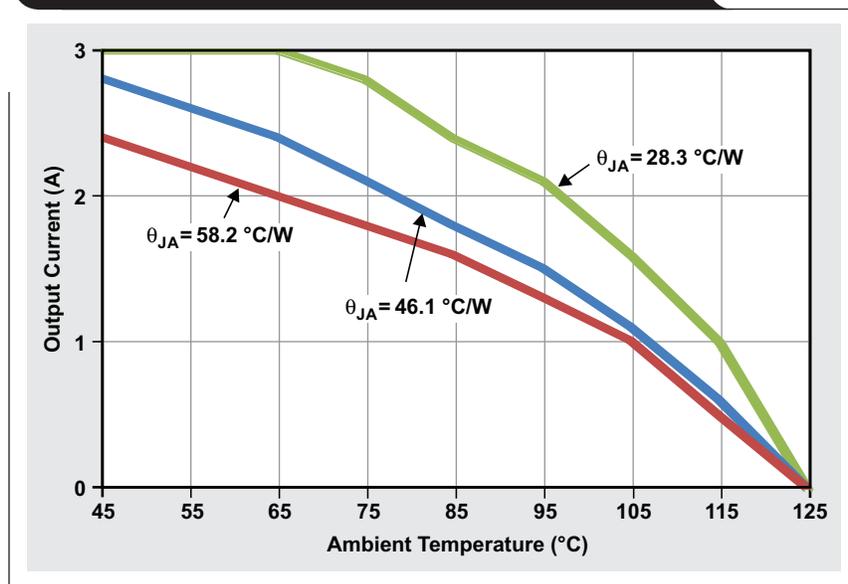
Product information:

TPS82130
MicroSiP™ and MicroSiL DC/DC Power Modules
TPS82130EVM-720 Evaluation Module

Application reports:

“Design Summary for MicroSiP™-enabled TPS8267xSiP,” Texas Instruments (SLIB006)
“Semiconductor and IC Package Thermal Metrics,” Texas Instruments (SPRA953C), April 2016

Figure 3. Derating comparison of different PCB designs



TI Worldwide Technical Support

TI Support

Thank you for your business. Find the answer to your support need or get in touch with our support center at

www.ti.com/support

China: <http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp>

Japan: <http://www.tij.co.jp/guidedsupport/jp/docs/supporthome.tsp>

Technical support forums

Search through millions of technical questions and answers at TI's E2E™ Community (engineer-to-engineer) at

e2e.ti.com

China: <http://www.deyisupport.com/>

Japan: <http://e2e.ti.com/group/jp/>

TI Training

From technology fundamentals to advanced implementation, we offer on-demand and live training to help bring your next-generation designs to life. Get started now at

training.ti.com

China: <http://www.ti.com.cn/general/cn/docs/gencontent.tsp?contentId=71968>

Japan: <https://training.ti.com/jp>

Important Notice: The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

A011617

E2E and MicroSiP are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

© 2017 Texas Instruments Incorporated.
All rights reserved.



SLYT724

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated