Op amps with complementary-pair input stages: What are the design trade-offs?

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Introduction

Operational amplifiers (op amps) designed in the 1970s typically used wide, dual supplies (such as ±15 V) with ground reference signals. Advancements in the design of op amps led to the single-supply op amp, whose common-mode input range included the negative supply rail, thereby eliminating the need for dual supplies. Decades later, however, many systems require much smaller single-supply voltages (such as 5.0 V or 3.3 V). These smaller supply voltages usually necessitate common-mode voltages that extend to both the negative and positive supply rails, which are known as rail-to-rail input devices.

Design engineers often believe that rail-to-rail input op amps have a linear input-operating range, where the common-mode voltage extends to (or slightly beyond) both of the supply rails without any variation in specifications. Unfortunately, this is not always the case.

When operating at common-mode voltages near the positive supply voltage, op amps with rail-to-rail inputs often have degraded specifications such as offset voltage, noise, and bandwidth. There are also op amps that are not considered rail-to-rail input, yet can still operate with reduced specifications at higher input common-mode voltages.

The purpose of this article is to clarify the term "rail-to-rail input" with regard to op amps. Similar to how the definitions of "wide bandwidth" and "low offset voltage" have changed over the years, rail-to-rail input can have various meanings.

Traditional PNP-transistor input stage

Figure 1 displays a simplified schematic of a traditional design for a p-channel, n-channel, p-channel (PNP) transistor input stage. Input stages with this design typically have common-mode voltage-input ranges that include V_{EE} but only go within 1 or 2 V of V_{CC}. When these types of devices were first released, they were referred to as single-supply op amps because their input common-mode voltage includes V_{EE}. This enabled designers to connect V_{EE} to GND and still accept GND-referenced input signals.

Phase inversion (or phase reversal) was a common issue with amplifiers that use this architecture, along with junction field-effect transistor (JFET) and some bipolar FET (BiFET) devices. It occurs when the input common-mode voltage exceeds the linear operating region of the amplifier input, which is not necessarily greater than the supply-voltage range. When the common-mode voltage exceeds the linear operating region, one of the transistors in the input stage is not biased properly and causes the output voltage to invert.

Figure 1. Typical PNP transistor single-supply input stage

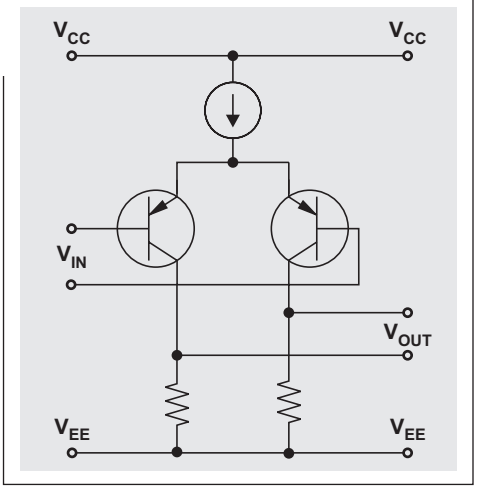


Figure 2 displays the input and output voltage of an amplifier that suffers from phase inversion. Notice that when the common-mode voltage goes outside the common-mode voltage limits of the device, the output voltage becomes inverted.

Figure 2. Phase inversion (reversal)

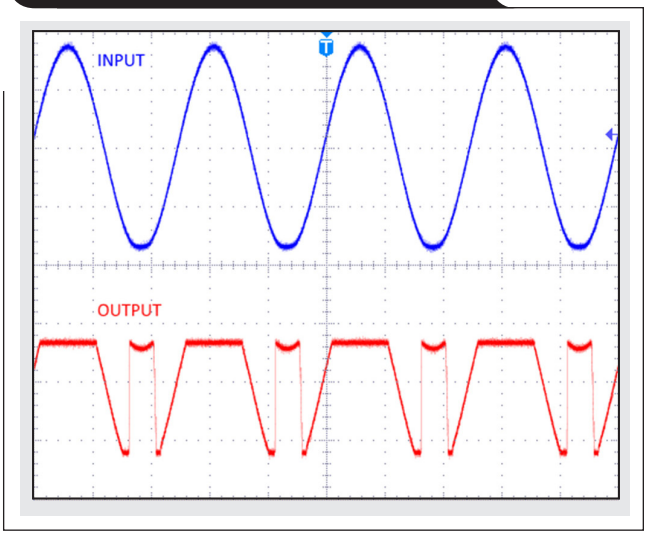
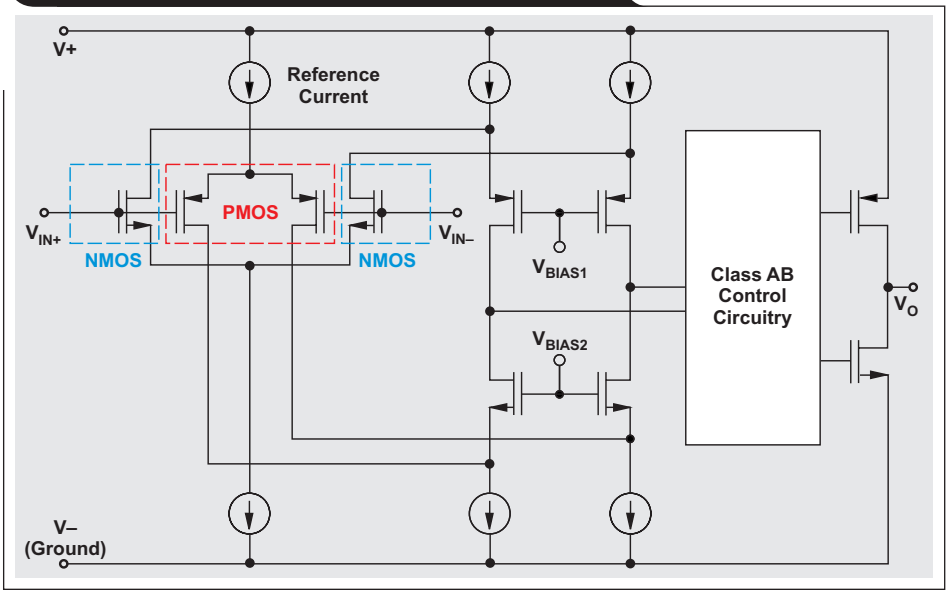


Figure 3. Input stage with complementary pair



One technique that can mitigate this issue is to use the device in an inverting configuration so that the common-mode voltage does not change with the input voltage. Another common technique is to place a resistor in series with the input (to limit the current) and Schottky diodes from the input node to the power-supply rails, thus reducing the likelihood that the input will exceed the supply rails by more than the forward voltage drop of the Schottky diodes. However, this technique is not necessarily effective for op amps whose common-mode voltage range is well within the supply rails and also requires external components, which adds cost and printed circuit board (PCB) area to the design.

Complementary-pair input stage

Phase inversion in amplifiers is eliminated internally by designing the input stage of the amplifier using a complementary pair of transistors, which is also sometimes known as an anti-phase-reversal differential pair. A complementary-pair input uses dual p-type metal-oxide semiconductor (PMOS) transistors and dual n-type metal-oxide semiconductor (NMOS) transistors for the differential inputs. Figure 3 shows a simplified schematic of an op amp with a complementary-pair input stage. Compared to the traditional input stage design, there is an additional NMOS transistor pair.

Figure 4 shows a plot from a modern data sheet that depicts a device without phase reversal.

Figure 4. No phase reversal

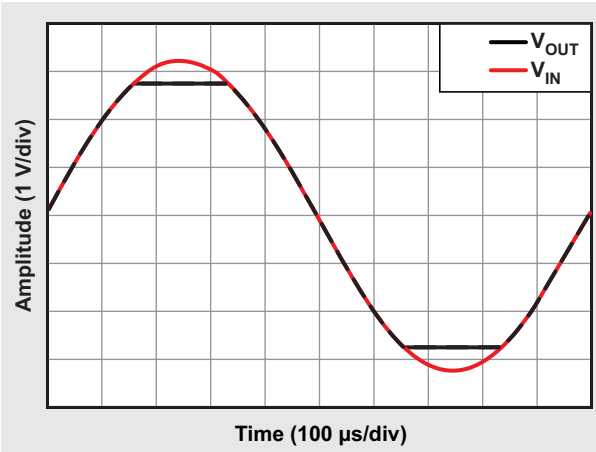
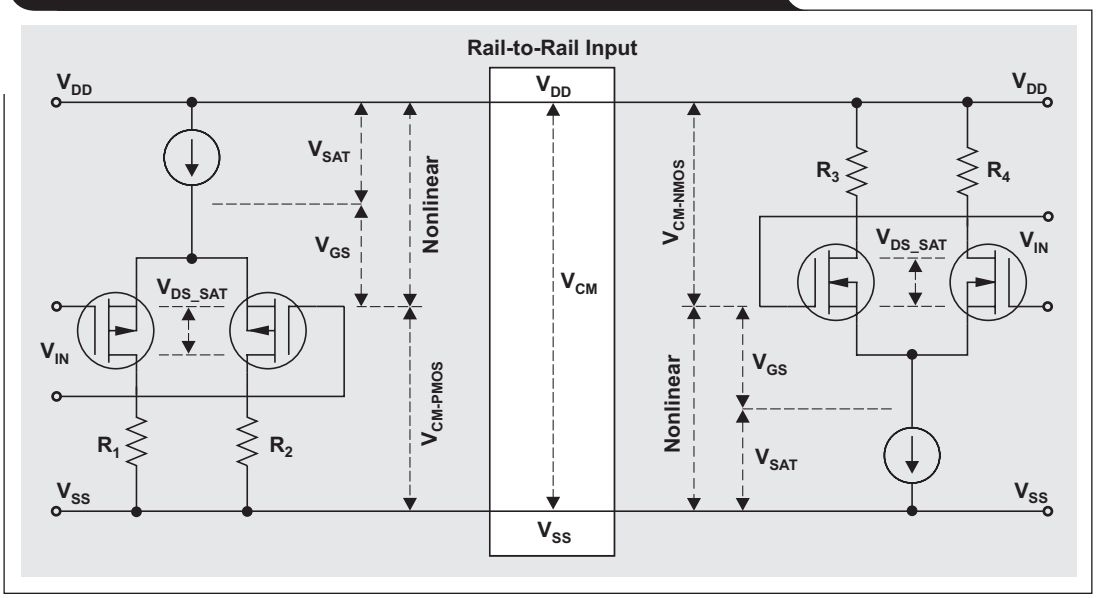


Figure 5. Complementary-pair common-mode voltage range



Common-mode range of devices with complementary-pair differential inputs

The complementary-pair inputs allows the common-mode voltage to extend to the supply rails without phase inversion. In a design with a complementary-pair input stage, the PMOS transistors enable operation slightly below the negative supply and the NMOS transistors allow for operation slightly above the positive supply. As the input common-mode voltage increases from V_{SS}, the PMOS transistors go into the cutoff region and the input transitions to the NMOS transistors, which enables operation above the positive supply. Figure 5 is a graphical representation of how the transition occurs.

The linear range of the PMOS input pair is calculated by using Kirchhoff's voltage law from the negative supply voltage (V_{SS}) to the input (V_{IN}) and from the positive supply voltage (V_{DD}) to the input (V_{IN}). Equation 1 shows the linear range of the PMOS input pair.

$$V_{CM} > V_{SS} + V_{R1/2} + V_{DS\_SAT} - V_{GS}$$
$$\text{and} \quad (1)$$
$$V_{CM} < V_{DD} - V_{GS} - V_{SAT}$$

The linear range of the NMOS input pair is calculated in the same manner as the PMOS input pair. Equation 2 shows the linear range of the NMOS input pair.

$$V_{CM} > V_{SS} + V_{SAT} + V_{GS}$$
$$\text{and} \quad (2)$$
$$V_{CM} < V_{DD} - V_{R3/4} - V_{DS\_SAT} + V_{GS}$$

Since the input stage uses both PMOS and NMOS transistors, combining Equations 1 and 2 gives the linear-input common mode of the complementary-pair inputs. Equation 3 depicts the linear input-voltage range of the combined input stage.

$$V_{CM} > V_{SS} + V_{R1/2} + V_{DS\_SAT} - V_{GS}$$
$$\text{and} \quad (3)$$
$$V_{CM} < V_{DD} - V_{R3/4} - V_{DS\_SAT} + V_{GS}$$

The transition from the PMOS transistor pair to the NMOS transistor pair (commonly referred to as the input-crossover region) causes a variation in performance. This is because the characteristics of the PMOS transistors are not exactly the same as the NMOS transistors.

When the characteristics of the PMOS transistors and NMOS transistors are significantly different, the performance of the device in the upper common-mode voltage range has significantly degraded specifications compared to operation in the lower common-mode voltage range. Such devices are typically not marketed as rail-to-rail input devices, but are capable of having rail-to-rail inputs without phase inversion. Two examples of such amplifiers include the OPA171 (36 V) and OPA376 (5 V). The OPA171, for example, is considered a single-supply amplifier because the common-mode range includes the negative supply. The common-mode range can only come within approximately 2 V of the positive supply before experiencing a significant degradation in specifications.

Figure 6 depicts the offset voltage versus common-mode voltage for the OPA171. Notice the dramatic increase in offset voltage when the common-mode voltage transitions from the PMOS to the NMOS pair.

Table 1 compares additional parameters of the OPA171 in the PMOS region to the NMOS region. Clearly, the performance of the NMOS region of operation is reduced from both an AC and DC perspective. The NMOS transistors do, however, protect against phase inversion.

Some devices, such as the TLV9062, have complementary-pair input stages whose NMOS and PMOS pairs are inherently more closely matched. These devices will be marketed as rail-to-rail input devices. Figure 7 shows a much smaller common-mode voltage transition between the PMOS and NMOS pairs of the TLV9062.

Parameters such as power-supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), offset voltage, offset voltage drift and total harmonic distortion (THD) will have degraded performance in the transition region and during operation in the NMOS region. However, the performance is still reasonable compared to the PMOS pair. In support of this, all of the aforementioned parameters are specified over the entire common-mode voltage range in the product data sheet with the exception of CMRR. The typical CMRR specification decreases only 16 dB when comparing PMOS region performance to that of the entire common-mode range.

Figure 6. V_{OS} versus V_{CM} for the OPA171

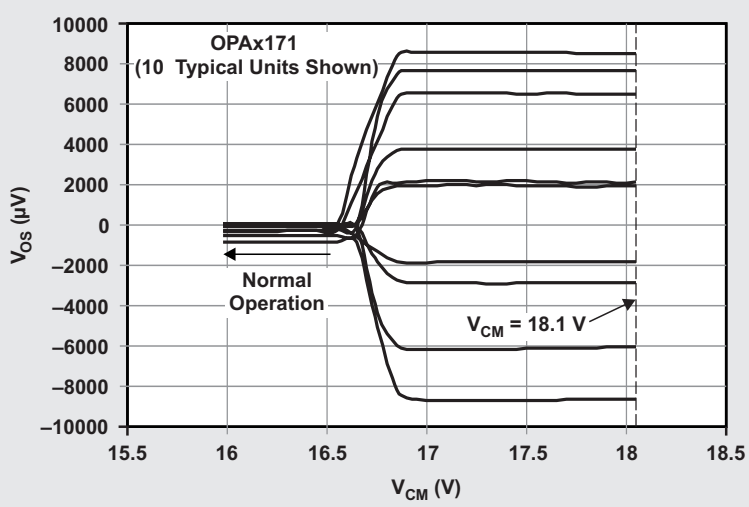
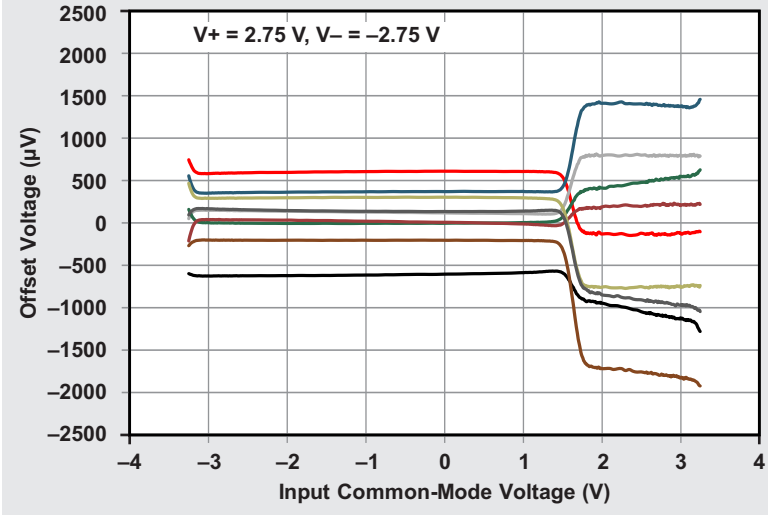


Table 1. OPA171 specification comparison between PMOS and NMOS regions

Parameter	PMOS (typical)	NMOS (typical)	Units
Offset voltage (V_{OS})	0.25	7	mV
Offset voltage vs. temperature (dV_{OS}/dT)	0.3	12	µV/°C
Common-mode rejection (CMRR)	120	65	dB
Open-loop gain (A_{OL})	130	60	dB
Gain bandwidth (GBW)	3.0	0.7	MHz
Slew rate (SR)	1.5	0.7	V/µs
Noise at f = 1 kHz (en)	14	30	nV/√Hz

Figure 7. Offset voltage versus common-mode voltage for the TLV9062



For optimal performance over the entire common-mode voltage range, some devices have trimmed PMOS and NMOS transistors. The OPA191, for example, trims the transistors to further match the performance of both complementary pairs, as shown in Figure 8.

While these devices still have a crossover region, the PMOS and NMOS performance after trimming is excellent, as shown in Figure 9.

Although the performance with respect to specifications such as CMRR will degrade, the initial performance is far better than untrimmed designs. For example, the typical CMRR performance in the PMOS region is 140 dB, but it's still 120 dB in the NMOS region.

Conclusion

The term rail-to-rail input can sometimes be misunderstood. Many designers interpret the term as devices that have the same performance over the entire range of the input common-mode voltage. However, devices such as the OPA171 have a complementary pair where the performance of the NMOS input pair is not as good as the primary PMOS pair. These devices do not exhibit phase inversion but do suffer from performance degradation near the positive supply rail.

Devices with better matching between the PMOS and NMOS input pairs, such as the TLV9062, will be marketed as having a rail-to-rail input, and consequently a smaller shift in performance over the entire common-mode range. Trimmed input pairs like those found in the OPA191 have overall better performance in both regions of operation, although there is still a crossover region. It is recommended that designers thoroughly examine the data sheet to ensure that the desired device operates as required in all common-mode regions.

Related web sites

Product information:
OPA171
OPA376
OPA191
TLV9062
Operational amplifiers

Figure 8. OPA191 trim

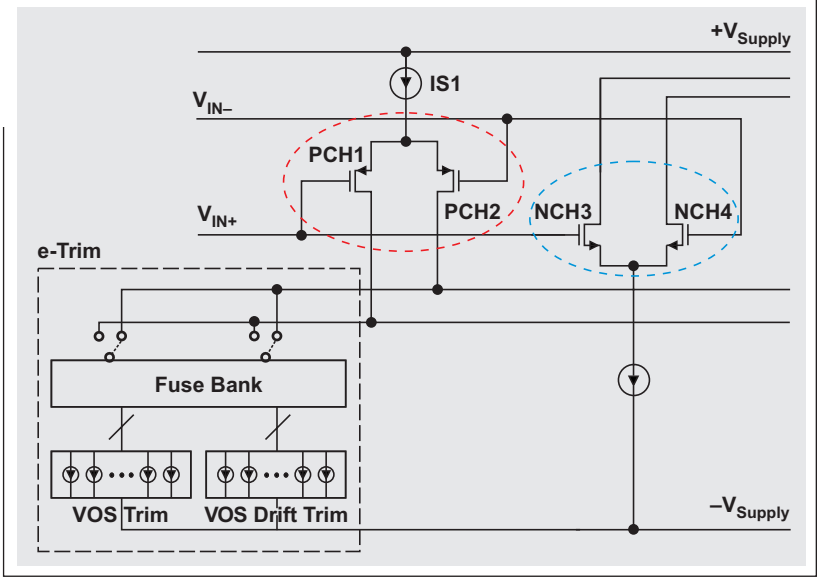
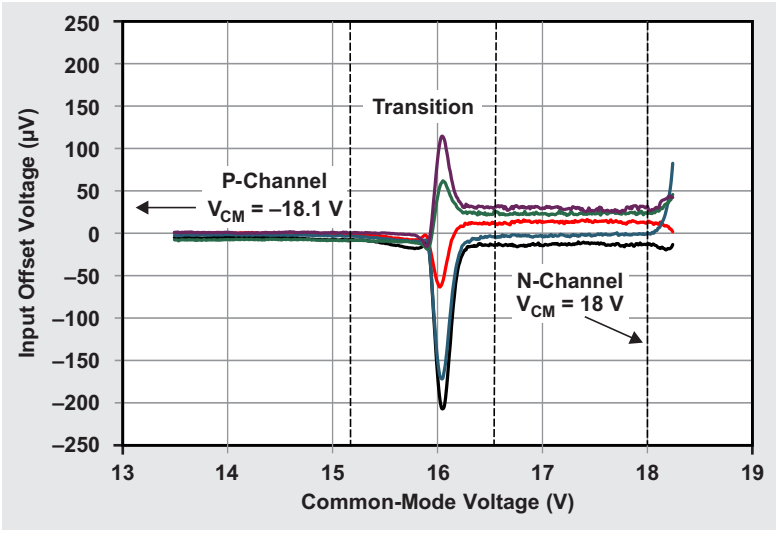


Figure 9. Input-offset voltage versus common-mode voltage for the OPA191



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