

# Designing PoE switching supplies for input power sharing and with power limiting

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## Introduction

Power sharing and power limiting are common requirements for systems that have multiple power inputs. One common approach is to apply even current sharing between power-supply modules based on an output current measurement from each module, as shown in Figure 1. One drawback of even current sharing is that this solution only applies when both channels are allowed to draw similar amount of power. Also, since the sharing is based on current measured at the output, the accuracy of input power sharing is then influenced by the relative efficiency of each DC/DC converter stage.

Some applications require a more universal approach to power sharing and power limiting, one example being power over Ethernet (PoE), which in some cases requires “uneven” power sharing in addition to input power limiting per power feed. The reason that is each power feed may have a different power allocated by the remote

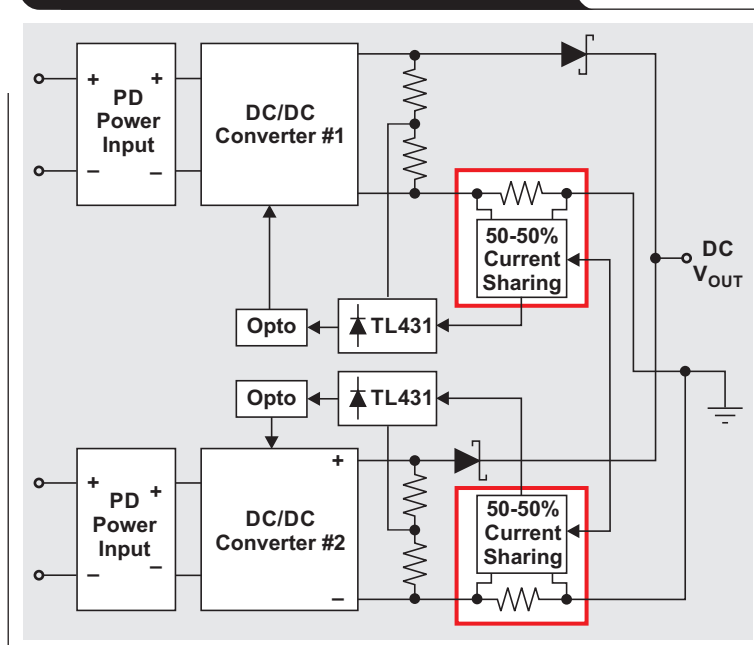
power-sourcing equipment (PSE), and the powered equipment is not allowed to exceed this negotiated power level.

PoE offers a convenient way to deliver electrical power through Ethernet cables. As defined in the Institute of Electrical and Electronic Engineers (IEEE) 802.3at and 802.3bt standards, after having detected a valid powered device (PD), the power sourcing equipment (PSE) typically proceeds through a physical layer classification. The PSE first inquires how much power the PD requires, signaling to the PD how much power it will actually allocate, and then providing power to the PD. The PD input power is not allowed to exceed the allocated power.

Equipment that needs a sum of power from multiple power feeds requires a control mechanism to meet the IEEE requirements. An application example is a compact switch which is typically powered by PoE cables and provides power to multiple loads through PoE output cables.

The challenges are many and include power measurement and accuracy.

**Figure 1. Top level view of an architecture with even current sharing**



### An input power-limiting solution

The best solution would combine individual input power limiting and input power summing with good accuracy and high efficiency.

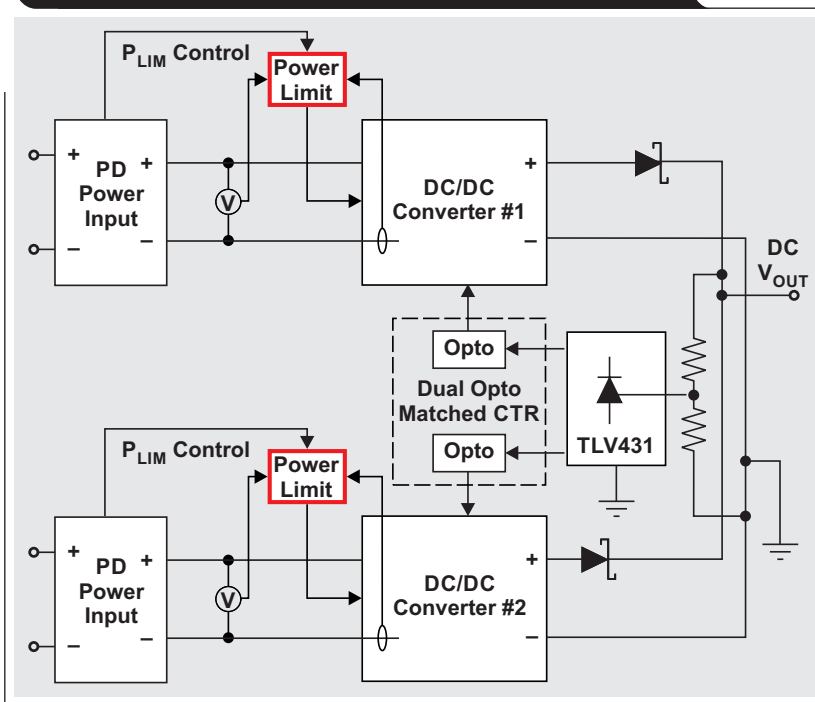
The solution shown in Figure 2 centers around a measurement of the input current and voltage. The figure illustrates a system with two input power feeds, although the same concept could apply to any number of input channels. Each of the two converters contribute to the total power delivered and each one delivers power up to its individual power limit. The single common regulation stage with a dual optocoupler, preferably with a limited current transfer ratio difference, is a reasonable choice if there is a need for “good” power sharing until one converter stage reaches its individual power limit.

$P_{LIM}$  Control is typically generated by the PD and reflects the level of power allocated by the PSE to the PD during physical layer classification. The  $P_{LIM}$  Control signal is then used to control the input power limit of the DC/DC converter stage.

Figure 3 shows more details about how this concept works. The summer is fed by the average input current signal and a signal proportional to the input voltage.  $V_{REF}$  is adjustable according to the power-limit setting. If the power limit is reached, the output of the power-limiting comparator (COMP) to the controller is forced down to keep power at the limit. Note that the impact is on only the current loop when the power limit is reached and the COMP action is transparent to the voltage loop.

Power limiting means that the power measurement needs to be accurate when close to the power-limiting operating point. Such accuracy is not necessary when the operation is far from that point. Mathematical analysis reveals that accuracy depends on the input voltage range of operation. Analysis shows that varying the input voltage within a range from 42.5 V to 57 V will introduce an error lower than  $\pm 1.5\%$ . If the input voltage varies from 37 V to 57 V, the error introduced is lower than  $\pm 2.5\%$ .

**Figure 2. Top-level view of an input power-sharing/ power-limiting architecture**



**Figure 3. The concept of power limiting**

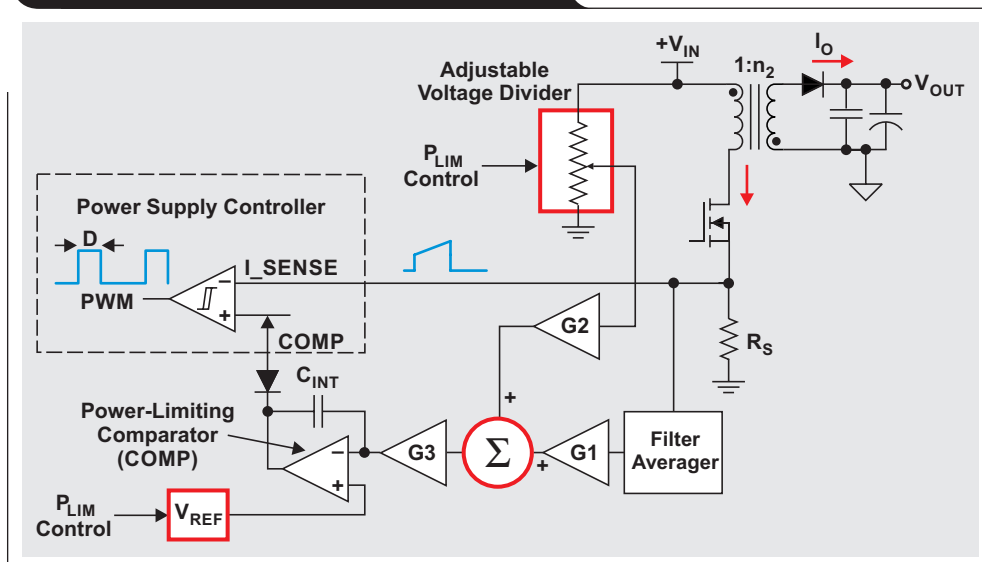


Figure 4 illustrates the mathematical predictions, assuming the maximum settings for each of the 13-W, 25.5-W and 51-W power categories (Types 1, 2 and 3). In practical implementations, it is important to also consider error contributors and allow some margin while still meeting the IEEE 802.3at or 802.3bt specifications.

At a system level, one of the benefits is that the power being measured at the input means that the power-supply efficiency has no impact on power-limiting accuracy. Also, no additional power current-limiting resistor is needed. Since the power limit is based on the average (and not the peak) current measurement, its accuracy is independent of power-supply parameters like magnetizing and leakage inductance and variations in switching frequency.

### Input power-limiting implementation

The input power limit is applied in three stages using a combination of operational amplifiers and a reference. These stages are the current-measuring, feed-forward adder, and COMP pull-down circuits.

Figure 5 shows a noninverting amplifier that takes the switching current from the sense resistor of a current-mode-controlled DC/DC converter and outputs its average primary current.

Since the primary current is switching, a low-pass filter is used at the input of the current amplifier. Using two resistor-capacitor (RC) filters will enable the first-stage RC filter to remove high-frequency noise, which can add to the averaging of the second-stage RC filter. The gain of the amplifier should be adjusted based on the expected voltage of the reference threshold and the added feed-forward voltage.

Figure 4. Power-limiting predictions

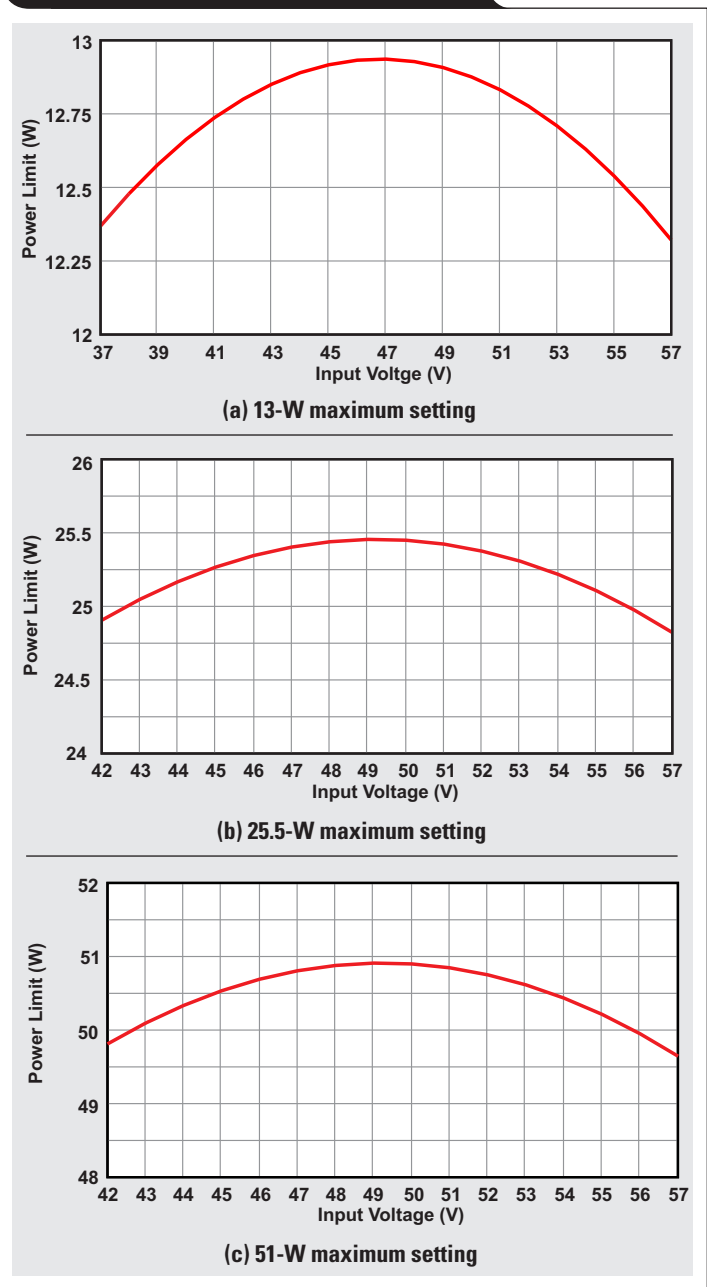
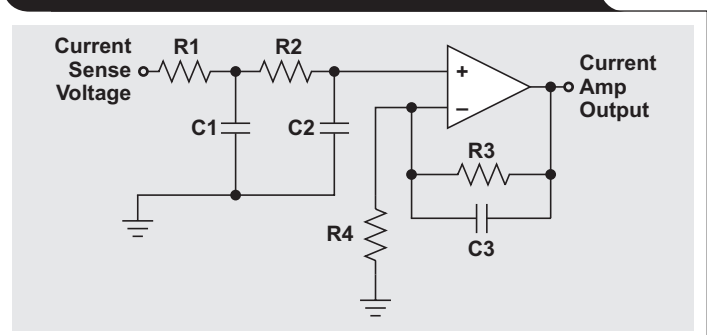


Figure 5. Noninverting current-sense amplifier



The IEEE802.3bt standard allows for up to 100 meters of Category 5 Ethernet (CAT5e) cable. This means that the voltage at a PoE PD and DC/DC converter load can vary within a wide range depending on the power level. The feed-forward circuit shown in Figure 6 minimizes the effect of the input voltage on power limiting of a DC/DC converter.

The summing amplifier circuit shown in Figure 6 will add an offset to the input current amplifier that is proportional to the buffered input voltage. As an example, if the input voltage is a higher voltage range due to a short cable length, the offset will be higher to negate a higher power limit in the absence of feed forward.

The COMP pull-down circuit shown in Figure 7 uses an integrator to pull its output lower when its input (the output of the summing amplifier) reaches the power-limiting threshold dictated by the reference circuit and its resistor divider.

While the DC/DC converter is in power limiting and the output power is increased, COMP will pull down harder to keep the output power limited.

### Design considerations

Because the reference sets the power-limiting threshold, a high-accuracy reference is chosen so that the power limit does not change much with temperature and input variations. The reference threshold is chosen so that it is much larger than the input offset introduced by the operational amplifiers. To minimize the effect of amplifying the input offset at each amplifier stage, minimize adding gain at each stage: this solution only adds a gain factor in the current amplifier stage.

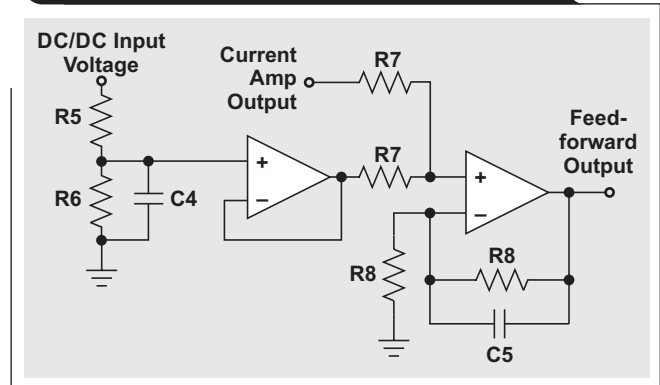
Three simplified equations can give an estimate of gain. Equation 1 expresses the power-limiting threshold:

$$\text{Power\_Limit}_{th} = V_{\text{Reference}} \frac{R_{12}}{R_{11} + R_{12}} \quad (1)$$

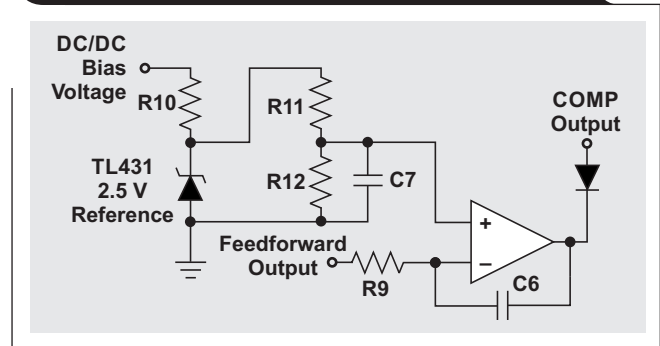
Equation 2 calculates the output of the adder stage. This signal accurately reflects the input power only when it is near  $\text{Power\_Limit}_{th}$ .

$$V_{\text{OUT\_Feedforward}} = V_{\text{IN\_DC/DC}} \frac{R_5}{R_5 + R_6} + A_{\text{CurrentAmp}} \frac{P_{\text{Max}}}{V_{\text{IN\_DC/DC}}} R_{\text{Sense}} \quad (2)$$

**Figure 6. Summing amplifier with power-limiting feed forward**



**Figure 7. Power limiting comparator circuit**



Since it is known that the input of the current amplifier is the average input current of the DC/DC converter, the gain of the current amplifier can be determined by setting the feed-forward output equal to the power-limiting threshold. The result is the gain shown by Equation 3:

$$A_{\text{CurrentAmp}} = 1 + \frac{R_3}{R_4} = \frac{\left( V_{\text{Reference}} \times \frac{R_{12}}{R_{11} + R_{12}} \right) - \left( V_{\text{IN\_DC/DC}} \times \frac{R_5}{R_5 + R_6} \right)}{\frac{P_{\text{Max}}}{V_{\text{IN\_DC/DC}}} \times R_{\text{Sense}}} \quad (3)$$

### Test results

Power limiting was implemented in a power-sharing reference design for a dual-input PoE IEEE802.3bt PD. The TPS2373-3 PoE PD is capable of identifying the power allocated to the PD through output logic signals gained during hardware classification. The power-limiting threshold can be adjusted for different power levels based on the power allocated by the PSE by using simple logic with field-effect transistors and resistors to change the reference threshold and feed-forward voltages. The result is a single DC/DC converter capable of Type 1 (13 W), Type 2 (25 W) and Type 3 (51 W) power limits, as shown in Figure 8.

### Power limiting in power-sharing applications

When limiting power in power-sharing applications, each converter will output the maximum power dictated by the power-limiting threshold. The added benefit is that the sharing is not dependent on how well the output current is shared by each converter, as shown in Figure 9.

The two converters have less than 60/40 sharing; however, the power on the higher-percentage-sharing converter will continue to output power until it reaches its power limit, at which point, the lower-percentage-sharing converter will continue providing limited power. This power-limited split eliminates the need for costly current-sharing controllers. The maximum shared output is not limited by the current-sharing accuracy and is independent of each converter's efficiency since power is sensed at the converter's input.

### Conclusion

Power-sharing applications are becoming prevalent in PoE applications as end-equipment requires higher power. Even though the IEEE802.3bt standard allows for up to 71 W of power at the PoE PD, a PSE can allocate lower-type power levels. Power sharing two PoE inputs helps achieve higher power.

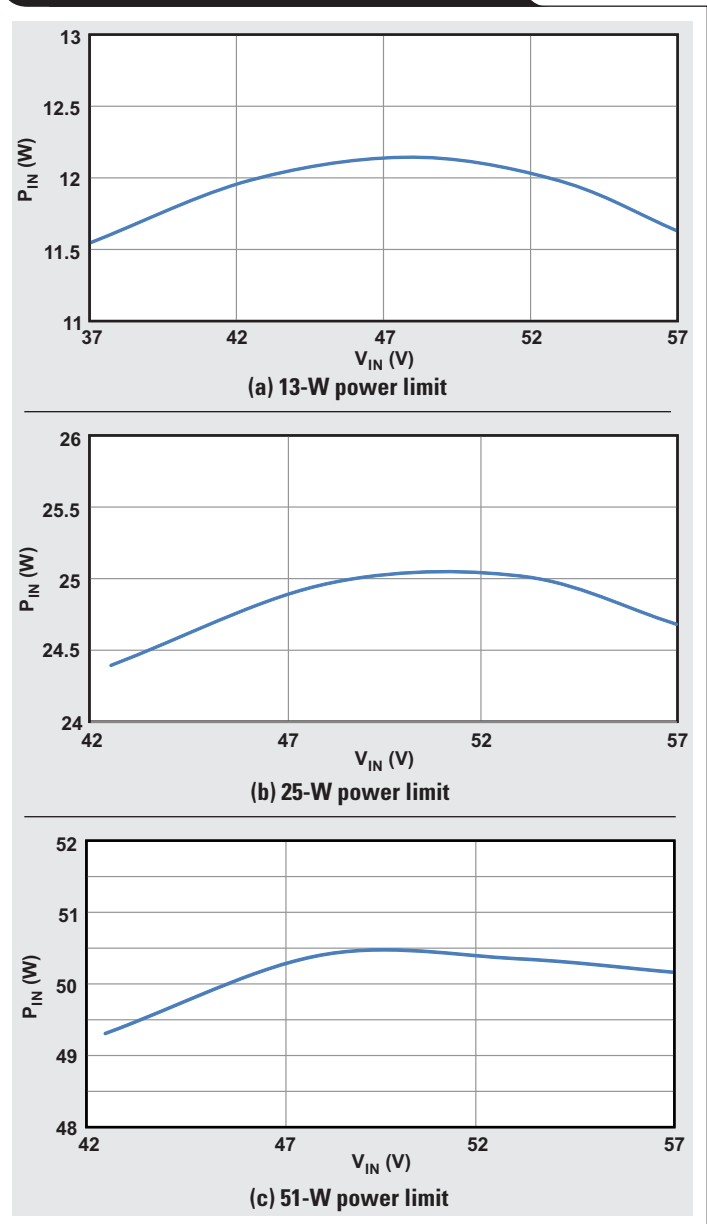
A power-limiting circuit that is independent of converter efficiency can be paired with a partial power-sharing design to use the maximum output power from the input PSE. This approach saves system-level costs versus a high-accuracy power-sharing solution using current-sharing controllers.

### Related Web sites

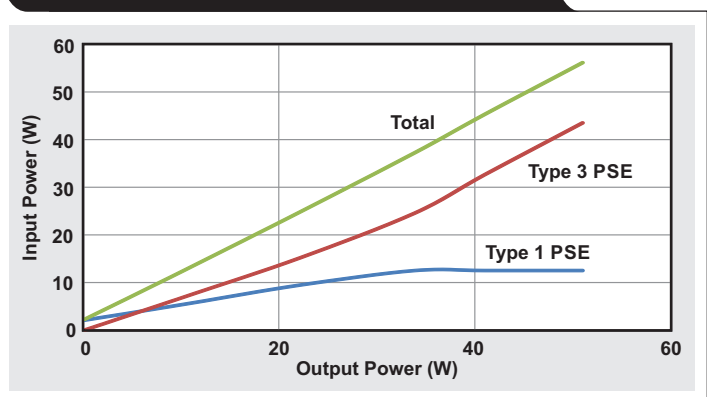
Product information:

**Power over Ethernet (PoE) Solutions  
TPS2373**

**Figure 8. Power-limiting bench results**



**Figure 9. Power sharing of two converters with power limiting**



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