Designing high-performance PWM DACs for field transmitters

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Introduction

Pulse-width modulation (PWM) is a common design method for representing voltage in control electronics because controlling timing accuracy in integrated circuits is easier than controlling voltage accuracy. Integrated digital clock dividers can generate accurate fractions from a clock references much easier than a typical analog-to-digital converter (ADC) can generate accurate fractions from a voltage reference. PWM control is widely used in power conversion, LED luminance control, motor control and telecommunications.

PWM-based digital-to-analog converters (DACs) are common in field transmitters due to their simplicity, robustness and cost. However, achieving high resolution over a relatively wide bandwidth is particularly challenging for the classical PWM DAC implementation because a DAC requires an excessively high-frequency clock.

This article explains different techniques to overcome classical PWM DAC limitations and how to reduce power consumption, followed by the design and validation of a high-performance PWM to 4- to 20-mA transmitter stage that employs these techniques.

Analyzing a PWM signal

Figure 1 shows a generic PWM signal of period (T_P), peak-to-peak amplitude (V_P) and pulse width (DT_P), where D is a fraction between 0 and 1.

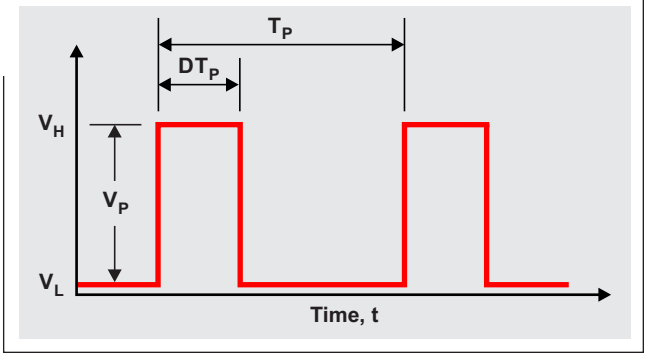
Equations 1 and 2 define the PWM frequency (f_P) and V_P, respectively.

$$f_P = \frac{1}{T_P} \tag{1}$$

$$V_P = V_H - V_L \tag{2}$$

where V_H and V_L are the high and low voltages of the digital output stage, respectively.

Figure 1. Generic PWM signal

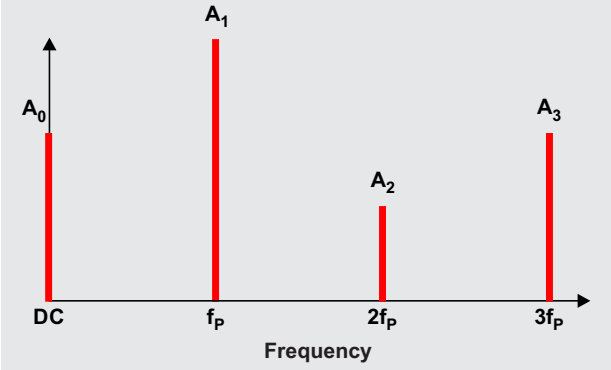


In steady state, and with little mathematical manipulation, Equation 3 computes the Fourier series representation of the former PWM signal.

$$f(t) = A_0 + \sum_{n=1}^{\infty} A_n \times \cos(2n\pi f_P t) \tag{3}$$

Equation 3 contains terms at DC, as well as terms of harmonics of f_P. See Reference 1 for the application report that shows more details of the derivation. Of specific interest are the magnitudes of those terms at DC and at the PWM frequency harmonics shown in Figure 2.

Figure 2. Frequency-domain representation of PWM Fourier series coefficients



Equations 4 and 5 show the DC and the harmonic terms magnitude in the PWM signal.

$$A_0 = D \quad V_P \tag{4}$$

$$A_n = \frac{V_P}{n\pi}\left\{\sin(n\pi D) - \sin\left[2n\pi\left(1 - \frac{D}{2}\right)\right]\right\} \tag{5}$$

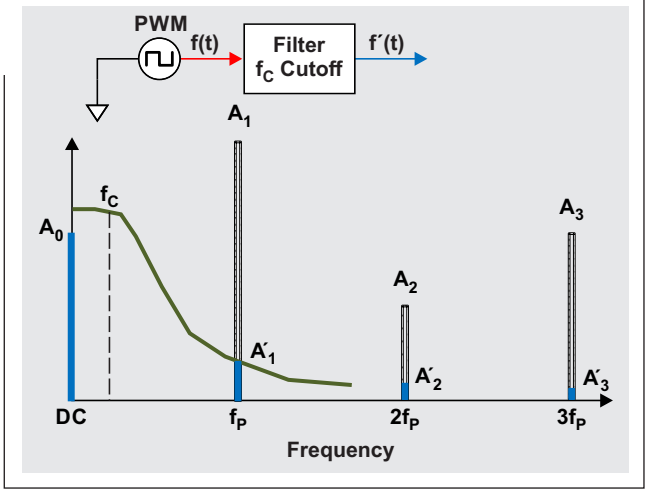
The value at DC A_0 equals the PWM signal's peak-to-peak magnitude multiplied by the duty cycle (D) and represents the desired DAC output. The other higher-order terms result in errors on top of the desired output; their values depend on both D and the harmonic order (n). The worst-case error occurs due to a first-order harmonic when D = 0.5, shown in Equation 6.

$$A_1 = \frac{V_P}{\pi} \text{ at } D = 0.5 \tag{6}$$

The high-order harmonics are typically suppressed by a low-pass filter of order (m) and cutoff frequency (f_C). Figure 3 shows the output of this low-pass filter, represented in Equation 7.

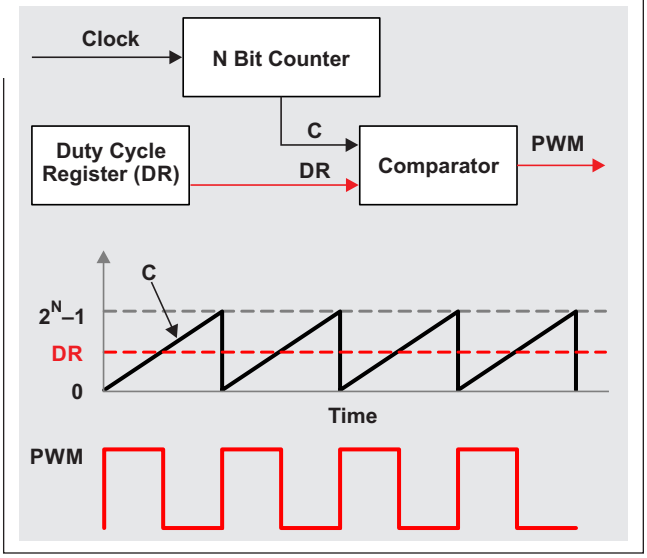
$$A_1' = A_1\left(\frac{f_C}{f_P}\right)^m \quad (7)$$

Figure 3. PWM filter-output Fourier coefficients



Most microcontrollers (MCUs) generate PWM signals using a hardware structure similar to the one shown in Figure 4. Simply put, a counter—counting up and resetting when reaching a specified limit—determines the PWM period and frequency. Another level set by the duty-cycle register determines when the PWM output switches from high to low. The "Timer_A" chapter excerpt[2] from the MSP430™ User's Guide[3] describes this hardware structure, and the application note, "Dual-Output 8-Bit PWM DAC Using Low-Memory MSP430 MCUs,"[4] explains how to use the hardware for generating PWM signals.

Figure 4. A simple MCU PWM generator and waveforms



With such a PWM signal generator, Equation 8 represents f_P as:

$$f_P = \frac{f_{CLK}}{2^N} \quad (8)$$

where f_{CLK} is the MCU clock frequency and N is the counter depth in bits.

The structure in Figure 4 implies that there is a minimum value of duty cycle that can be generated as expressed by Equation 9.

$$D_{min} = \frac{1}{2^N} \quad (9)$$

Equation 9 sets the minimum increment (or resolution) for a DAC output that is possible using such a structure. However, the uncertainty of the output exceeds the resolution due to the harmonics components left after filtering. Filter-output ripples appear like noise and reduce the effective number of bits (ENOBs) of the DAC.

Equation 10 defines this total uncertainty (TU) as the sum of minimum resolution and ripples.

$$TU = D_{min} \times V_P + \frac{V_P}{\pi}\left(\frac{f_C}{f_P}\right)^m \quad (10)$$

Substituting D_{min} from Equation 9 into Equation 10 results in Equation 11.

$$TU = \frac{V_P}{2^N} + \frac{V_P}{\pi}\left(\frac{2^N \times f_C}{f_{CLK}}\right)^m \quad (11)$$

Equation 12 defines the relative filter bandwidth (BW).

$$BW = \frac{f_C}{f_{CLK}} \quad (12)$$

Equation 13 rewrites the uncertainty as a function of this relative filter bandwidth, and normalizes it by dividing by the peak-to-peak level.

$$TU_{normalized} = \frac{1}{2^N} + \frac{1}{\pi}\left(2^N \times BW\right)^m \quad (13)$$

Equation 13 enables the ENOBs to be written as a function of relative bandwidth with Equation 14.

$$ENOBs = \frac{-\log\left(TU_{normalized}\right)}{\log(2)} \quad (14)$$

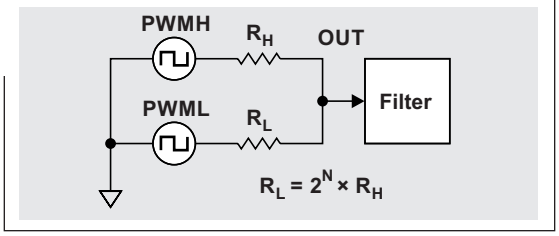
Plotting this function with different values for N and m, as shown in Figure 5, reveals an interesting fact: The PWM architecture has an intrinsic limitation, achieving high resolution over a reasonable bandwidth. For example, if N = 12 bits, and assuming that f_{CLK} = 16 MHz, it is only possible to achieve 12-bit ENOBs (with f_{PWM} = 4 kHz) by using a third-order filter, up to a bandwidth of $10^{-5} \times 16$ MHz = 160 Hz. This is a theoretical limit that doesn't take into account errors due to a circuit implementation of the filter.

The two-path PWM technique

To overcome the intrinsic limitation and enable PWM-based high resolution conversion, others have suggested dithering and PWM stochastic modulation,[5] but neither are readily implemented on a standard MCU. Another method entails using a sample-and-hold circuit, which adds to analog complexity and errors.[6]

A two-path PWM technique is quite simple and can produce excellent results.[7] Figure 6 illustrates a simplified concept of this technique. Two PWM outputs: PWMH represents the N most-significant bits, while PWML represents the N least-significant bits. Scaling resistors (R_H and R_L) attenuates the least-significant PWM to generate an output in tiny steps. R_H and R_L form a potential divider, and the superposition method can be used to calculate the actual output.

Figure 6. Simplified schematic for the two-path PWM technique



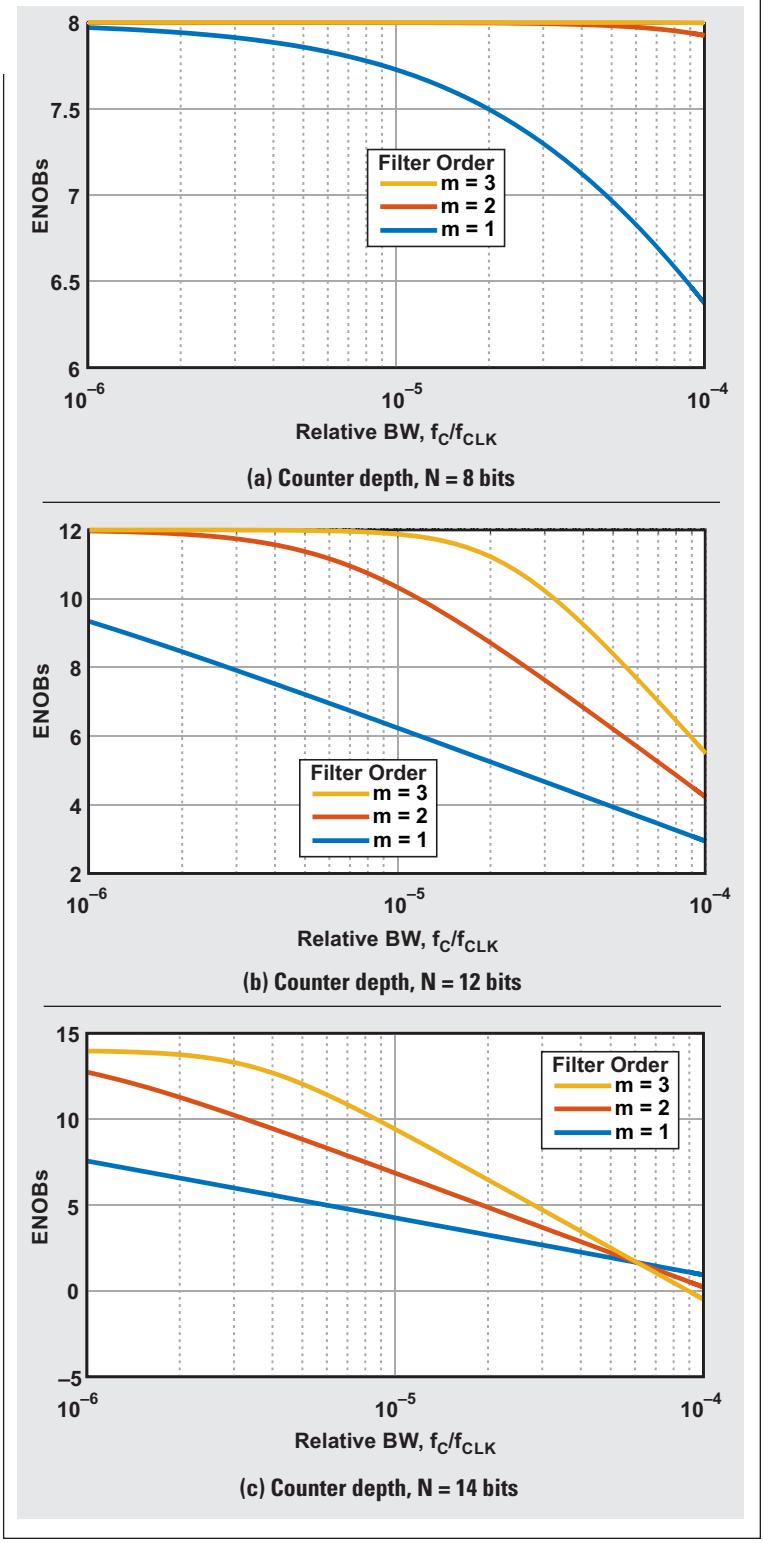
In the frequency domain, the output of each PWM input is treated separately. Equations 15 and 16 express the DC components of both the high and low signals, respectively.

$$A_{H0} = D_H \times \left(\frac{2^{N_L} - 1}{2^{N_L}} \right) \times V_P \quad (15)$$

$$A_{L0} = D_L \quad \frac{V_P}{2^{N_L}} \quad (16)$$

where the H and L subscripts refer to PWMH and PWML, respectively. Assuming that both PWMH and PWML run at the same frequency, have the same peak-to-peak magnitude, and have the same resolution

Figure 5. ENOBs vs. relative bandwidth for different N and m values



where $N = N_L = N_H$, the output can be defined by summing Equations 15 and 16, as in Equation 17.

$$OUT = A_{H0} + A_{L0} = \left(D_H \times \frac{2^{N_L} - 1}{2^{N_L}} + D_L \times \frac{1}{2^{N_L}} \right) \times V_P \quad (17)$$

Equation 18 calculates total uncertainty in the same way.

$$TU_{normalized} = \frac{1}{2^{2N}} + \frac{1}{\pi} \left(2^N \times BW \right)^m \quad (18)$$

The magic of the two-path technique becomes more obvious when looking at the equivalent ENOB versus relative bandwidth diagram in Figure 7. Achieving 16 bits of resolution over almost 1 kHz of bandwidth (assuming a 16-MHz clock) is possible just by using a second 8-bit PWM output and two precision resistors.

Active ripple suppression

Although the two-path PWM technique helps achieve higher resolution, the worst-case ripple still relates to the most significant bits. Active ripple suppression is a technique used in PWM audio converters to reduce ripple levels. The idea is to get an inverted PWM signal band-pass filtered to eliminate the DC. Summing this inverted signal to the main signal suppresses the undesired high-order harmonics. Figure 8 shows this concept illustrated on one path, with a first-order filter.

The effect of active ripple suppression can be explained in the frequency domain as summing the Fourier series components (as in Figure 3) to equivalent ones, but with a 180-degree phase shift. Simulation results show –20 dB of ripple suppression, which is equivalent to an extra pole for the filter.

Buffering the PWM signals

Because the peak-to-peak PWM signal value directly appears in the resolution (Equation 4), it is highly desirable to get this value as stable as possible. This value is a combination of the supply-voltage accuracy and the driver's voltage-high and voltage-low accuracy. The accuracy and stability of these parameters are poor for MCU general-purpose inputs/outputs.

A simple solution is to buffer the MCU PWM output with low-power high-speed logic gates, which would also be required to invert signals required by active ripple suppression. Powering logic gates with a stable voltage reference instead of a typical power device leads to very accurate and stable signal generation.

Figure 7. ENOBs vs. relative bandwidth for different m values using the two-path PWM technique

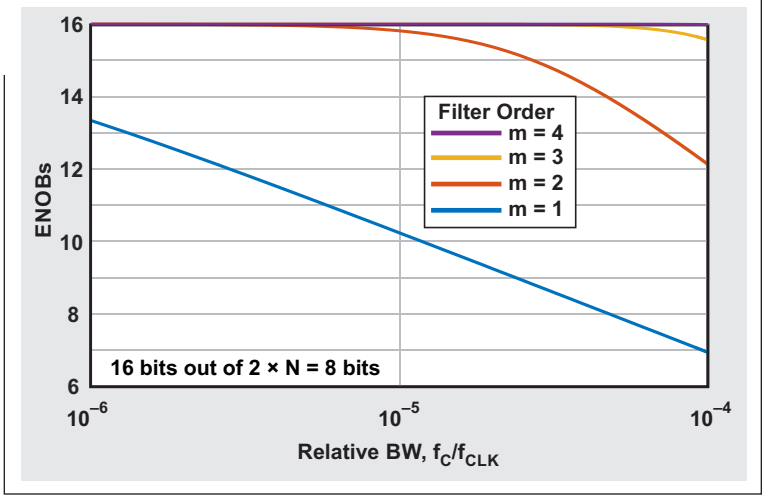
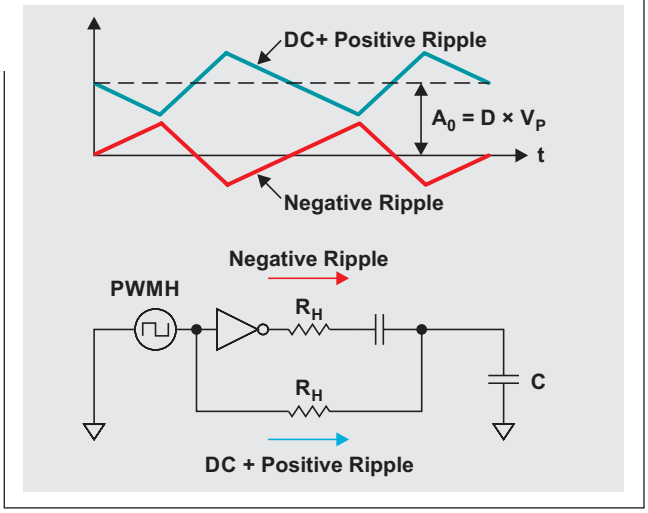


Figure 8. The active ripple suppression concept



Circuit schematic

The circuit in Figure 9 shows an example of the concepts described thus far: two-path PWM signals, buffered with a voltage reference as the supply, with ripple suppression through inverted signals. The ripple suppression stage with a first-order resistor-capacitor (RC) filter provides –40 dB/decade suppression of PWM ripples. A second-order active Sallen-Key filter follows to add another two poles, so the overall effective filter is a fourth-order filter. The low-drift, 3-V REF3330 voltage reference powers the active components.

A 4- to 20-mA current converter uses the filter output (V_2) as an input, creating a loop current expressed by Equation 19.

$$I_{Loop} = \frac{R12}{R20}\ \frac{V_2}{R3} = 8\ \ V_2\,mA \qquad (19)$$

As V_2 ranges from 0 V to 3 V, the loop current range is 0 mA to 24 mA. For details about the loop transmitter and its calculations, see Reference 8.

The transmitter is powered by the TPS7A16-Q1 high-voltage low-dropout regulator (LDO), which has an input range of 3 V to 60 V. The LDO generates 4.5 V of intermediate voltage to power the REF3330.

Protection

For loop protection, placing the TVS3300 33-V, bidirectional transient-voltage suppression diode (D1) at the loop input protects against surges, while Schottky diodes D2 and D3 protect against input reversal miswiring, which might damage the high-voltage LDO. In the event of a high capacitive load on power devices, the high in-rush current will pass to the local ground down to sense resistor R20, which might exceed the power limit of that resistor. Adding a current limiter in front of the LDO will mitigate in-rush current. For more details about the design of the current limiter, see Reference 9.

Low-power techniques

Achieving low power—specifically 100 µA for the whole converter—was a target for the circuit, but required several design techniques. The first was to use low-quiescent-current devices, including the LDO, the voltage reference and the logic buffer, as well as the operational amplifier (in this case, the OPA2333). Using R_H = 3.9 kΩ, plus a higher 20 kΩ for the first-order RC filter, is a good practice because resistance values—specifically R_H—play an important role in buffer dynamic power. The remaining power is consumed in R3, then R12, then Q1 of the current converter. For maximum output, letting R3 = 100 kΩ draws 25 µA, while the base of Q1 draws 20 mA/β(Q1) in the worst case. For a typical bipolar junction transistor (BJT) where β = 100, the base current would reach 200 µA, necessitating a much higher gain for the BJT. A transistor pair where $\beta = 10^4$ reduces the maximum current in the Q1 base to 2 µA.

Figure 9. High-resolution two-path PWM to 4- to 20-mA converter

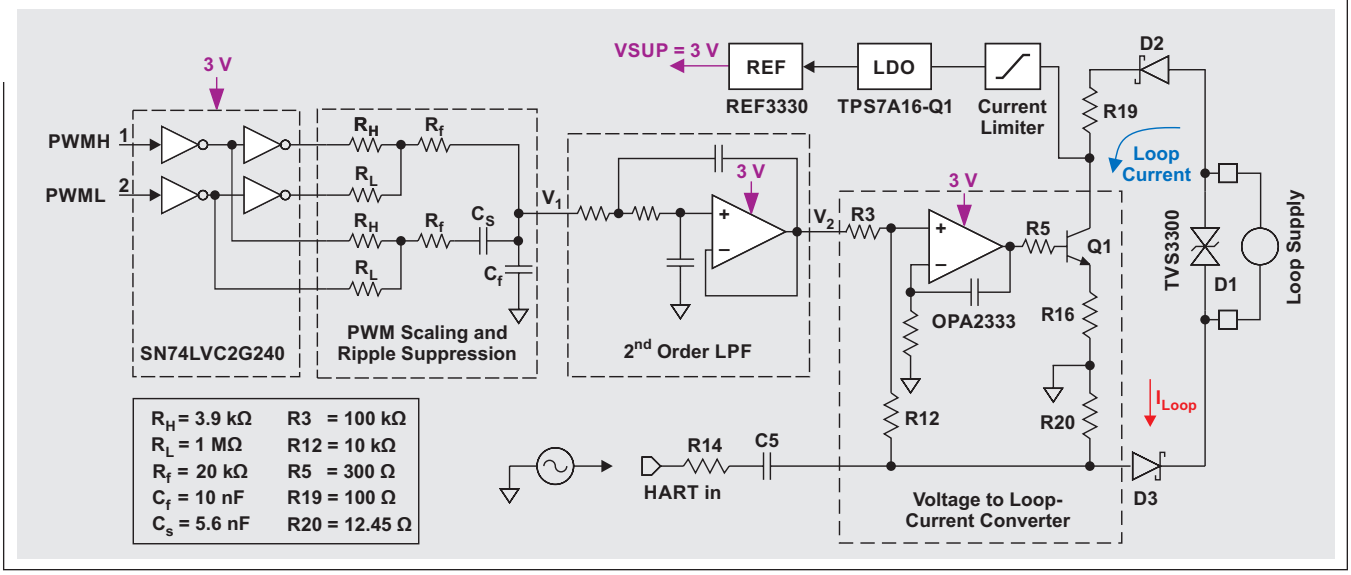


Figure 10 is the printed circuit board (PCB) layout of the circuit shown in Figure 9. The PWM-to-voltage area is 15 mm by 7 mm. Protection devices are 8 mm by 5 mm, while the power stage is 13 mm by 3 mm. Although the circuit footprint is actually minimal, it is possible to reduce it further by using smaller packages of most devices.

Test setup

Figure 11 shows the setup in which the circuit board was tested. An analog waveform generator (AWG) with floating ground generates the two PWM signals. The power supply is providing loop power. The loop current is measured with a 6.5-digit resolution multimeter over one power cycle. A precision burden resistor (R_{Burden}) converts the current to voltage, while a 24-bit ADC captures current noise not otherwise captured by the multimeter due to averaging. A differential scope probe placed at the J15 PCB node (V_2 in Figure 9) measures the settling time.

Test results

Table 1 lists the circuit test results. See Reference 10 for more details about results and measurement graphs.

Conclusion

An exploration of the limitation of the classical PWM DAC technique through mathematical analysis has shown that a PWM to 4- 20-mA converter design that uses a voltage reference and active ripple suppression can lower noise to almost 0.1% FS. Using a scaled two-path technique achieves a resolution of 16 bits over a 600-Hz bandwidth. Low-power amplifiers, low-quiescent-current regulators and an output-transistor pair bring power to a maximum of 102 µA over temperature. The amplifiers also feature very low temperature drift, which resuls in low offset errors and stable performance over the whole industrial temperature range.

References

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Figure 10. PWM to 4- to 20-mA circuit PCB

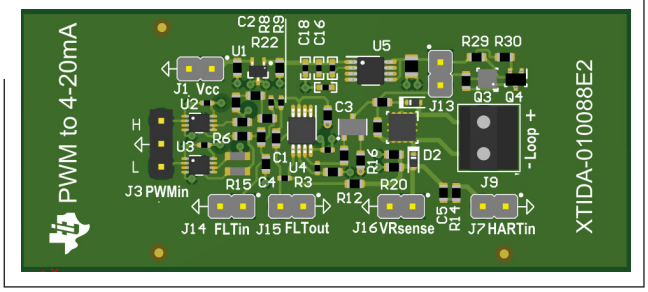

Figure 11. Circuit test setup

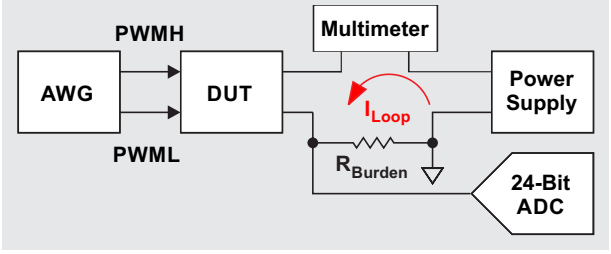

Table 1. Measured performance of the test setup

Parameter	Value
Loop supply voltage	9.5 V to 32 V
Loop current range	40 µA to 24.075 mA
Resolution	16 bits
Current consumption	102 µA maximum
Temperature range	–40° to +125°C
Bandwidth	600 Hz
Settling time	3 ms for 4- to 20-mA steps
Offset error	–6.66 µA to 5.02 µA
Offset error tempo	5.84 ppmFS/°C maximum
Gain error	–0.18 to 0.08% full scale
HART input gain	1.1 mA/V at 1.2 kHz, 1 Vpp
	1.3 mA/V at 2.2 kHz, 1 Vpp

8. "Highly Accurate, Loop-Powered, 4-mA to 20-mA Field Transmitter with HART Modem Reference Design," TI Designs (TIDA-01504), December 2017.
9. "Isolated, Ultra-Low Power Design for 4- to 20-mA Loop-Powered Transmitters Reference Design," TI Designs (TIDU414), September 2014.
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Related Web sites

Product information:

SN74LVC2G240, REF3330, TPS7A16-Q1, TVS3300, OPA2333

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