Design considerations for AC adapters with USB Type-C® and USB PD ports

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Introduction

Despite nearly ubiquitous wireless connectivity options, consumers are still tethered to a wire that delivers energy from an AC charging adapter to the batteries of wireless devices. The connectors between the adapter and the device are often not identical, however, and the power that a laptop needs, for example, is higher than the power that a fitness tracker needs. That's why most devices come with their own adapter.

USB Power Delivery (PD) simplifies this conundrum. USB PD is an emerging standard for charging and transferring data included in devices like laptops, smartphones and tablets; USB PD is the standard that supports the power delivery requirements. Shipments of USB PD ports are expected to increase from 94 million in 2018 to 4.7 billion in 2023, with growth driven by original equipment manufacturers like Google, who mandated that future smartphones be compatible with USB Type-C® ports.

USB PD supports a single adapter for many devices through a feature that negotiates with the attached device to learn its required charging voltage. The normative voltages in USB PD are 5 V, 9 V, 15 V and 20 V. A cellphone needs 5 V, whereas a laptop needs 20 V. This negotiating feature enables the adapter to adjust the voltage and power delivery for on-the-fly compatibility with everything from small devices that need milliwatts of power to large laptops that need 65 W of power. When used with USB PD devices, the USB Type-C (USB-C®) connector and cable support multiple devices requiring up to 100 W of power, as shown in Figure 1. As the adoption of new PD standards expand, consumers will have fewer adapters to keep up with and OEMs will be able to reduce the number of adapters in inventory.

In addition to the demand for higher power density, there's a need for low-power losses in no-load and standby modes. Power-loss limits vary according to the power-supply rating and the governing body. The European Code of Conduct (CoC) Tier 2 requires power consumption below 75 mW in adapters rated for 50 W and below. For adapters from 50 W to 250 W, the standard requires standby power below 150 mW. In the United States, the governing CoC is U.S. Department of Energy (DoE) Level VI. Most adapters must meet these standards and others in order to be considered viable in the global market.

Figure 1. USB PD covers a wide range of devices and power requirements

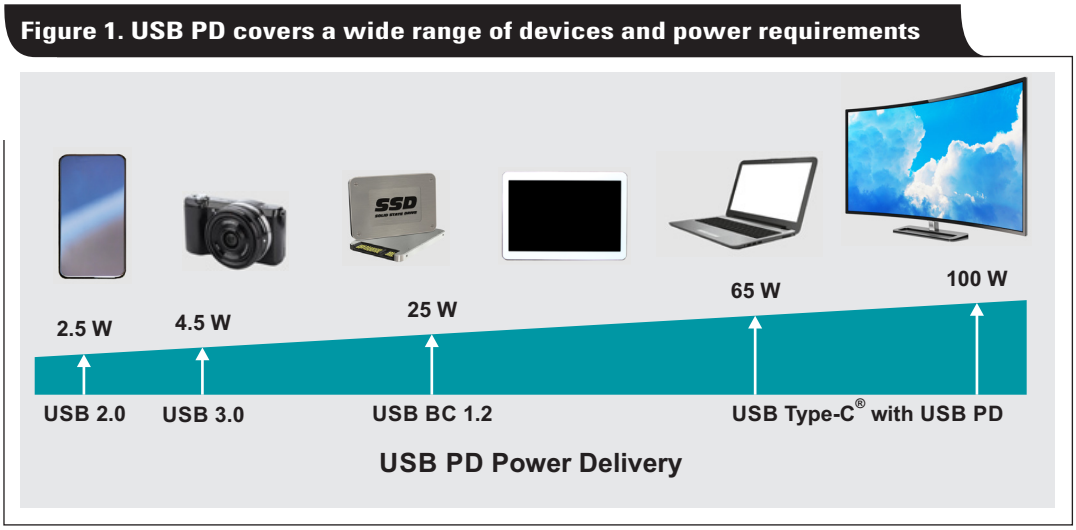
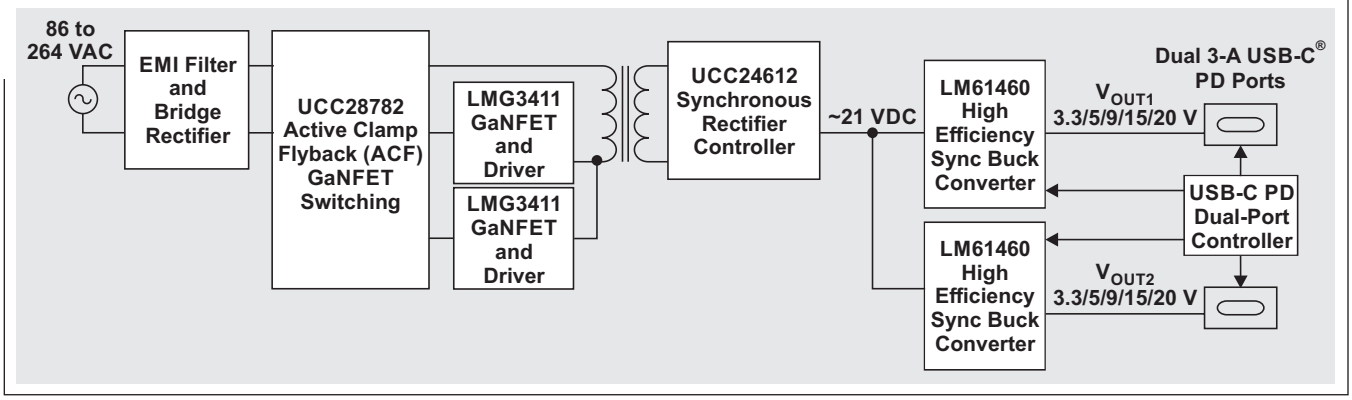


Figure 2. USB PD block diagram with an ACF and two independently controlled USB ports



This article describes the design considerations for a 65-W AC adapter with a dual-power USB PD configuration that enables independent control of the power delivery on each port, which improves the user experience. While there are many dual-port adapters, they often do not support independent control of the output power on each port, enabling simultaneous charging only when both devices require the same input voltage and effectively preventing users from charging two types of devices (like a phone and a laptop) at the same time. The design presented in this article optimizes power density and standby power consumption while enabling the connection of multiple device types to the adapter simultaneously.

Figure 2 is the block diagram for the dual USB-port design. There are two functional stages. The first stage is the AC/DC power-conversion stage with an active-clamp flyback (ACF). The second stage is the power delivery and control stage with high-efficiency DC/DC converters. The USB-C PD dual-port controller is responsible for managing the power negotiation for each port and controlling the output voltage of the DC/DC converters accordingly. The focus of this article is on the power conversion.

Design considerations for the AC/DC power-conversion stage

Power architectures for AC adapters traditionally use a quasi-resonant flyback (QRF) converter because of its high efficiency and smaller size compared to a hard switching flyback converter. However, the continued use of this architecture to support high-power, multioutput USB PD adapters will result in large and difficult-to-use adapter products. This limitation is because the higher power density through a higher switching frequency results in higher heat dissipation in the QRF from frequency-dependent losses. An ACF with gallium nitride (GaN) switching field-effect transistors (FETs) and a dual DC/DC converter architecture enables the smallest possible size while offering consumers the best possible multidevice charging experience.

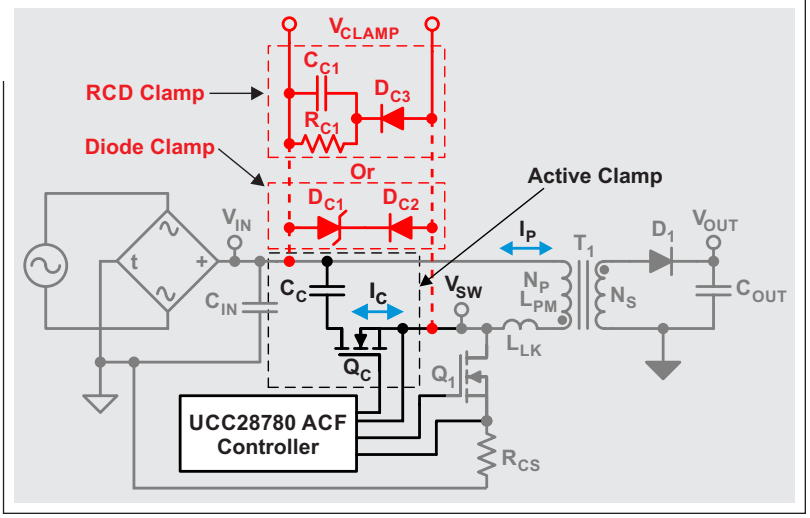
QRF size-reduction limitations

In power-supply design, the magnetic components are often the limiting factors when attempting to achieve smaller-size adapters and increase the power output capability. It is possible to reduce the size of magnetic components by increasing the switching frequency (f_{SW}). But an increased f_{SW} brings higher switching losses and more power dissipation and heat.

The discontinuous-conduction-mode QRF suffers from high power dissipation in the passive clamp circuits needed to protect the main switch (Q1) from electrical overstress (see Figure 3). QRF passive-clamp options are shown in red for resistor-capacitor-diode or diode clamps, which can provide a path to dissipate the energy stored in the leakage inductance (L_{LK}) of the transformer (T1). Energy is lost in these clamps during each switching cycle. The resulting power loss for the QRF is directly proportional to f_{SW}, as expressed by Equation 1.

$$P_{CLAMP} = \frac{V_{CLAMP}}{V_{CLAMP} - \frac{N_P}{N_S} \times V_{OUT}} \times \frac{1}{2} \times L_{LK} \times I_P^2 \times f_{SW} \quad (1)$$

Figure 3. QRF passive clamps compared to ACF active clamp



In addition to loss in the passive clamp, the QRF exhibits frequency-dependent losses at the switch node that are evident by examining Equation 2.

$$P_{SW(QRF)} = \frac{1}{2} \times C_{SW} \times \left(V_{IN} - \frac{N_P}{N_S} \times V_{OUT} \right)^2 \times f_{SW} \quad (2)$$

where C_{SW} is the capacitance at the switch node.

How an ACF virtually eliminates frequency-dependent power loss

The UCC2878x ACF controller family takes advantage of the bidirectional current flow in the active clamp of the flyback converter's Q_C and C_C in Figure 3. This bidirectional current flow is not possible in diode-based clamps, and energy dissipates through excess switch-node ringing. Figure 4 compares the switching waveforms of an ACF vs. a QRF. As evident from the red QRF waveforms of the switch-node voltage (V_{SW}) and primary current (I_P), the energy in the clamp and the nonzero switch node create losses that increase with increasing frequency. The ACF waveforms are shown in black.

Figure 4 shows that virtually no energy dissipates in the clamp portion of the switch cycle. The bidirectional clamp also enables the storage of energy from the leakage inductance in C_C for later transfer back to the V_{OUT} through the transformer turns ratio. True zero voltage switching occurs when the UCC28780 adjusts the on-time of Q_C to allow additional energy from C_C to discharge the switch-node capacitance to ground when Q_C turns off. This results in near zero volts across the drain to source of the primary-side switch Q1 and eliminates switching losses.

The ACF with the UCC28780 controller eliminates the frequency-dependent losses of the QRF and makes it possible to increase the f_{SW} and reduce the size of magnetic components without uncontrollable heat dissipation.

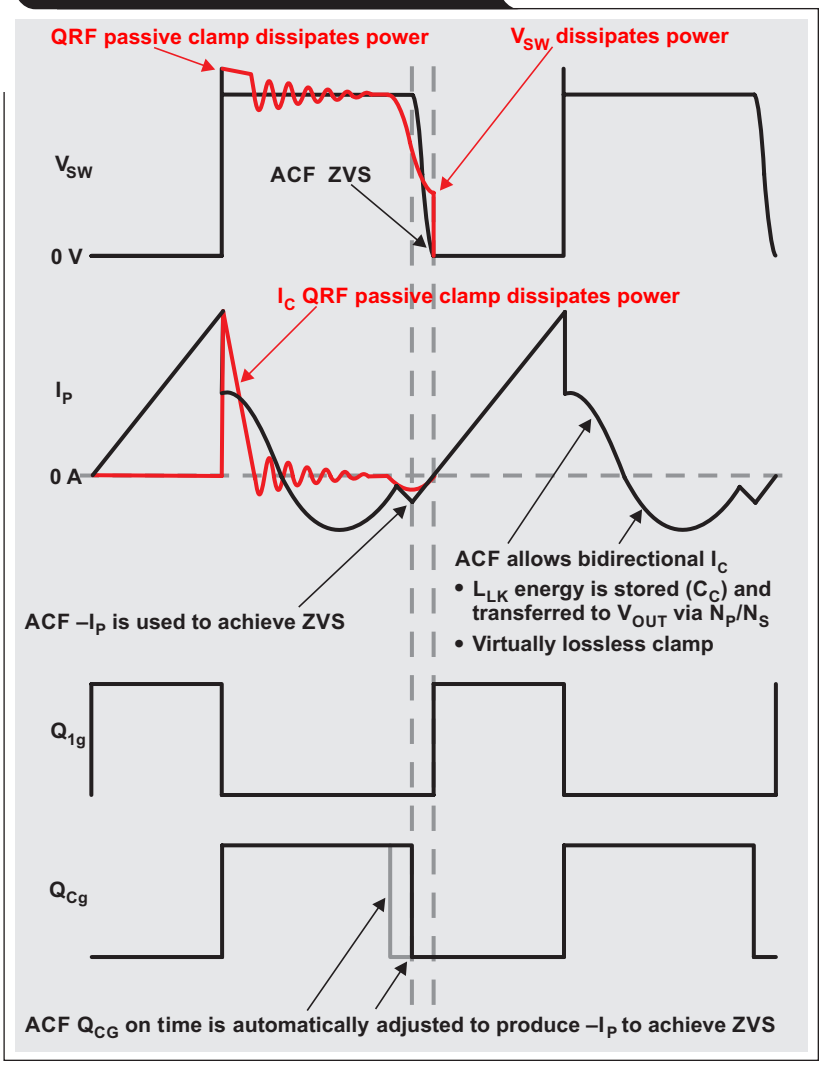
Optimizing design for size and power-loss reduction

The UCC78280 controller supports ACF designs using either silicon or GaN FETs. The magnitude of the GaN FET's circulating currents related to C_{OSS} is dramatically reduced compared to silicon FETs because of the significant reduction of C_{OSS} in GaN FET structures. This enables an ACF with a GaN FET to operate up to 1 MHz, enabling very small form factors, particularly when using GaN FETs. The LMG3411R150 is an example of a 600-V, 150-mΩ GaN FET with integrated driver and protection. GaN FETs offer the ability to reduce switching losses by as much as 80% compared to silicon metal-oxide semiconductor FETs (MOSFETs).

It is possible to eliminate further power losses and heat generation by replacing the secondary-side rectification diode with a MOSFET switch. Synchronous rectification on the secondary side offers near-perfect diode performance compared to the high power losses across V_D of the real diode. Design considerations for the synchronous rectifier controller include fast switching times, high frequency operation and a high-enough gate-drive voltage to fully enhance the MOSFET switch. The UCC24612 high-frequency synchronous rectifier controller is designed to work in high-frequency applications like the ACF. It supports operation up to 1 MHz and is tolerant of high voltages, making it a good fit for output voltages over 20 V. It uses intelligent V_{DS} sensing control and a proportional gate drive to operate the synchronous FET as an ideal diode.

The combination of ACF with a GaN FET and secondary-side synchronous rectification can easily achieve power density for a 65-W AC adapter greater than 30 W/in^3.

Figure 4. Comparing the switching waveforms of an ACF vs. a QRF



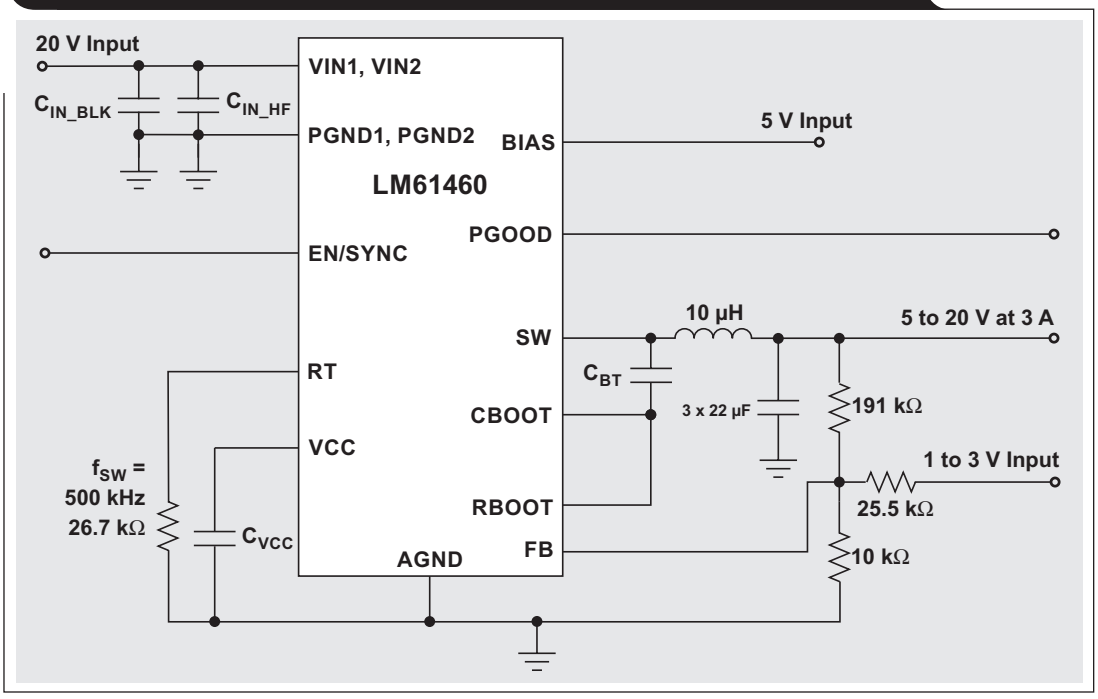
In addition, this approach can deliver efficiency greater than 94% and no-load power consumption of 60 mW. These figures are more than adequate to meet even the toughest CoC standards for standby power consumption.

Design considerations for power delivery and the control stage

There are many ways to approach the power delivery and control for single- and dual-port adapters. A dual-port adapter is designed to control power delivery to multiple devices simultaneously; for example, a notebook PC that needs 20 V to charge its battery and a cellphone that needs 5 V. Additionally, the power requirements of each device are different. It is important to balance the need for small size and low power consumption as well, without making design trade-offs that result in suboptimal performance.

One approach that balances the user's ability to charge two types of devices simultaneously with performance is the use of dual DC/DC converters between the output of the ACF AC/DC stage and the USB Type-C port. Each DC/DC converter can be independently controlled to deliver the output voltage that corresponds to the normative voltage point for the device being charged. One can be set to 20 V, while the other can be set to 5 V. The USB PD controller has the ability to detect the power requirements of the device and set the output voltage accordingly. This is easily done by connecting a 25.5-kΩ resistor between the USB PD control pin and the feedback network on the DC/DC controller, as shown in Figure 5. By varying the voltage on this pin, the output can be scaled from 3.3 V to 20 V with 20-mV resolution, as required by the USB PD Programmable Power Supply specification.

Figure 5. LM61460 36-V, 6-A DC/DC converter configuration for USB PD



DC/DC converter design considerations

A number of important system-level requirements will drive DC/DC converter selection. The device must be able to operate without subharmonic oscillations at a very high duty cycle to achieve a 20-V input to a 19.3-V output. The device must have extremely high efficiency. DC/DC converters like the LM61460 in can achieve 99% efficiency and stable operation with inductor values as low as 4.7 µH.

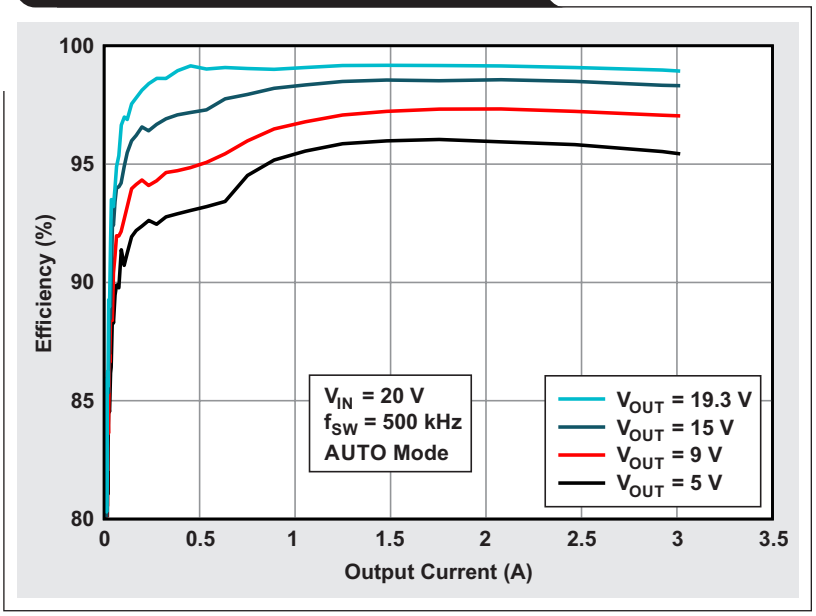
Figure 6 shows the efficiency curves for the LM61460 with a 20-V input and each of the normative USB PD output voltages.

Designing for stable operation in low dropout conditions with low inductor values requires special attention to the design of the internal slope compensation on the current-mode DC/DC converter. If the slope compensation isn't adequate, then the DC/DC converter will exhibit subharmonic oscillations when operating at a high duty cycle. The LM61460 slope compensation circuit was designed for unconditional stability in low dropout situations, such as those found in USB-C and automotive applications.

Low dropout operation is also not possible at high frequencies if the minimum off-time of the DC/DC converter is too large. The LM61460's minimum off-time of 65 ns enables stable operation at high frequencies under low dropout conditions.

Finally, even though the efficiency is high, there are still thermal challenges when packaging an adapter with power density greater than 30 W/in^3. Having the highest possible operating junction temperature will provide additional thermal design headroom. The DC/DC converter should have an operating junction temperature of 150°C, which the LM61460 has.

Figure 6. LM61460 efficiency curves for USB PD normative voltages



Conclusion

Achieving higher power density is a challenge when designing USB-C adapters. Many factors limit the possible size reductions in traditional QRF approaches. Implementing a power stage with an ACF and a GaN FET with secondary-side synchronous rectification can overcome significant barriers to high-density AC/DC designs. Further optimization is possible through independently-controlled DC/DC converters for each USB-C port.

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Related Web sites

Product information:

LM61460

UCC28780

LMG3411R150

UCC24612

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