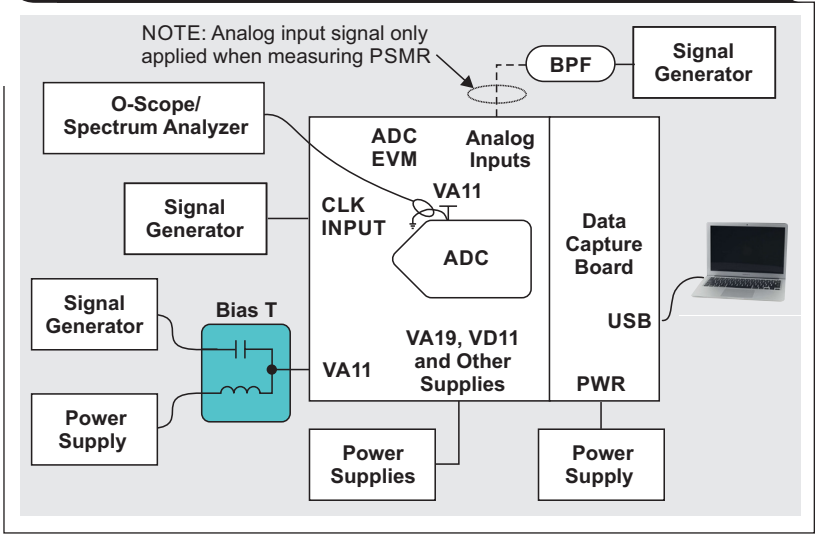
Clutter-free power supplies for RF converters in radar applications (Part 2)

By Rob Reeder, *Applications Engineer, High-Speed Data Converters*
Neeraj Gill, *Applications Engineer, High-Speed Data Converters*

Introduction

The Part-1 installment[1] of this series described how noise couples into an analog-to-digital converter's (ADC) supply, how it might couple through the ADC's circuitry and some common power-supply trade-offs. That knowledge will now be applied by measuring the ADC12DJ5200RF ADC's rejection to noise and spurs, known as the power-supply rejection ratio (PSRR) or power-supply modulation ratio (PSMR). An example is provided that shows how much noise can be presented to the ADC's supply pins to assist in properly narrowing down the selection of suitable power-management devices for your next signal-chain design. Some practical design guidelines are also included.

Figure 1. Bench test setup for PSRR or PSMR measurement



Measuring PSRR or PSMR

Figure 1 shows a measurement setup for testing PSRR or PSMR supply nodes individually using a bias T. Available off the shelf, a bias T combines the AC and DC signals to the individual supply under test. The bias T must have a high-enough current rating to supply enough bias; otherwise, the measurement could produce unreliable results.

To measure the PSRR:

1. Set up the evaluation module or system board as you normally would, then isolate the supply under test. This may require the removal of the decoupling capacitors for that specific power domain.
2. Apply the bias T to that supply domain, setting the appropriate DC voltage using a clean external bench power supply.
3. Use a digital multimeter to confirm that the test point for the supply under test is as close to the ADC as possible (next to the power pin, for example) to ensure the application of the appropriate DC voltage at the nominal data-sheet value. The bench supply might require a slight adjustment to compensate for the bias-T and cable losses.
4. Apply power to the rest of the ADC and board's supplies, keeping those supplies at nominal values. Select an appropriate frequency within the first Nyquist zone—in this case, 10 MHz was used to start—and inject the sine-wave signal source to the bias T. This is called the error signal.
5. Start the signal low in amplitude, slowly bringing the amplitude up until a spur comes out of the noise floor, using TI's high-speed data converter pro software (HSDC-Pro)[2] to display and measure the digital output fast Fourier transform (FFT) spectrum. The error spur should be high enough in the FFT spectrum where it is repeatable and becomes evident at the error test frequency injected, 10 MHz. In this case, the error spur amplitude captured was –78 dB. Figure 2 on the next page illustrates an example of the injected error signal coming out of the output spectrum.
6. Use an oscilloscope or spectrum analyzer to note the level of error signal injected. Again, take this measurement as close to the ADC's supply node under test, preferably the ADC's power pin.

   Note the voltage peak-to-peak (V_{PP}) signal injected at that pin. Once you know this, you can calculate the PSRR using some simple math. For example, if the measured error signal applied were 8 mV_{PP} and the ADC's full-scale voltage is 0.8 V_{PP}, simply take the ratio of those two numbers or 20 × log(8 mV/800 mV) = –40 dB. To find the PSRR, subtract this number from the error spur amplitude found previously in the FFT spectrum or PSRR: –78 dB – (–40 dB) = –38 dB.
7. Measure various error signal injection levels and frequencies at least across the first Nyquist zone of the ADC.
8. Repeat these same steps for the rest of the ADC's power supply nodes.

Figure 2. ADC output FFT spectrum with error signal applied

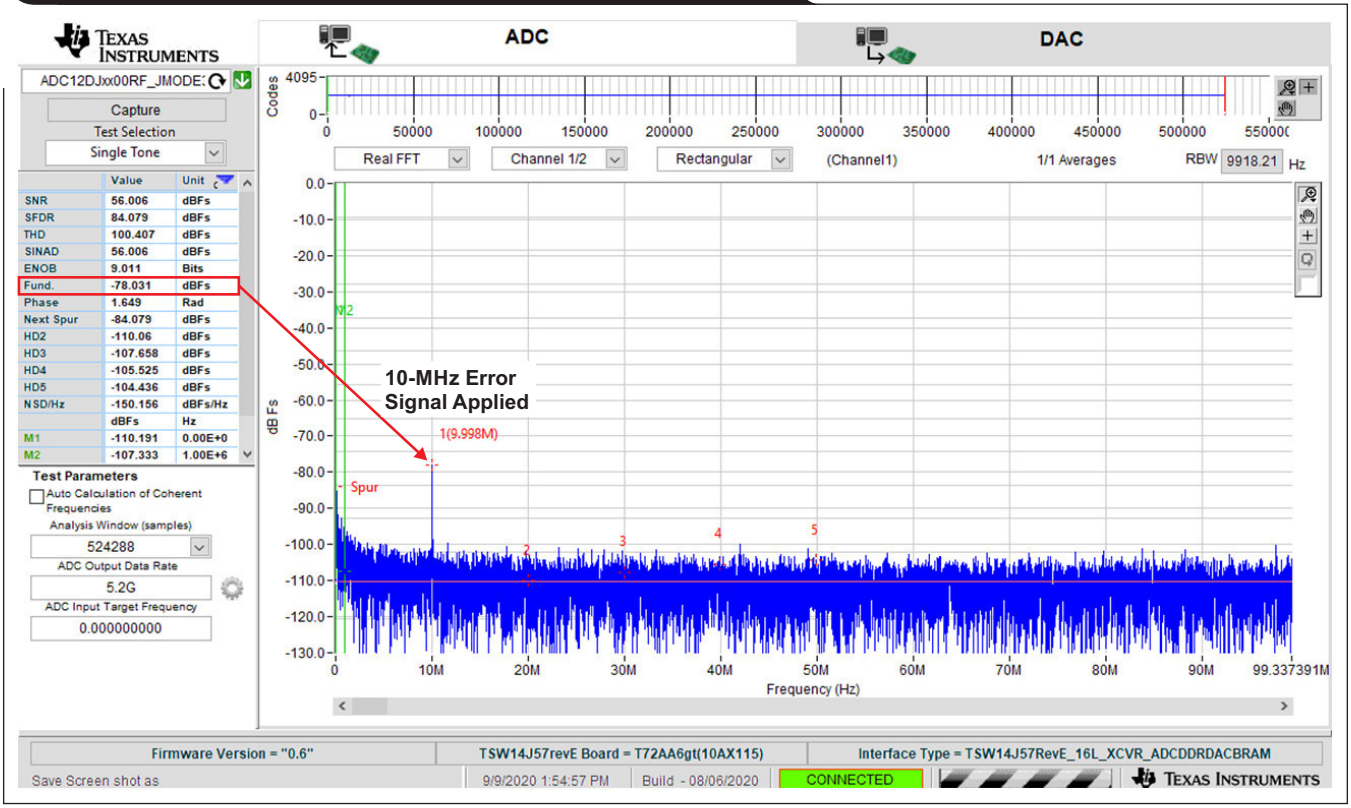


Figure 3 highlights the PSRR measurement results of the ADC12DJ5200RF. The VA11 and VA19 plots shows that ADC analog supplies can be less robust and more prone to power-supply noise than the digital supplies (VD11) because of the different internal ADC circuit topologies, as mentioned in the Part 1 article. Also, the PSRR generally degrades in performance the higher the frequency applied is closer to Nyquist or $f_S/2$. This offers insight into the power-supply circuit design for the ADC, underscoring how important it is to understand the noise distribution of the low-dropout regulator (LDO) or switcher. In many cases, the noise distribution is considered white or flat across frequency, but that should be confirmed.

The PSMR is the ratio of power-supply noise injected at the ADC's power-supply pin and the amplitude of modulation product appearing around the signal applied to the ADC analog input. The technique to measure PSMR is similar to PSRR, except that PSMR is measured as a coupling of the supply noise or spur and the additional RF

Figure 3. ADC12DJ5200RF PSRR vs. each supply domain

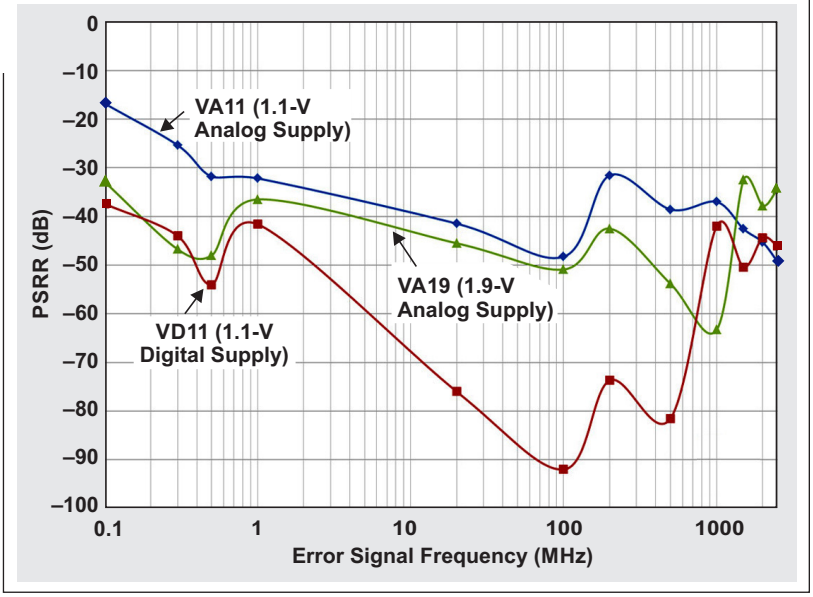
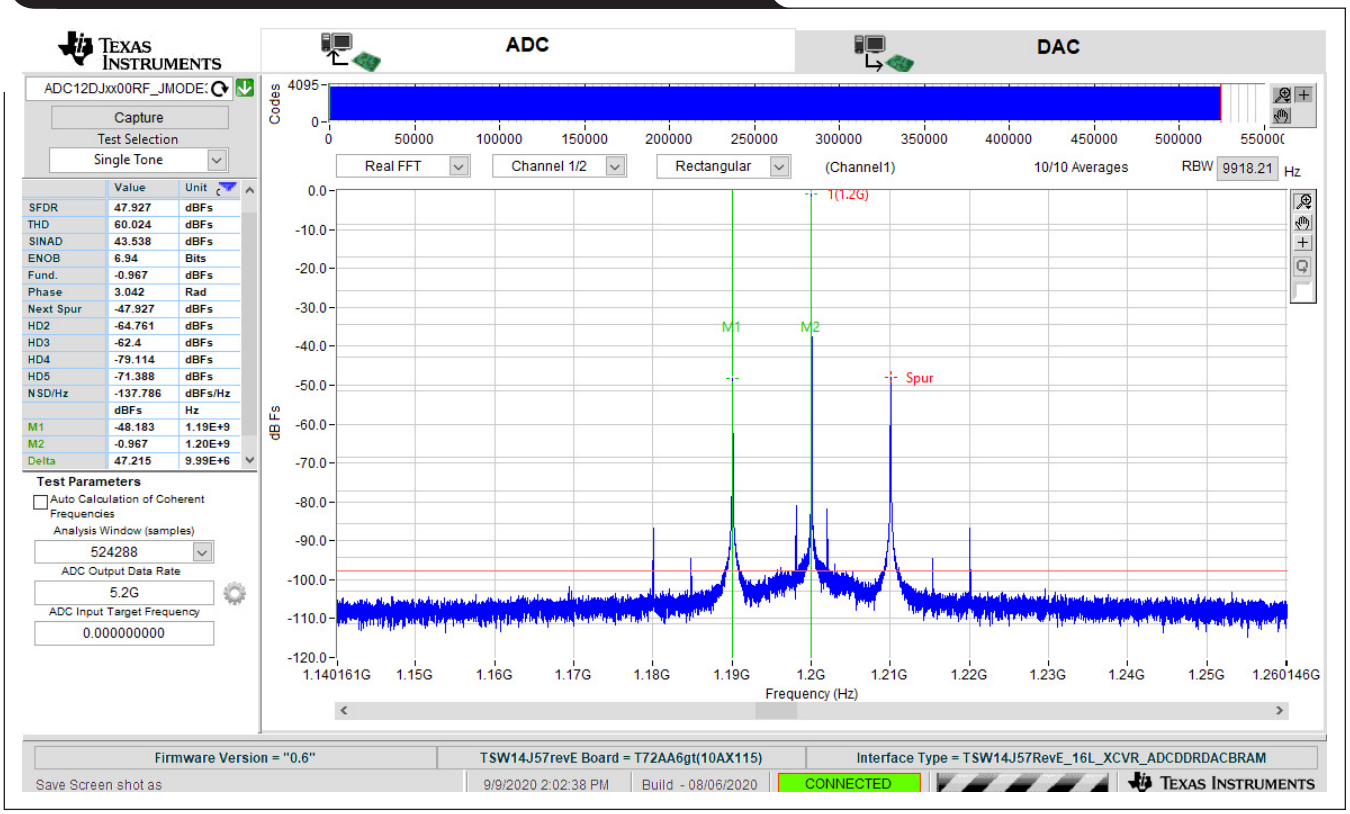


Figure 4. PSMR example with forced error signal applied



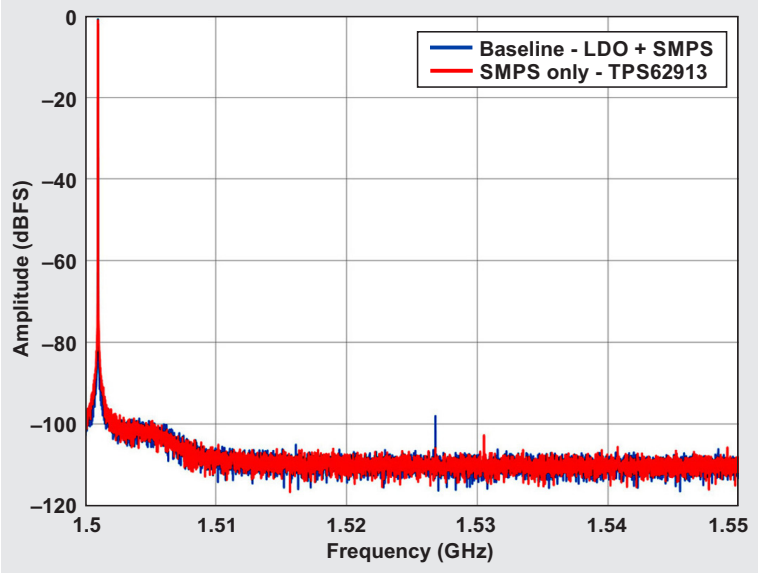
input signal applied to the ADC. As shown in Figure 4, using the principle of modulation, applying a 10-MHz error signal on the power-supply pin will modulate on to the RF input signal and create modulation products around the RF input frequency plus or minus the error signal frequency ($f_{IN} + f_{Error}$), or 1.2 GHz ±10 MHz.

To find the PSMR, the amplitude as shown in Figure 4 of $f_{IN} - f_{Error}$ (1.2 GHz – 10 MHz) is –48.13 dBFS. If the error signal (f_{Error}) applied to the power-supply pin is approximately 100 mV_{PP} and the ADC's full-scale voltage is 0.8 V_{PP}, simply take the ratio of those two numbers, or $20 \times \log(100\ mV/800\ mV) = -18$ dB, then subtract this number from the modulation amplitude found in the FFT spectrum or PSMR: –48 dB – (–18 dB) = –30 dB.

The main difference between LDOs and DC/DC converters is the switching mechanism required for voltage conversion. DC/DC converters are considered noisier because they create harmonics and ripple. In noise-sensitive applications, LDOs are often recommended for sensitive power supplies, but with advancements in power integrated circuit (IC) designs, new DC/DC converters can closely approach LDO noise performance.

Figure 5 compares an LDO-based power-supply design (LDO + switched-mode power supply [SMPS]) to a DC/DC converter-based power supply (SMPS only). The two plots illustrate the application of a 1.5-GHz analog input frequency to the ADC12DJ5200RF ADC, using averaged FFT data to compare the performance differences. There is no visible power-supply modulated signal next to the fundamental frequency (1.502 GHz) with the LDO versus the SMPS (TPS62913) design.

Figure 5. PSMR comparison around a 1.502-GHz input signal



Because DC/DC converters generally switch at a frequency from around 20 kHz to 2 MHz, the switching spur can also appear at a switch frequency near DC (0 Hz) in the FFT output spectrum.

Figure 6 shows a zoomed-in section of the spectrum near DC and compares DC/DC converter performance to an LDO-based power-supply design. There are no visible spurs that degrade ADC performance.

The spurious-free dynamic range (SFDR) is an important parameter when looking at ADC performance. Other than the fundamental frequency, SFDR is the highest spur present in the ADC's frequency spectrum. The highest spur is typically harmonically related, but could also be defined by a switching spur. In either case, spurs caused by power supplies or other coupled noise can degrade an ADC's SFDR performance.

Figure 7 compares the SFDR performance over several frequency points from near-DC to near 10 GHz. The SFDR performance of the SMPS (DC/DC converter) design is comparable with the SFDR performance of the LDO + SMPS design.

Figure 6. PSMR comparison at DC

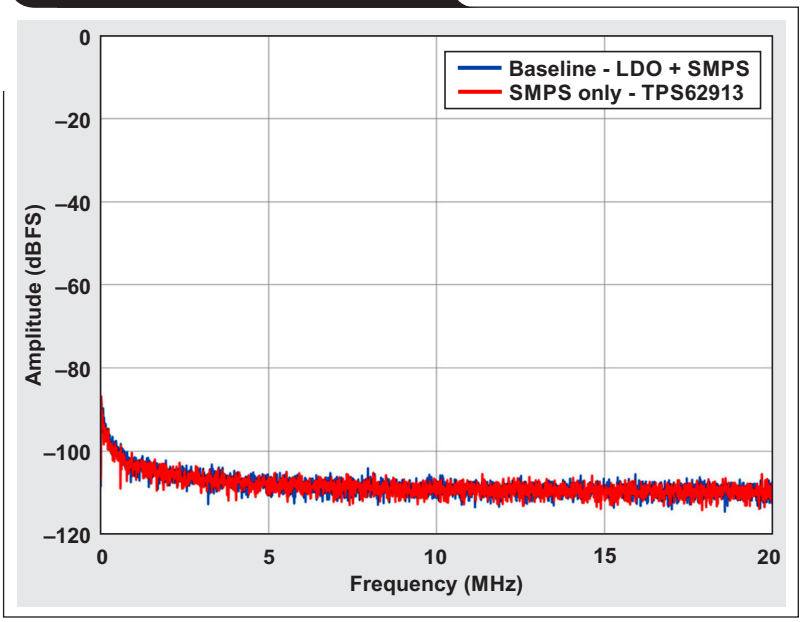
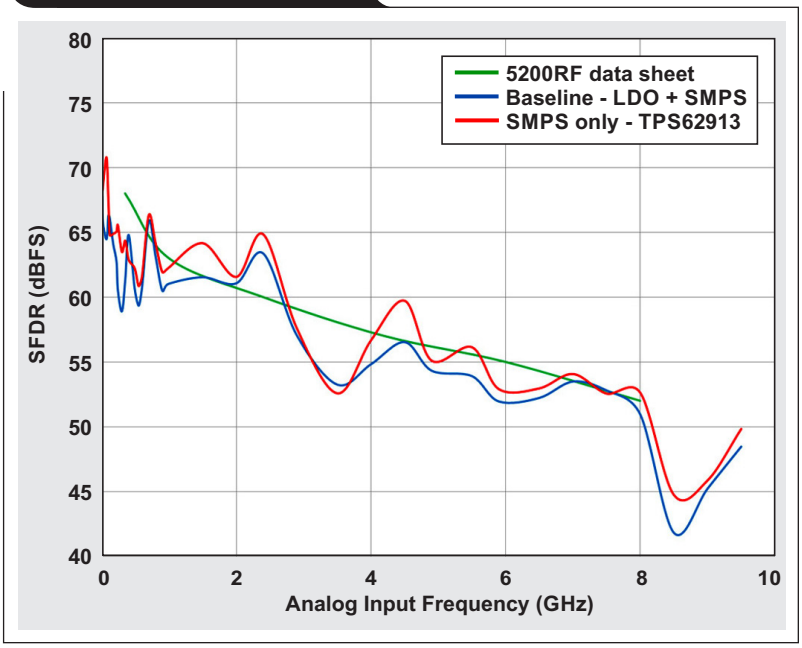


Figure 7. SFDR comparison



It would be prudent to compare the signal-to-noise ratio (SNR) of the two designs. Power-supply noise can manifest itself as an unwanted modulated signal around the fundamental, or it can appear near DC and affect the SNR performance of the ADC. Figure 8 compares the SNR performance between the two power-supply designs. Once again, the SMPS (DC/DC converter) design is on par with the SNR performance of the LDO + SMPS design.

For more details about this comparison, see the application report that is linked in Reference 3, "Powering Sensitive ADC Designs with the TPS62913 Low-Ripple and Low-Noise Buck Converter."

Tying it all together

Given the effect that PSRR and PSMR measurement can have on ADC performance, the following example shows how to choose an LDO or SMPS for your next power-supply design.

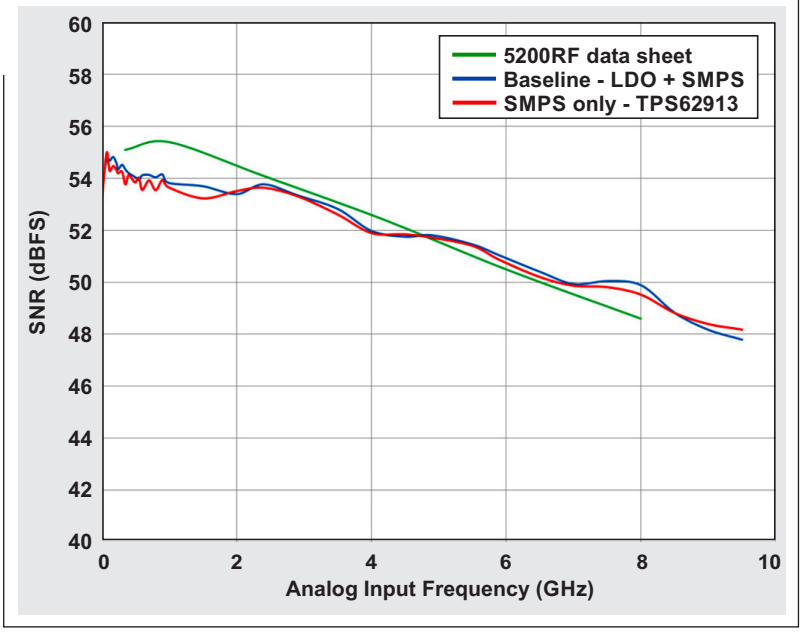
Using the TPS62913 buck converter as an example, the data sheet shows that when properly with LC filtering, the switcher circuit will have a combined integrated noise and output voltage ripple of 18.3 μV_{RMS} over a 100-kHz bandwidth. Assuming that the noise is Gaussian, the noise density is 57.8 $nV_{RMS}/\sqrt{Hz}$.

Typical PSRR ranges from –40 to –60 dB on the analog supply of a high-speed ADC. Using the ADC12DJ5200RF as shown in Figure 3, the supply has a PSRR of –40 dB (10 mV/V) for VA11 on average across Nyquist or $f_S/2$. The noise floor of the ADC can either be measured or calculated using Equation 1. The ADC12DJ5200RF is a 12-bit, 5.2-GSPS (f_S) ADC that has an 0.8-V_{PP} differential-input full-scale range (FSR) and an SNR of approximately 54 dB when sampling in first Nyquist, taken from Figure 8.

$$\text{ADC noise floor} = \frac{\text{FSR} / \left(2/\sqrt{2}\right)}{\frac{10^{\text{SNR}/20}}{\sqrt{f_S/2}}} = 11.07 \text{ nV}_{RMS} \quad (1)$$

The SMPS's noise floor is almost five times higher (or 57.8 nV/11.1 nV) compared to the noise floor of the ADC. The attenuation of the ADC's PSRR that the SMPS regulator will see when its noise enters the ADC's power pin (which is –40 dB) translates to a convolved regulator noise of 578 $pV/\sqrt{Hz}$, or 57.8 $nV/\sqrt{Hz}$ × 10 mV/V. Note that –40 dB is much lower than the ADC's noise floor and will not appear in the ADC's output spectrum, nor will it degrade the ADC's AC performance.

Figure 8. SNR comparison



General power-supply design summary and guidelines

High-speed, precision and RF ICs and circuits are sensitive to noise and spurious contents that result from high current in switching elements, output capacitor equivalent series resistance and the magnetics involved when using standard DC/DC converter designs.

The ADC's analog and clock inputs (and circuits) get the most scrutiny when it comes to addressing low noise on their inputs. But power supplies are also inputs. Just because they may be thought of as DC biasing circuits doesn't mean that they can't degrade RF performance.

By understanding how to apply PSRR and PSMR numbers in the analysis of a power-supply design, it is much easier to choose which regulator technologies and types to use. If the PSRR numbers for the ADC cannot be found, you can request this information in TI's E2E™ technical support questions or use the guidelines outlined in this article to measure PSRR.

When designing power-supply domains for any high-speed or precision ADC, or RF or noise-sensitive IC, here are a few tips for fortifying your next design against power-supply noise:

- Decouple all power-supply rails and bus voltages as they come onto the system board and near or at the ADC itself.
- Remember that each additional filtering stage adds approximately 20-dB per decade of noise suppression.
- Decouple for both high and low frequencies, which might require multiple capacitor values.
- Use series ferrite beads at the power entry point, just before the decoupling capacitor to ground, and for each individual supply voltage coming in or onto the system board, whether it comes from an LDO or SMPS .
- For added capacitance, use tightly stacked power and ground plane pairs (≤4-mil spacing). This adds inherent high-frequency (>500 MHz) decoupling to the printed circuit board design, and it's free.
- Practice good layout partitioning. Keep noisy supplies away from sensitive analog circuitry such as the front-end stage of the ADC and clocking circuits.
- Locate some components (high-current magnetics) on the opposite side of the PCB for added isolation.
- Follow the IC manufacturer recommendations; if they are not directly stated in the application note or data sheet, study the evaluation board, which is a great vehicle to learn from.

Following this advice can help provide a solid power-supply design yielding data-sheet performance in many applications.

References

1. Rob Reeder and Neeraj Gill, "Clutter-free power supplies for RF converters in radar applications (Part 1)," Texas Instruments Analog Design Journal (SLYT811), 2Q 2021.
2. High-Speed Data Converter Pro software, Texas Instruments Design Resources.
3. Rob Reeder and Steve Schnier, "Powering Sensitive ADC Designs with the TPS62913 Low-Ripple and Low-Noise Buck Converter," Texas Instruments Application Report (SLVAEW7), September 2020.

Related Web sites

Product information:
ADC12DJ5200RF
TPS62913

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