Using a second stage filter to reduce voltage ripple

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Introduction

Advanced processors and system-on-chip (SoC) with integrated point-to-point serial communication or an analog front end (AFE) require a power supply with low output-voltage ripple to maintain signal integrity and improve performance. The output-voltage ripple requirement of the processor's point-of-load (POL) power supply can be below 2-mV, which is about one-tenth of the ripple for a typical design, putting heavy design constraint on the synchronous buck converter. Since the processor's output current requirements exceed the capabilities of a linear post-regulator, employing a second-stage filter, a higher switching frequency and additional output capacitance greatly reduce the POL's ripple. Synchronous-buck converters are available with several different control architectures, each having a unique method to ensure stability when designing for low-ripple voltage. This article compares three different control architectures: externally-compensated voltage-mode, constant on-time and selectable-compensation current-mode to achieve 1-mV output voltage ripple complete with test data using the same electrical specifications and comparison of output voltage ripple, solution size, load transients and efficiency.

Selecting and bounding the application

Three different power supplies were designed and built to demonstrate the performance of each control mode under similar operating conditions. For each design, the input voltage is 12 V, the output voltage is 1 V and the output current for each device is capable of 15-A. These requirements are typical for powering a high-performance SoC that integrates sensitive analog circuitry, requiring low output voltage ripple.

To bound the filter design and performance expectations, the allowable ripple voltage is ±0.15 percent, or ±1.5 mV (3 mVpp) of the output voltage. Our comparison features three TI DC/DC converters: a 15-A D-CAP3™ buck converter (**TPS548A28**), a 20-A internally compensated advanced current-mode (ACM) buck converter (**TPS543B22**) and a 15-A voltage-mode buck converter (**TPS56121**). We selected output voltage, output current and operating frequencies as close as possible to one another within the converter's capability to support similar second-stage filter components.

Designing the second-stage filter

Even with low equivalent series resistance (ESR) ceramic output capacitors, it is not practical to use a buck converter's inductor and capacitor (LC) output filter to achieve low output voltage ripple. Designers will likely need to use a second-stage LC filter in order to achieve output ripple below 5-mV. For more information about the design of a second-stage filter or the ripple measuring techniques, please see resources section. The value of the inductor of the second-stage filter can be calculated using **Equation 1** and solving for L2. The inductor L2 is the second-stage inductor, C1 is the primary-stage output capacitor of the buck converter, and C2 is the second-stage capacitor network. For all three designs, the same second-stage filter was used (as shown in **Table 1**), occupying a circuit board area of 92mm^2 (as shown in **Figure 1**).

$$Switching\ Frequency = 1/\left(2\pi * \sqrt{L2 * Cs}\right),\ where\ Cs = 1/\left(\frac{1}{C1} + \frac{1}{C2}\right) \quad (1)$$

Part Number	Control Architecture	Switching Frequency	Second-Stage Inductance	Second-Stage Capacitance
TPS548A28	D-CAP3	800 kHz	2 x 0.68 µH	4x 100 µF + 0.1 µF
TPS543B22	ACM	1000 kHz	2 x 0.68 µH	4x 100 µF + 0.1 µF
TPS56121	Voltage-Mode	500 kHz	2 x 0.68 µH	4 x 100 µF + 0.1 µF

Table 1. *Converter control architecture and second-stage filter.*

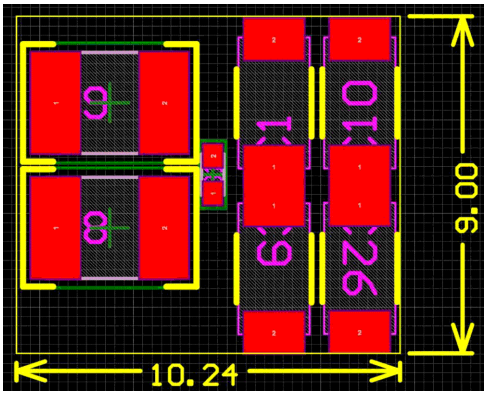

Figure 1. *Circuit board area of second-stage filter at 92mm².*

Once the second-stage inductor value (L2) is chosen and the components are assembled, the next step is to re-compensate the DC/DC converter's control loop with the addition of the second-stage inductance and capacitance to ensure stability. It is important to mention that each control architecture has its own unique technique to re-compensate the control loop after adding the second stage filter, if needed. The output voltage ripple, efficiency penalty and stability of each control architecture were evaluated and then summarized the results.

Voltage-mode control architecture

Pulse-width modulation (PWM) with voltage-mode control architecture is accomplished by comparing a voltage error signal from the output voltage and reference voltage to a constant sawtooth-ramp waveform. The ramp is initiated by a clock signal from an oscillator. The **TPS56121** employs externally-compensated, type-3 compensation addressing a double-pole power stage that allows the converter to be re-compensated after the addition of a second-stage filter. Adjusting external resistor and capacitor values after the addition of a second stage filter ensures stability. The output voltage peak-to-peak ripple without an additional filter is 4.8-mV. With the additional filter applied, the output voltage ripple is 1.9-mV (as shown in **Figure 2**). In this case, the TPS56121 design required no loop compensation adjustments to ensure stability. **Figure 3** shows a load transient waveform with a 10-A load-step, and the output voltage waveform after the implementation of the second-stage filter shows no sign of instability.

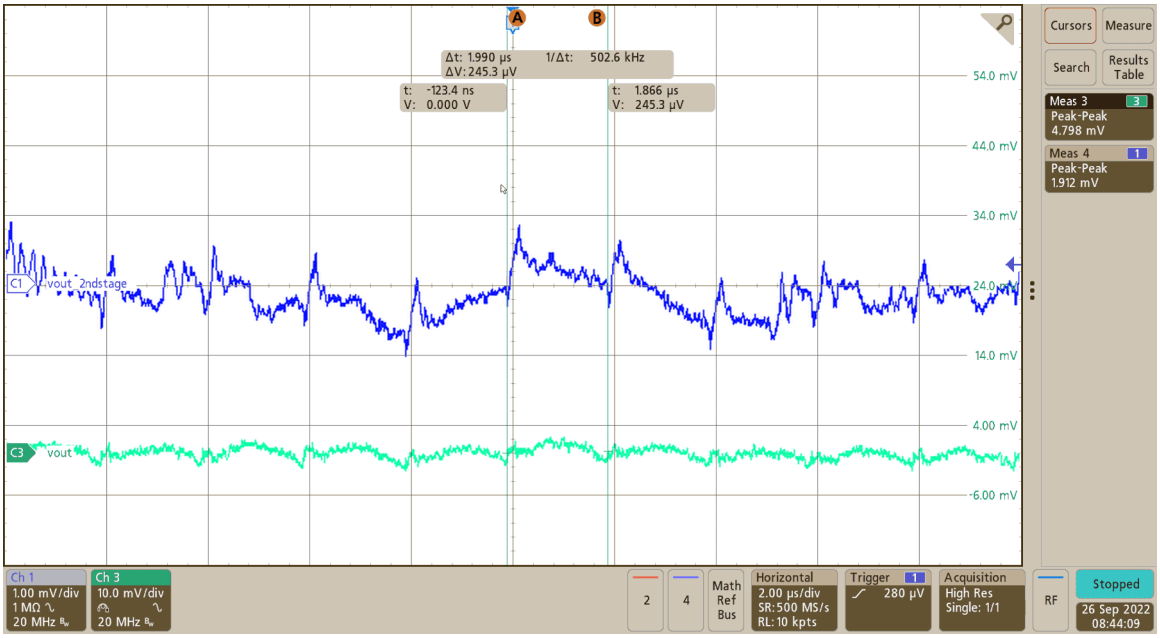

Figure 2. *TPS56121 output voltage ripple with and without additional second-stage filter.*

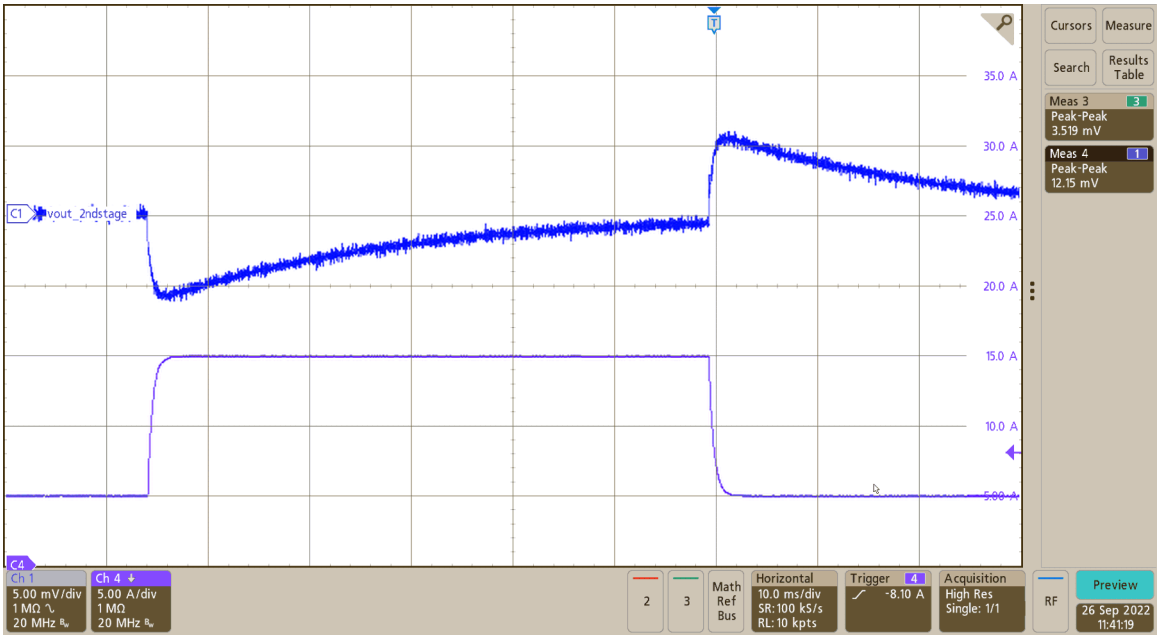

Figure 3. *Transient response of TPS56121 using voltage-mode control.*

D-CAP3 control architecture

D-CAP3 uses a one-shot timer to generate an on-time pulse that is proportional to the input voltage and the output voltage. When the falling feedback voltage equals the reference voltage, a new PWM on-pulse is generated. The ramp is emulated by the output inductor. A signal from an internal ripple-injection circuit is fed directly into the comparator with its offset voltage eliminated, reducing the need for output voltage ripple from the capacitor's ESR. One advantage of D-CAP3 and other constant on-time converters is additional loop compensation circuitry is not required. But, the control loop may have the ability adjusted by an adjustable ramp, if the device supports this feature, and the addition of feed forward capacitance at the

output voltage feedback resistor divider network. The **TPS548A28** output voltage peak-to-peak ripple without an additional filter is 7.6-mV. With the additional filter applied, the output voltage ripple is 2.3-mV (as shown in **Figure 4**). In this case, the **TPS548A28** design required no adjustments to ensure stability. **Figure 5** shows a load transient waveform with the same 10-A load-step as the previous converter, and the output voltage waveform after the implementation of the second-stage filter shows no sign of instability.

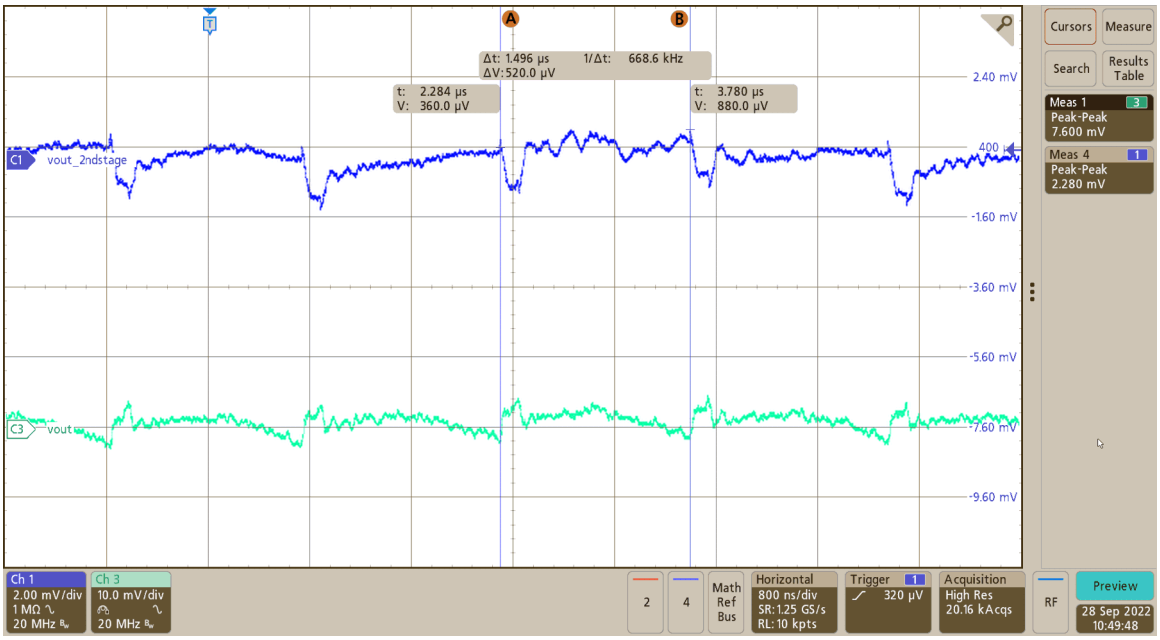

Figure 4. *TPS548A28 output voltage ripple with and without additional second-stage filter.*

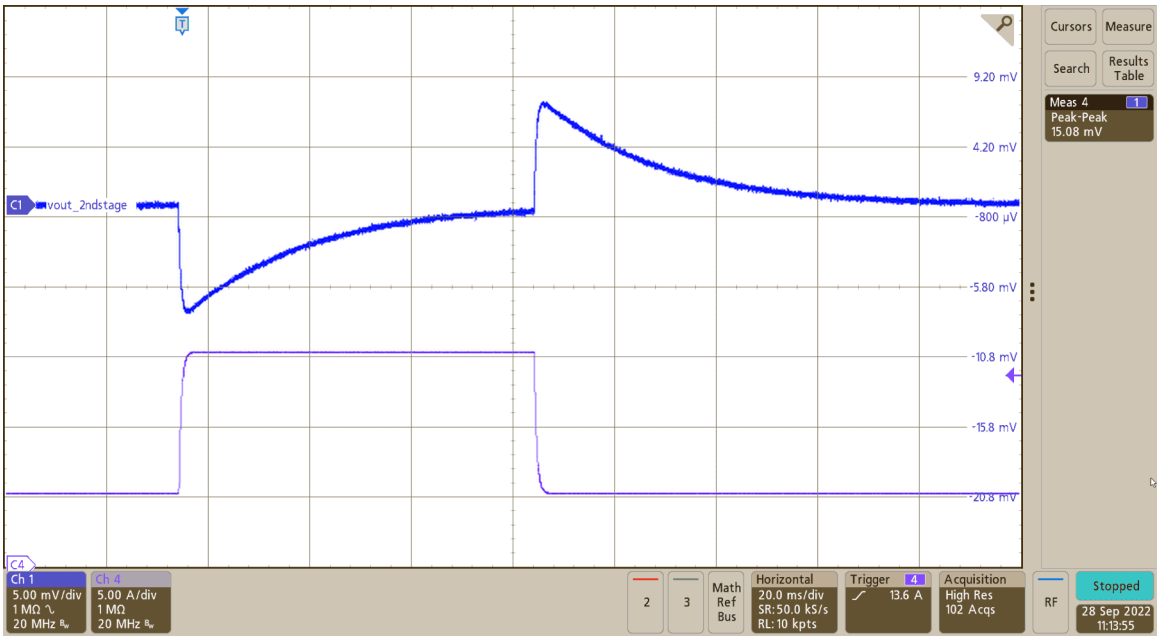

Figure 5. *Transient response of TPS548A28 using D-CAP3 control.*

Advanced current mode (ACM) control architecture

Internally-compensated ACM is a ripple-based, peak-current-mode control scheme that uses an internally generated ramp to represent the inductor current. This control mode provides a balance between the faster transient response of non-linear control modes, like D-CAP3, and the broad capacitor stability of other externally-compensated, fixed-frequency control architectures, like voltage-mode control. ACM is a newer control architecture that allows the loop to be compensated with a single resistor instead of a resistor and capacitor network. The **TPS543B22** has three selectable PWM ramp options to optimize the control loop performance when a second stage filter is implemented. Interestingly, we noticed that its evaluation module has capacitor and inductor solder pads on the circuit board to conveniently accommodate second-stage filter components. The **TPS543B22** output voltage peak-to-peak ripple without an additional filter is 7.4-mV. With the additional filter applied, the output voltage ripple is 1.3-mV (as shown in **Figure 6**). The **TPS543B22** design required no adjustments to the ramp to ensure stability. **Figure 7** shows a load transient waveform with the same 10-A load-step as the previous converter, and the output voltage waveform after the implementation of the second-stage filter shows no sign of instability.

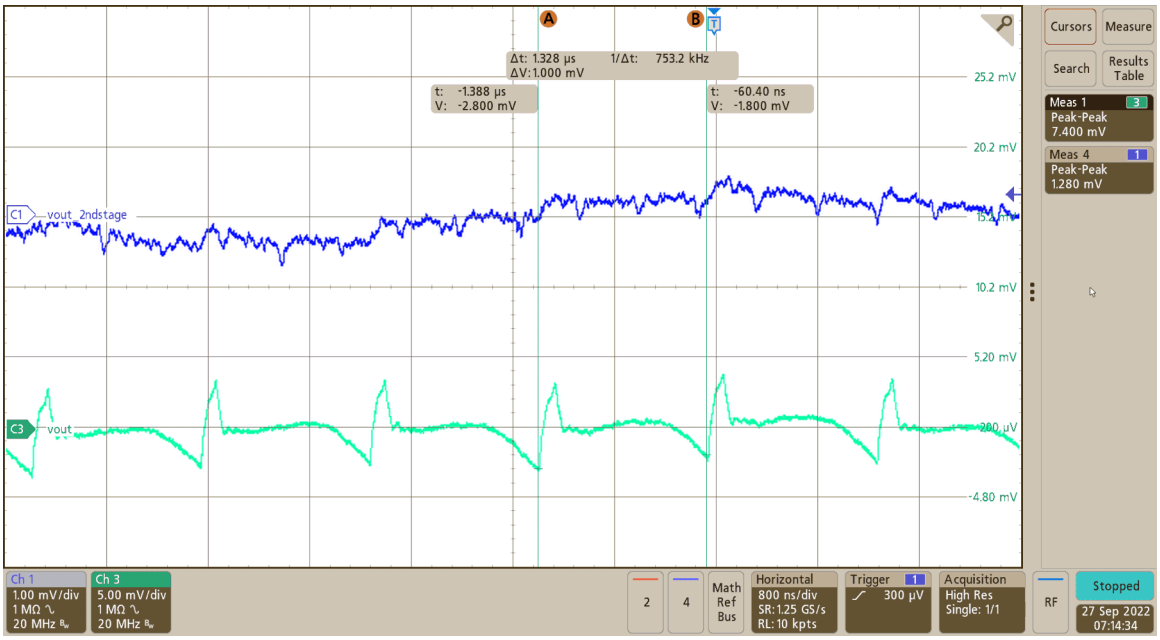

Figure 6. *TPS543B22 output voltage ripple with and without additional second-stage filter.*

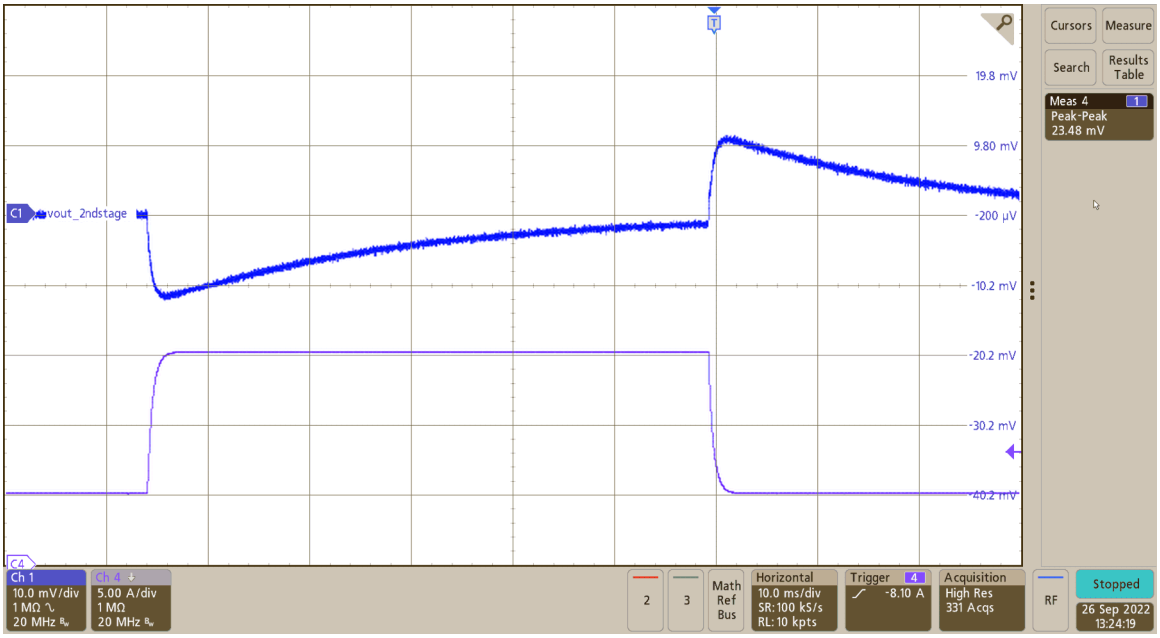

Figure 7. *Transient response of TPS543B22 using ACM control.*

Efficiency penalty

The full-load efficiency of each DC/DC converter was measured with and without the additional second-stage filter to compare the power losses. The results are shown in **Table 2**. The second-stage filter contributes negligible power loss and efficiency penalty. The deficiency and power loss differences were measured because each DC/DC converter has unique power MOSFETs, which lead to an inaccurate efficiency conclusion. It is the designer's decision to determine if the efficiency penalty and additional required board space of 92mm^2 is worth the output voltage ripple improvement.

Designers have traditionally used an additional low drop-out (LDO) regulator to post-regulate the output voltage of a DC/DC converter and achieve low output voltage ripple. If a designer prefers to use anLDO instead of a second-stage filter, the 4-A **TPS7A54** can be paralleled to provide up to 8-A. For example, if the LDO has a 175-mV voltage drop, two LDOs will dissipate 1.4-W at 8-A versus 0.02-W of the second-stage filter. The LDO will have a lower output voltage ripple noise of 4 µV, but if the second-stage filter provides acceptable low output voltage ripple for the SoC and AFE, the advantages are a smaller design, less power loss and lower component cost.

P/N	Iout (A)	Filter	Efficiency	Power Loss (W)
TPS543B22	**15**	Primary	86.43%	2.358
		Primary + Secondary	86.33%	2.378
		Difference	-0.1%	-0.02
TPS548A28	**15**	Primary	83.98%	2.829
		Primary + Secondary	83.87%	2.850
		Difference	-0.11%	-0.021
TPS56121	**15**	Primary	89.19%	1.834
		Primary + Secondary	89.34%	1.806
		Difference	-0.15%	-0.028

Table 2. *Efficiency and power loss comparison.*

Conclusion

A second-stage filter is an easy, small, efficient and low-cost solution to design and provide low output voltage ripple for high current loads. There is no perfect control mode for every design situation, but a second-stage filter can be implemented in many buck converter control architectures. If you are designing with a network interface card SoC or a remote radio unit using an AFE, a second-stage filter will provide much lower ripple than a standard buck converter. **Table 3** summarizes the ripple and the efficiency and size trade-offs associated with each device.

Device	Current Capability (A)	Control Architecture	Ripple Voltage (mV)	Filter Size	Power Loss penalty (W)
TPS543B22	20	ACM	1.3	92mm^2	0.020
TPS548A28	15	D-CAP3	2.3	92mm^2	0.021
TPS56121	15	Voltage Mode	1.9	92mm^2	0.028

Table 3. *Ripple, size and efficiency trade-offs.*

References

1. Texas Instruments: **Power Tips: Designing a two-stage LC filter**
2. Texas Instruments: ***Reducing noise on the output of a switching regulator***
3. Texas Instruments: ***Control-Mode Quick Reference Guide - Step-Down Non-Isolated DC/DC***

Related Websites

- **TPS548A28** - 2.7-V to 16-V, 15-A synchronous buck converter with remote sense and 3-V LDO
- **TPS543B22** - 4-V to 18-V input, advanced current mode, 20-A synchronous SWIFT™ step-down converter
- **TPS56121** - 4.5-V to 14-V, 15-A synchronous SWIFT™ buck converter
- **TPS7A54** - 4-A, low-VIN (1.1-V), low-noise, high-accuracy, ultra-low dropout voltage regulator

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