Texas Instruments

TMS28F512A 512K Flash Memory

Technical Brief

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TMS28F512A
512K Flash EEPROM
Technical Brief

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Chapter 1

Introduction

About This Technical Brief

This technical brief was developed to provide you with details about our 512K Flash memory device that aren't available in data sheets or application notes. We hope you find this information package helpful and easy to use.

Description	The TMS28F512A is a 524 288-bit Flash memory organized as 64K $\times$ 8
Technology	CMOS H-Cell 0.8μm
Fabrication	Wafer Fabrication: TI LMOS (Lubbock, Texas)
	Assembly and Test: TI SGP (Singapore)
Package	32-pin plastic leaded-chip carrier package (PLCC) using 50-mil lead spacing
Customer Assistance	Marketing: Bob Darilek . . . . (713) 274-3342
	Customer Quality Engineering: Lee Bowman . . . (713) 274-4147

Chapter 2

Device Information

Vendor Name Texas Instruments Inc.

Vendor Part Number TMS28F512A FML

- **CMOS Technology**
  - **Memory type** Electrically Erasable PROM
  - **Density** 64K × 8
  - **Number of Metal Layers / Composition**
    1: Ti / TiW / AlSi (1%) Cu (0.5%)
  - **Number of Poly Layers**
    2: P1 = Poly Si
    P2 = Polycide (WSi / Poly)
  - **CMOS Well** Twin Well
  - **Mask List by Level** 16
- **Package Type**
  - **Number of Pins** 32
  - **Width** 0.450 in × 0.550 in
  - **Package Material** Plastic
  - **Lead Plate Material** SN / PB
  - **Wire Bond Material** Gold
  - **Wire Bond Technology**
    Thermosonic
  - **Die Attach Material** Ablebond 71-1
  - **Leadframe Material** Alloy 42
  - **Assembly Site** Singapore

- **Device Process Information**
  - **Passivation** Oxide over Oxynitride
  - **Die Size** 178 Mils × 159 Mils
  - **Memory Cell Size** 2.8 µm × 3.25 µm
  - **Wafer Diameter** 125mm
  - **Wafer Fabrication** Lubbock, Texas, USA

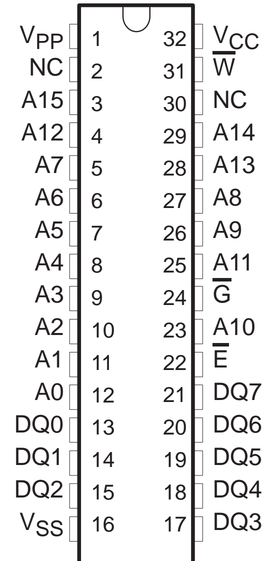
- **Test Process Data**
  - **Wafer Test Site** Lubbock, Texas, USA
  - **Final Test Site** Singapore
  - **Final Test Production Tester**
    TI NEM
  - **Tester Used for Datalogged Units**
    GENESIS

- **Organization . . . 64K × 8-Bit Flash Memory**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time:**

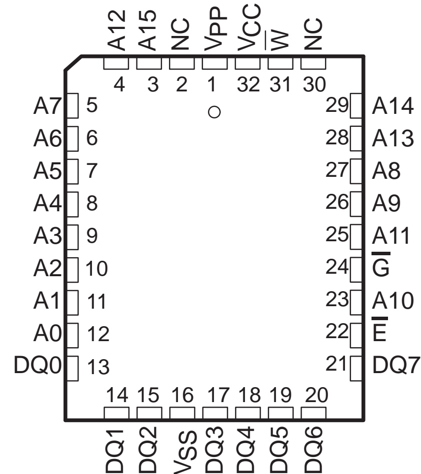
V_{CC} ± 10%	
’28F512-10	100 ns
’28F512-12	120 ns
’28F512-15	150 ns
’28F512-17	170 ns

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10 000, 1 000 and 100 Program/Erase Cycle Versions**
- **Low Power Dissipation (V_{CC} = 5.50 V)**
  - **– Active Write . . . 55 mW**
  - **– Active Read . . . 165 mW**
  - **– Electrical Erase . . . 82.5 mW**
  - **– Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range: – 40°C to + 125°C**

N PACKAGE†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{W}$	Write Enable
DQ0–DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply
V_{SS}	Ground

description

The TMS28F512A is a 524 288-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed.

The TMS28F512A is available in 10 000, 1 000, and 100 program/erase endurance cycle versions.

The TMS28F512A Flash EEPROM is offered in a dual in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) centers, a 32-lead plastic leaded-chip carrier package using 1,25 mm (50-mil) lead spacing (FM suffix), a 32-lead thin small outline package (DD suffix), and a reverse pinout TSOP package (DU suffix).

The TMS28F512A is offered with three choices of temperature ranges of 0°C to 70°C (NL, FML, DDL, and DUL suffixes), –40°C to 85°C (NE, FME, DDE, and DUE suffixes), and –40°C to 125°C (NQ, FMQ, DDQ, and DUQ suffixes). All package types are offered with 168 hour burn-in (4 suffix).

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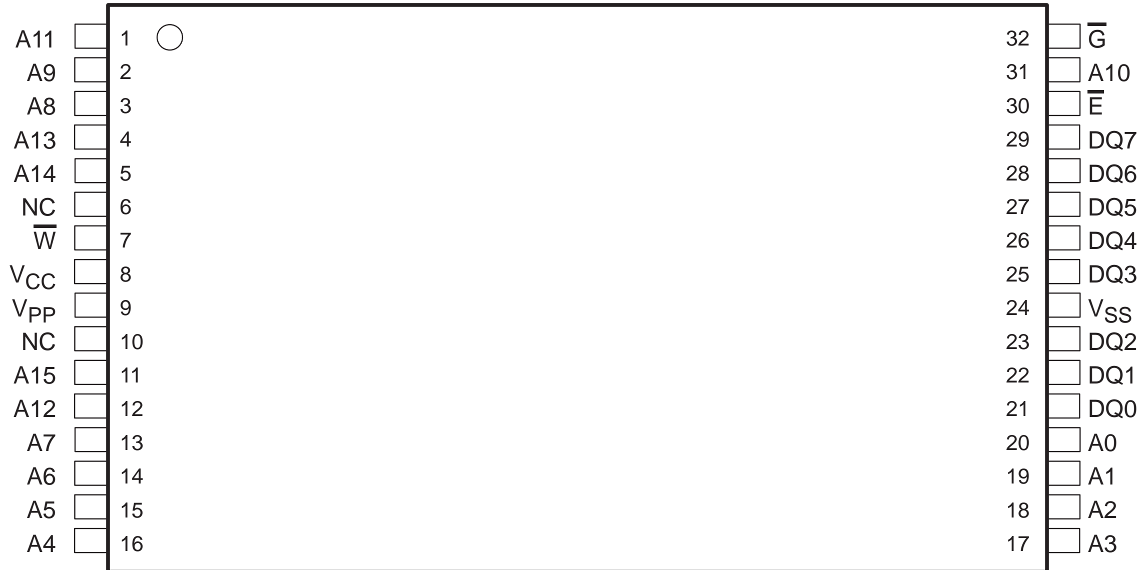
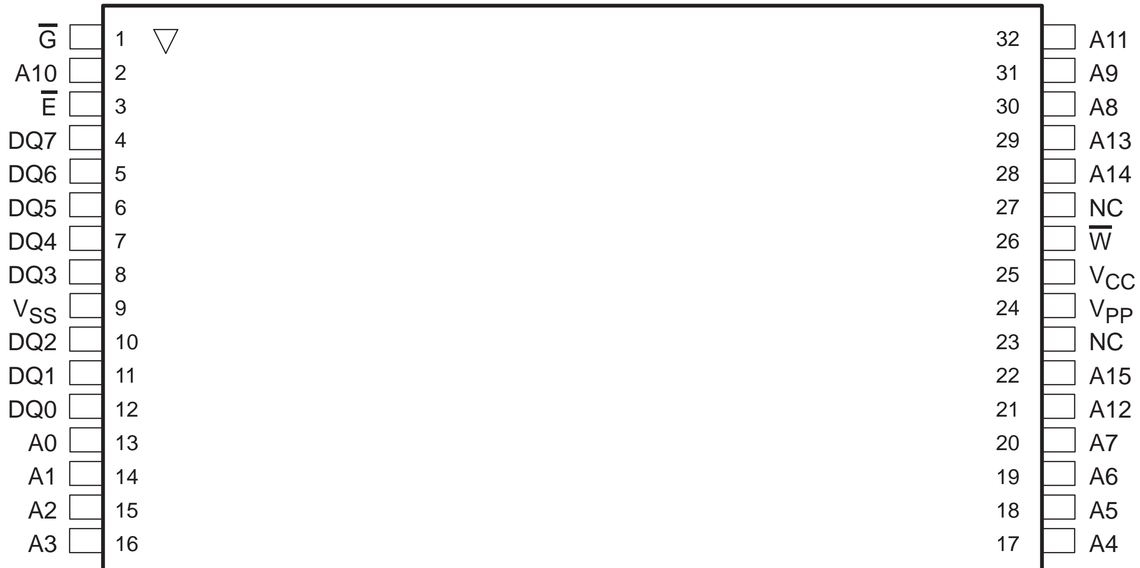
DD PACKAGE†
(TOP VIEW)

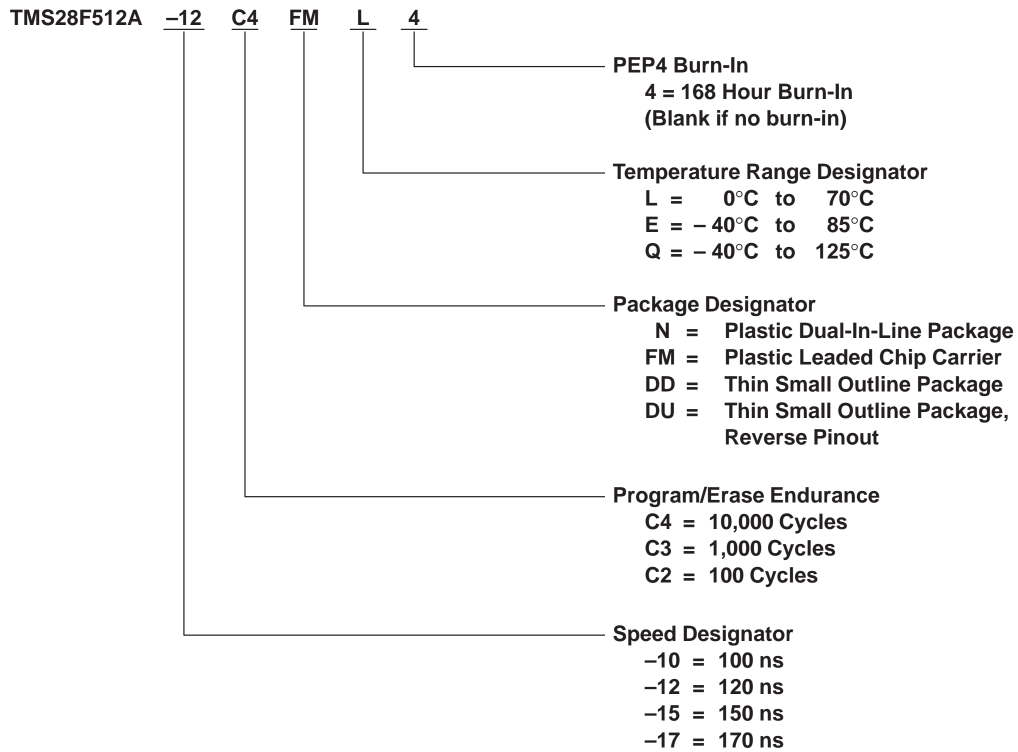


DU PACKAGE†
REVERSE PINOUT
(TOP VIEW)



† The packages shown are for pinout reference only.

device symbol nomenclature



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functional block diagram

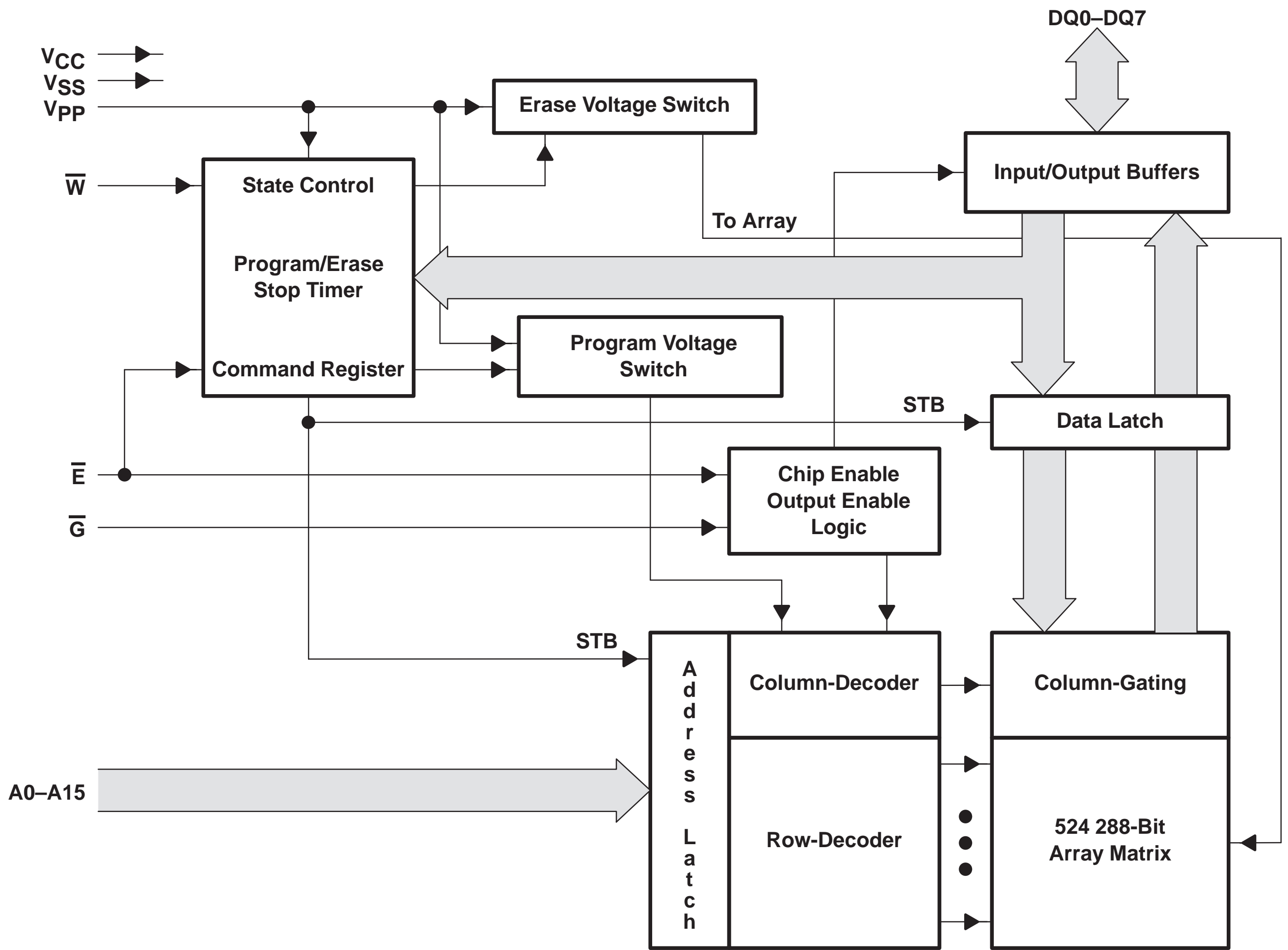

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Table 1. Operation Modes

MODE†		FUNCTION						
		V_{PP}§ (1)	$\overline{E}$ (22)	$\overline{G}$ (24)	A0 (12)	A9 (26)	$\overline{W}$ (31)	DQ0–DQ7 (13–15, 17–21)
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X†	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	HI-Z
	Algorithm Selection Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_H‡	V_{IH}	MFG Code 97h
					V_{IH}			Device Code 73h
Read/Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	HI-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}
‡ 11.5 V < V_H < 13.0 V
§ $V_{PPL} \leq V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F512As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices.

To read the output of the TMS28F512A, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 μA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F512A draws active current when it is deselected during programming, erasure, or program/erase verification. It will continue to draw active current until the operation is terminated.

algorithm selection mode

The algorithm selection mode provides access to a binary code identifying the correct programming and erase algorithms. This mode is activated when A9 (pin 26) is forced to V_H. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer-equivalent code 89h, and A0 high selects the device code B8h, as shown in the algorithm selection mode table below:

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Code	V_{IL}	1	0	0	0	1	0	0	1	89
Device Code	V_{IH}	1	0	1	1	1	0	0	0	B8

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A15 = V_{IL}, $V_{PP} = V_{PPL}$.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1's, may be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

command register

The command register controls the program and erase functions of the TMS28F512A. The algorithm selection mode may be activated using the command register in addition to the above method. When V_{PP} is high, the contents of the command register, and therefore the function being performed, may be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1 µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} will require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

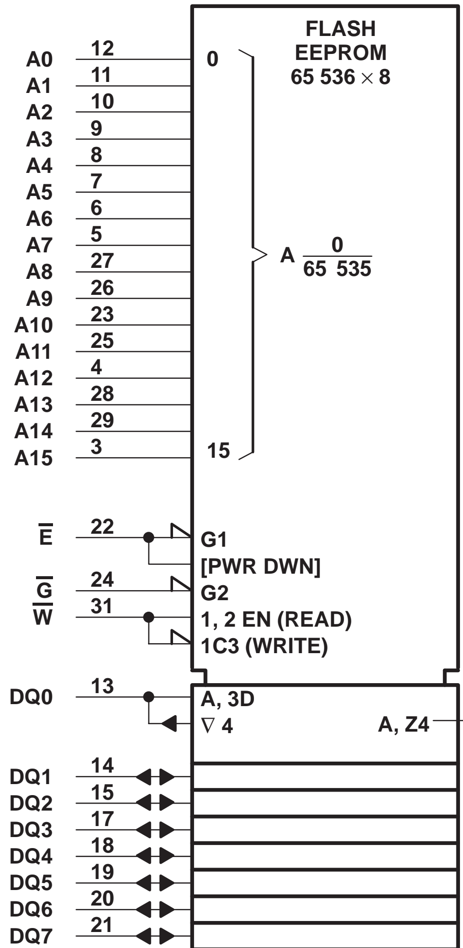
COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION (see Note 1)	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Algorithm Selection Mode	3	Write	X	90h	Read	0000 0001	89h B8h
Set-up Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA†	A0h	Read	X	EVD
Set-up Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

NOTE 1: Modes of operation are defined in Table 1.

† Description of Terms

- EA Address of memory location to be read during erase verify.
- RA Address of memory location to be read.
- PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
- RD Data read from location RA during the read operation.
- EVD Data read from location EA during erase verify.
- PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
- PVD Data read from location PA during program verify.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

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command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. Also, when the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different, valid command is written to the command register.

algorithm selection mode command

The algorithm selection mode is activated by writing 90h into the command register. The manufacturer-equivalent code (89h) is identified by the value read from address location 0000h, and the device-equivalent code (B8h) is identified by the value read from address location 0001h.

set-up erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, V_{PP} = 12 V, and V_{CC} = 5 V. To enter the erase mode, write the set-up erase command, 20h, into the command register. After the TMS28F512A is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase verify, read, or reset command is received.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F512A applies a margin voltage to each byte. If FFh is read from the byte, then all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, then an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F512A.

set-up program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, V_{PP} = 12 V, and V_{CC} = 5 V. To enter the programming mode, write the set-up program command, 40h, into the command register. The programming operation will be invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program verify, read, or reset command is received.

program-verify command

The TMS28F512A can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed.

The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation will end on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F512A applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming can continue to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

reset command

To reset the TMS28F512A after set-up erase command or set-up program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F512A is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

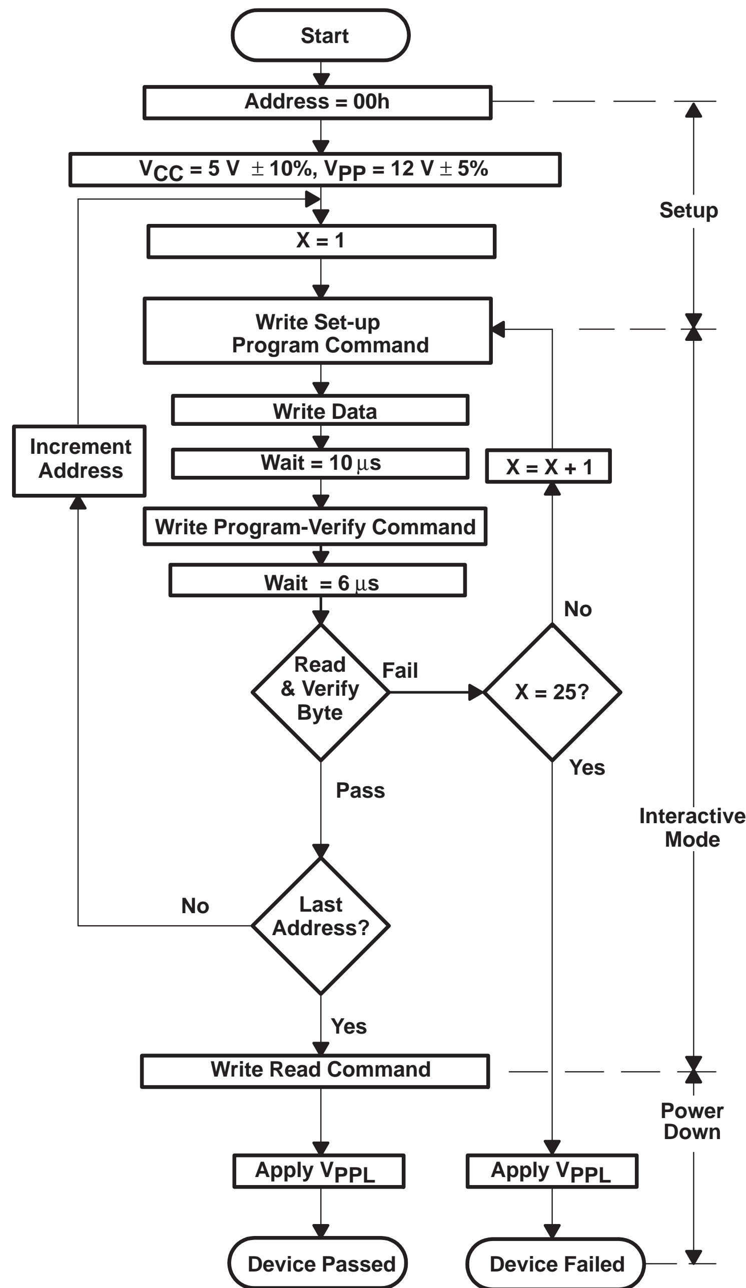
Fasterase algorithm

The TMS28F512A is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices may be erased in parallel. Since each Flash EEPROM may erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished. See Figure 3, Parallel Erase Flow Diagram.

Examples of how to mask a device during parallel erase include driving the device's $\overline{E}$ pin high, writing the read command (00h) to the device when the others receive a setup erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.



Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for V_{PP} to Ramp to V_{PPH} (see Note 2) Initialize Pulse Count
Write	Set Up Program Write	Data = 40h
Write	Write Data	Valid Address/Data
Standby		Wait = 10 µs
Write	Program-Verify	Data = C0h; Ends Program Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Programming; Compare Output to Expected Output
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for V_{PP} to Ramp to V_{PPL} (see Note 3)

NOTES: 2. Refer to the recommended operating conditions for the value of V_{PPH}.
3. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm

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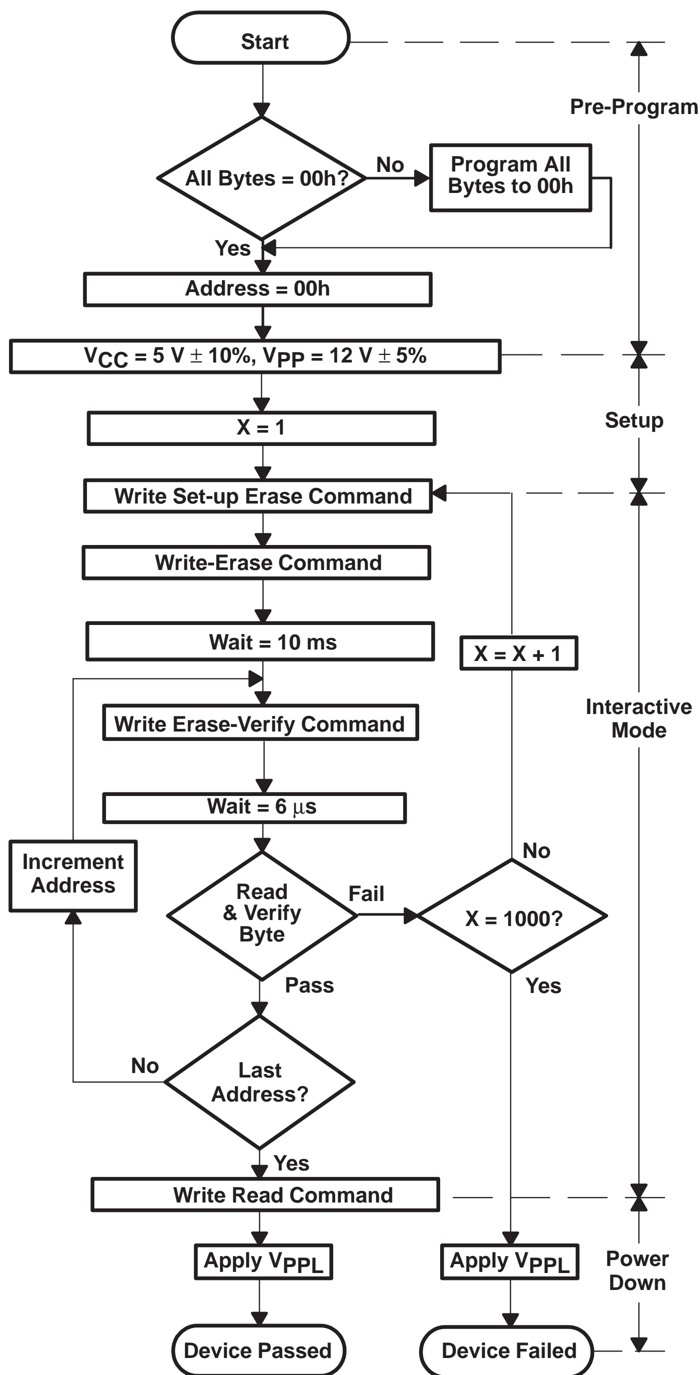
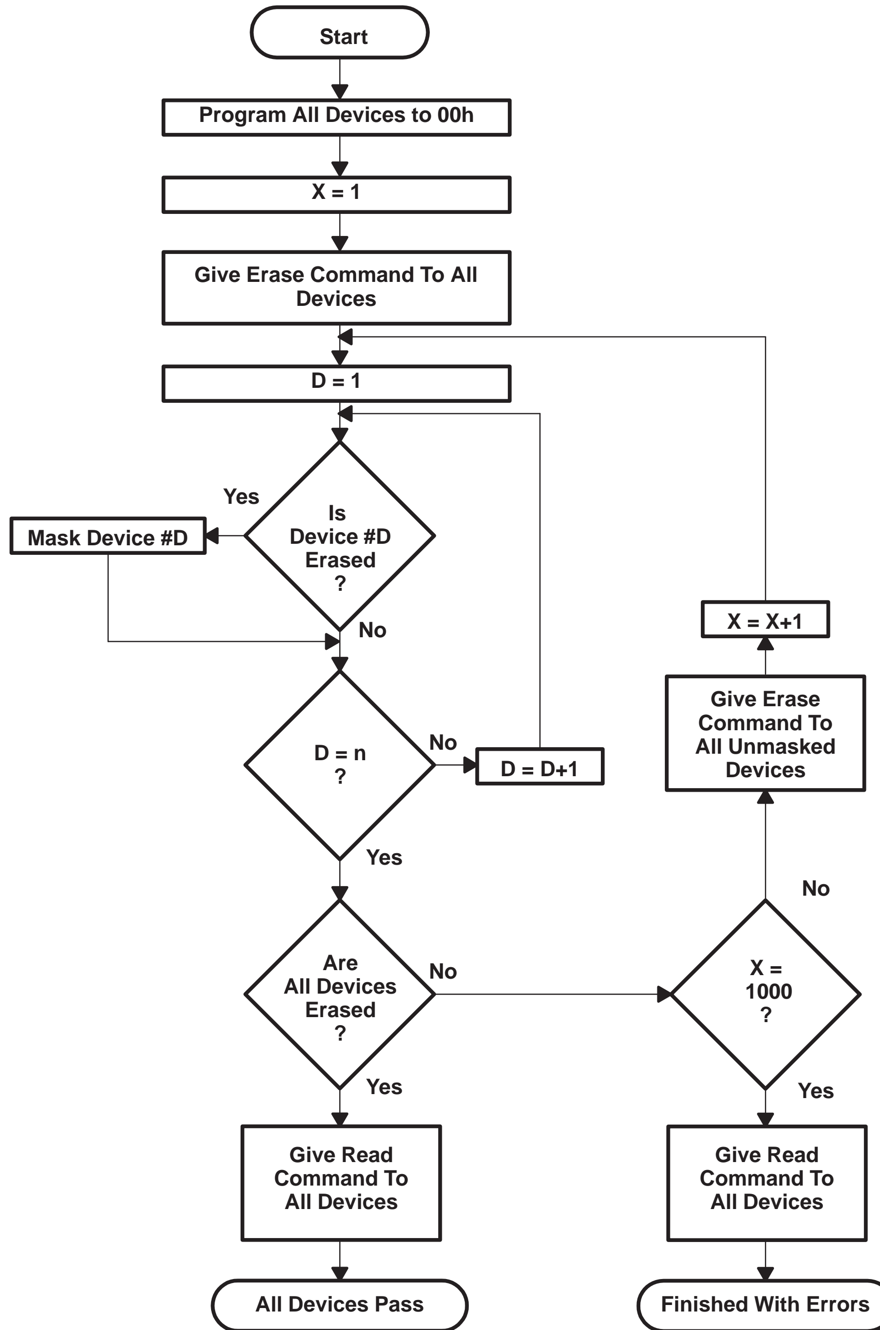


Bus Operation	Command	Comments
		Entire Memory Must = 00h Before Erasure Use Fastwrite Programming Algorithm
		Initialize Addresses
Standby		Wait for V_{PP} to Ramp to V_{PPH} (see Note 2)
		Initialize Pulse Count
Write	Set Up Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Byte to Verify; Data = A0h; Ends the Erase Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Erasure; Compare Output to FFh
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for V_{PP} to Ramp to V_{PPL} (see Note 3)

NOTES: 2 Refer to the recommended operating conditions for the value of V_{PPH}.
3 Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm



NOTE: n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4)	−0.6 V to 7 V
Supply voltage range, V_{PP}	−0.6 V to 14 V
Input voltage range (see Note 5): All inputs except A9	−0.6 V to V_{CC} + 1 V
A9 (see Note 5)	−0.6 V to 13.5 V
Output voltage range (see Note 6)	−0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program (NL, FML, DDL, DUL)	0°C to 70°C
Operating free-air temperature range during read/erase/program (NE, FME, DDE, DUE)	– 40°C to 85°C
Operating free-air temperature range during read/erase/program (NQ, FMQ, DDQ, DUQ)	– 40° C to 125°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to GND.
5. The voltage on any input pin may undershoot to –2.0 V for periods less than 20 ns.
6. The voltage on any output pin may overshoot to 7.0 V for periods less than 20 ns.

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recommended operating conditions

				’28F512A-10 ’28F512A-12 ’28F512A-15 ’28F512A-17			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})		0		V_{CC} + 2	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.5		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	–0.5		0.8	V
			CMOS	GND – 0.2		GND+0.2	

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	2.4			V
			I_{OH} = – 100 µA	V_{CC} – 0.4			
V_{OL}	Low-level output voltage		I_{OL} = 5.8 mA			0.45	V
			I_{OL} = 100 µA			0.1	
I_I	Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	µA
		A9	VI = 0 to 13 V			± 200	
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±10	µA
I_{PP1}	V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, read mode			200	µA
			VPP = V_{PPL}			±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP4}	VPP supply current (during program/erase verify) (see Note 7)		V_{PP} = V_{PPH}			5.0	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			100	µA
I_{CC1}	V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, outputs open			30	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, programming in progress			10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, erasure in progress			15	mA
I_{CC4}	V_{CC} average supply current (program/erase verify) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, program/erase-verify in progress			15	mA

NOTE 7: Not 100% tested; characterization data available.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1MHz			6	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz			12	pF

† Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

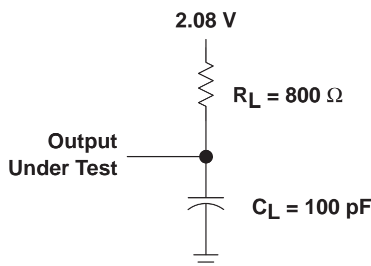

Figure 4. AC Test Output Load Circuit

AC testing input/output wave forms

AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1 µF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

ADVANCE INFORMATION

switching characteristics over full ranges of recommended operating conditions

DESCRIPTION		TEST CONDITIONS	ALTERNATE SYMBOL	’28F512A-10		’28F512A-12		’28F512A-15		’28F512A-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load Input $t_r \leq$ 20 ns Input $t_f \leq$ 20 ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from chip enable		t_{ELQV}		100		120		150		170	ns
$t_{en(G)}$	Access time from output enable		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Read cycle time		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, chip enable low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, output enable low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable to hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Hold time, output enable to hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{wr(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first.

AC characteristics–write/erase/program operations

DESCRIPTION		ALTERNATE SYMBOL	’28F512A-10		’28F512A-12		’28F512A-15		’28F512A-17		UNIT
			MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVWL}	0		0		0		0		ns
$t_{h(A)}$	Address hold time	t_{WLAX}	55		60		60		70		ns
$t_{su(D)}$	Data setup time	t_{DVWH}	50		50		50		50		ns
$t_{hw(D)}$	Data hold time	t_{WHDX}	10		10		10		10		ns
$t_{wr(W)}$	Write recovery time before read	t_{WHGL}	6		6		6		6		µs
$t_{rr(W)}$	Read recovery time before write	t_{GHWL}	0		0		0		0		µs
$t_{su(E)}$	Chip enable setup time before write	t_{ELWL}	20		20		20		20		ns
$t_{h(E)}$	Chip enable hold time	t_{WHEH}	0		0		0		0		ns
$t_{w(W)}$	Write pulse duration (see Note 8)	t_{WLWH}	60		60		60		60		ns
$t_{wh(W)}$	Write pulse duration high	t_{WHWL}	20		20		20		20		ns
$t_{c(W)B}$	Duration of programming operation	t_{WHWH1}	10		10		10		10		µs
$t_{c(E)B}$	Duration of erase operation	t_{WHWH2}	9.5	10	9.5	10	9.5	10	9.5	10	ms
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{su(E)P}$	Chip enable, setup time to V_{PP} ramp	t_{EHVP}	100		100		100		100		ns
$t_{s(P)R}$	V_{PP} rise time	t_{VPPR}	1		1		1		1		µs
$t_{s(P)F}$	V_{PP} fall time	t_{VPPF}	1		1		1		1		µs

NOTE 8: Rise/fall time ≤ 10 ns.

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alternative $\overline{CE}$-controlled writes

	DESCRIPTION	ALTERNATE SYMBOL	'28F512A-10		'28F512A-12		'28F512A-15		'28F512A-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVEL}	0		0		0		0		ns
$t_{hE(A)}$	Address hold time	t_{ELAX}	75		80		80		90		ns
$t_{su(D)}$	Data setup time	t_{DVEH}	50		50		50		50		ns
$t_{hE(D)}$	Data hold time	t_{EHDX}	10		10		10		10		ns
$t_{wr(E)}$	Write recovery time before read	t_{EHGL}	6		6		6		6		µs
$t_{rr(E)}$	Read recovery time before write	t_{GHEL}	0		0		0		0		µs
$t_{su(W)}$	Write enable setup time before chip enable	t_{WLEL}	0		0		0		0		ns
$t_{h(W)}$	Write enable hold time	t_{EHWH}	0		0		0		0		ns
$t_{w(E)}$	Write pulse duration	t_{ELEH}	70		70		70		80		ns
$t_{wh(E)}$	Write pulse duration high	t_{EHEL}	20		20		20		20		ns
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{c(W)B}$	Duration of programming operation	t_{EHEH}	10		10		10		10		µs

PARAMETER MEASUREMENT INFORMATION

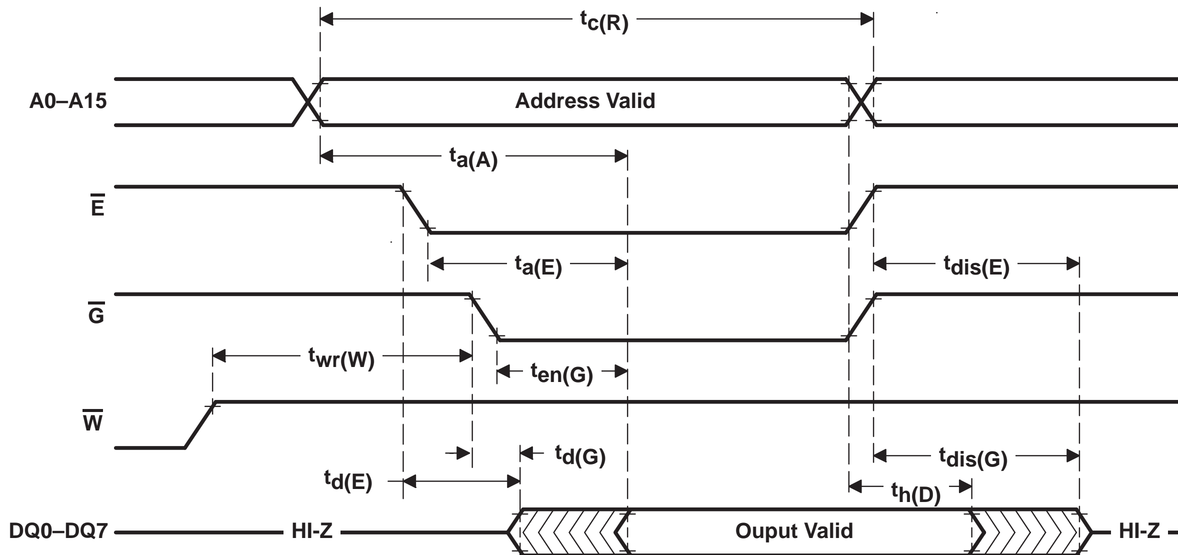

Figure 5. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

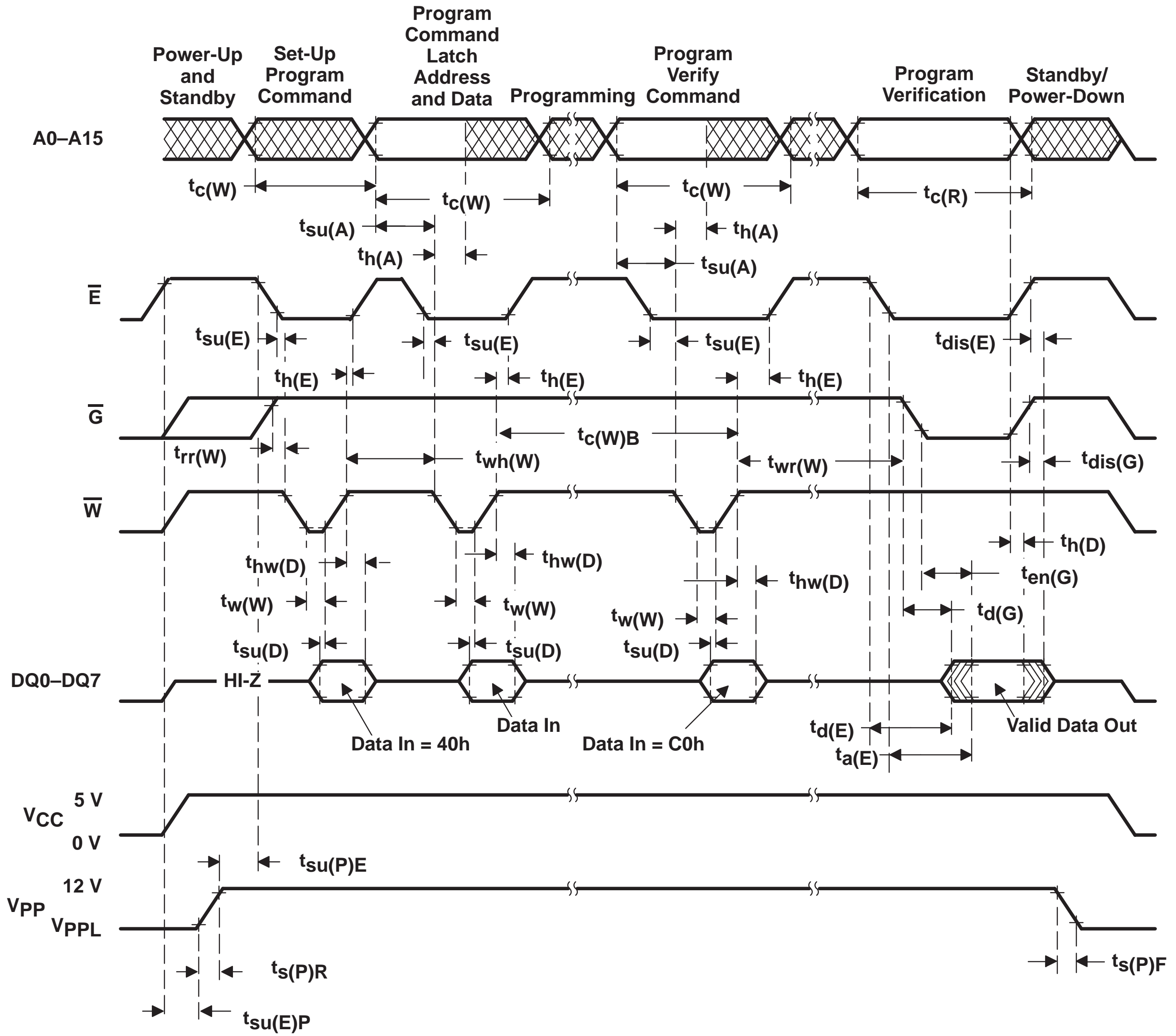

Figure 6. Write Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

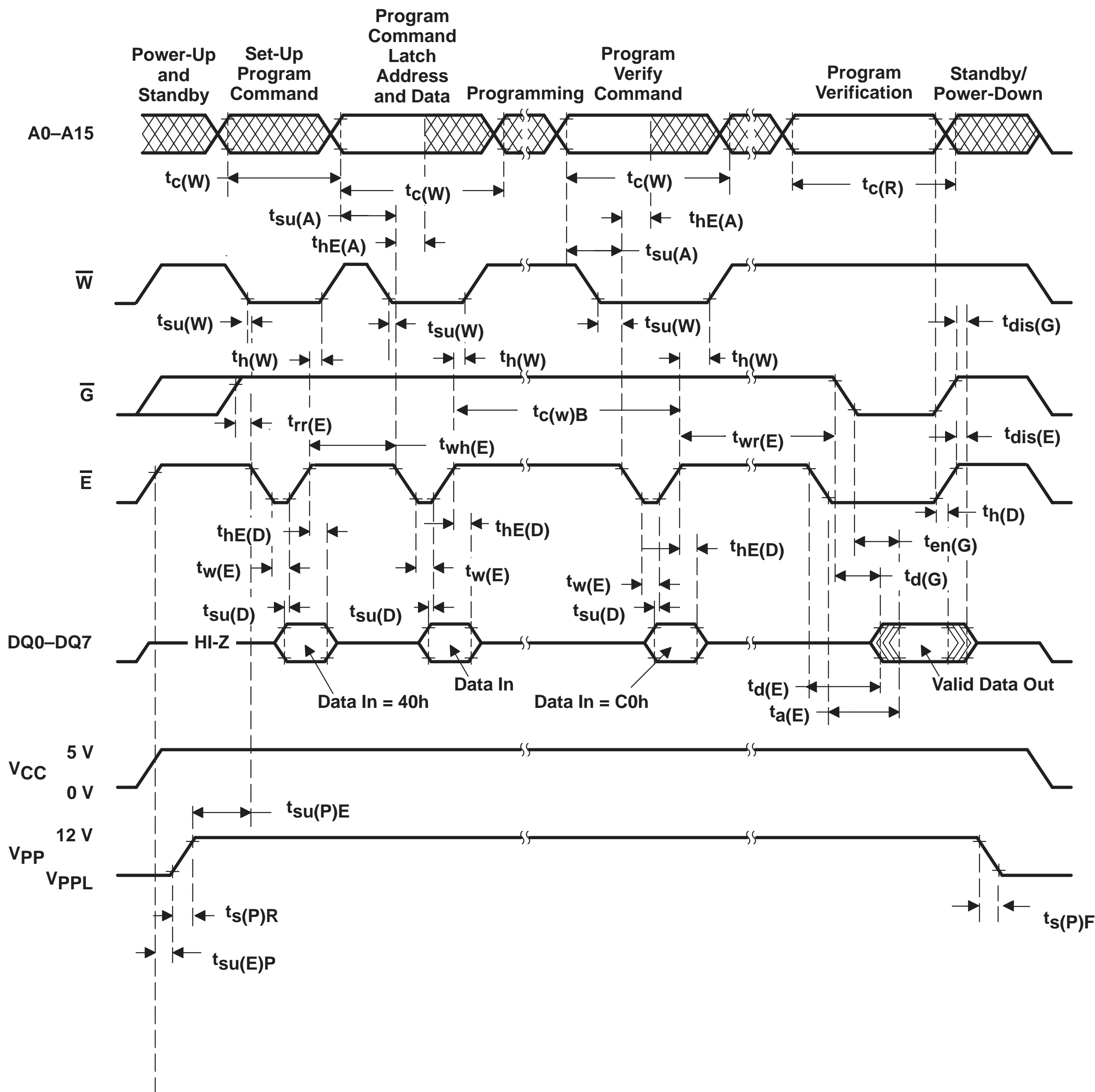

Figure 7. Write Cycle (Alternative $\overline{CE}$-Controlled Writes) Timing

ADVANCE INFORMATION

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

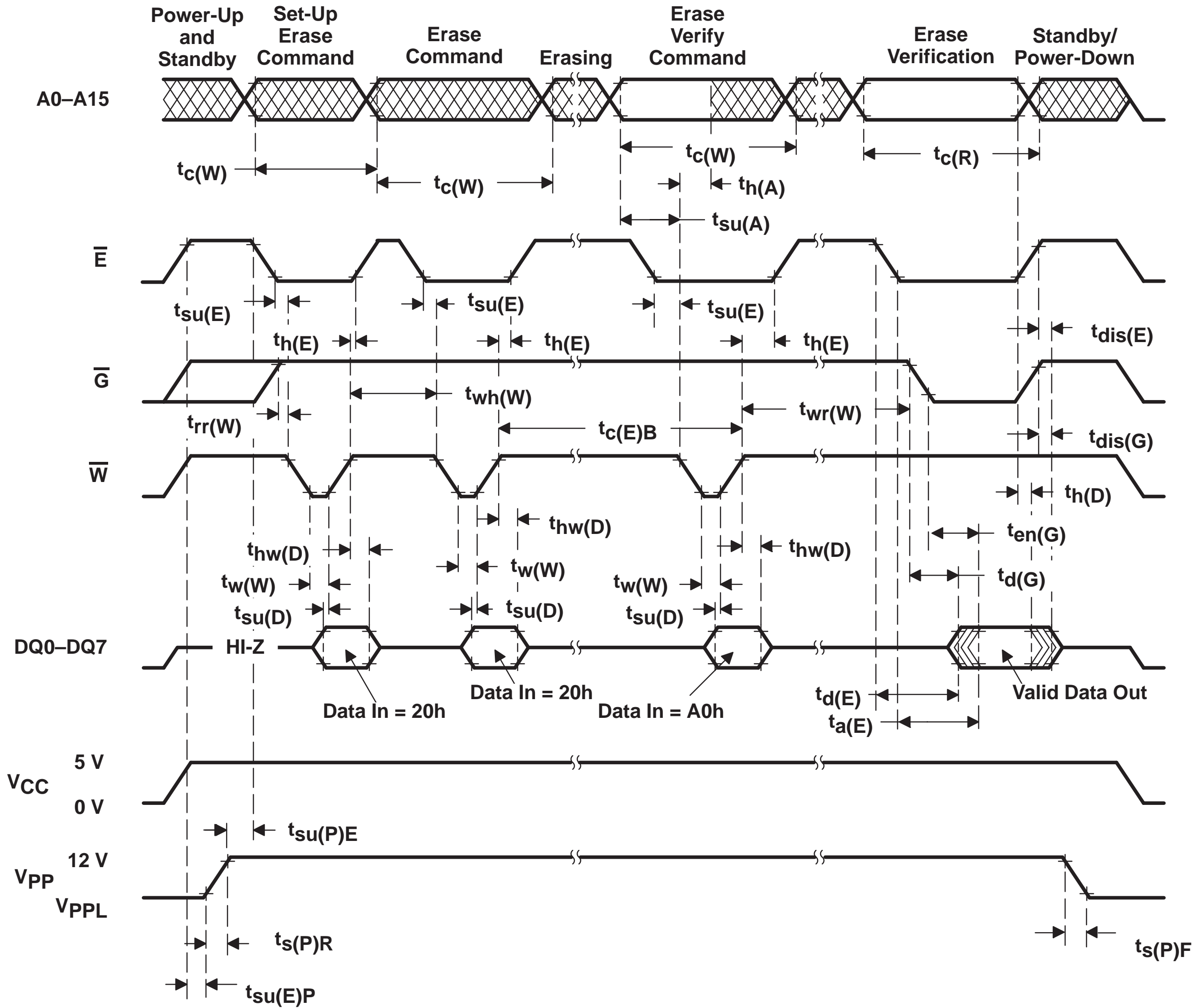

Figure 8. Flash-Erase Cycle Timing

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Chapter 4

Qualification Results

4.1 Summary of the TMS28F512A Qualification — 1000 hours

Read Hours →		96	168	240	336	500	1000	
Test	**Sample**							**Failures**
1K W/E + 125•C OPLIFE	200	–	0	–	–	0	0	0
1K W/E + 150•C BAKE	200	–	0	–	–	0	0	0
150 HTRB	150	–	0	–	–	0	0	0
85/85	200	–	0	–	0	–	0	0
Autoclave PCT	200	0	–	0	–	–	–	0

Cycles →		200	500	1000	
Test	**Sample**				**Failures**
T/C –65/150•C	200	0	0	0	0

Test	Sample	Failures
Latchup	10	0
Salt Atmosphere	22	0
Lead Finish Adhesion	22	0
Lead Integrity	22	0
Moisture Resistance	38	0
Solvent Resistance	44	0

1K W/E +125•C OPLIFE After completing 1K W/E endurance, the parts are operated at 125°C with input signals that exercise the part while outputs are loaded.

85/85 85•C and 85% relative humidity with pins alternately biased with V_{CC} and V_{SS}.

4.2 Reliability Test Descriptions

1K W/E +150•C BAKE After completing 1K W/E endurance, the parts undergo an unbiased storage test at150°C; per JEDEC STD 22, method A101.

150•C HTRB High temperature stress testing with appropriate biasing.

T/C –65/150•C (temp cycle) Devices are subjected to alternating ambient temperatures of –65°C and +150°C. Cycle time is 30 minutes with no ambient dwell; per Mil STD 883D, method 1010.

Autoclave PCT The parts are subjected to pressure cooker test at 121•C, 100% R.H. per JEDEC STD 22, method A102.

Lead Finish Adhesion Per Mil STD 883D, method 2025.

Lead Integrity Per Mil STD 883D, method 2004, condition A, B2, C1.

Solvent Resistance Per Mil STD 883D, method 2015.

Salt Atmosphere Per Mil STD-883D, method 1009, Condition A, 24 hours minimum.

Latchup Per JEDEC STD 17.

Moisture Resistance Per Mil STD 883D, method 1004.

Chapter 5

Electrical Characterization Data

Test Facility **Stafford**
Tester **GENESIS-II**
Pattern **Random pattern (50% of bits programmed)**
Device **TMS28F512A**

Wafer Lot Number	Number of Units
3118627	10
3132228	10
3146486	10
Total	**30**

	–40°C		25°C		125°C		
V_{CC}	AVG	STD	AVG	STD	AVG	STD	UNIT
1) V_{CC} Standby Current, TTL Level (spec = 1 mA)							
4.35V	82.01	5.253	69.40	4.024	63.28	2.380	μA
4.50V	104.46	6.666	85.92	5.439	75.76	4.173	μA
5.00V	192.44	9.964	150.84	6.193	126.04	6.391	μA
5.50V	294.81	14.923	230.80	8.610	188.28	6.901	μA
5.65V	327.86	16.042	256.00	9.952	207.29	8.666	μA
2) V_{CC} Standby Current, CMOS Level (spec = 100 μA)							
4.35V	6.11	1.921	6.45	1.892	7.28	1.348	μA
4.50V	6.89	1.743	7.05	1.567	7.80	0.000	μA
5.00V	7.80	0.000	7.20	1.435	7.80	0.000	μA
5.50V	7.80	0.000	7.80	0.000	7.80	0.000	μA
5.65V	7.80	0.000	7.80	0.000	7.80	0.000	μA
3) V_{CC} Active Read Current, TTL Level, f = 7.5 MHz (spec = 30 mA)							
4.35V	10.89	0.198	10.40	0.145	10.33	0.118	mA
4.50V	11.76	0.228	11.15	0.152	11.01	0.134	mA
5.00V	15.10	0.325	13.99	0.216	13.45	0.180	mA
5.50V	19.18	0.445	17.38	0.277	16.29	0.226	mA
5.65V	20.54	0.483	18.50	0.296	17.20	0.245	mA
4) V_{CC} Active Read Current, CMOS Level, f = 7.5 MHz – (spec = 30 mA)							
4.35V	10.92	0.182	10.44	0.144	10.30	0.113	mA
4.50V	11.68	0.197	11.12	0.148	10.92	0.123	mA
5.00V	14.49	0.278	13.58	0.191	13.12	0.154	mA
5.50V	17.88	0.367	16.48	0.235	15.62	0.198	mA
5.65V	18.99	0.388	17.42	0.254	16.40	0.200	mA
5) V_{OL} Measurement, V_{CC} = 4.35V, I_{OL} 5.8 mA (spec = 0.45 V):							
V_{OL}	183.37	8.299	249.12	2.688	363.63	6.371	mV
6) V_{OH} Measurement, V_{CC} = 4.35V, I_{OH} = – 2.5 mA (spec = 2.4)							
V_{OH}	4.25	0.005	4.22	0.000	4.18	0.000	V
7) V_{CC} Program Verify Current V_{PP} = 12.6 V, TTL Level (spec = 15 mA)							
4.35V	8.18	0.275	6.85	0.215	6.03	0.176	mA
4.50V	8.17	0.264	6.86	0.192	6.07	0.173	mA
5.00V	8.16	0.275	6.85	0.184	6.06	0.169	mA
5.50V	8.16	0.299	6.84	0.197	6.05	0.183	mA
5.65V	8.16	0.260	6.82	0.224	6.01	0.165	mA

V_{CC}	–40°C AVG	–40°C STD	25°C AVG	25°C STD	125°C AVG	125°C STD	UNIT
8) V_{CC} Program Verify Current, V_{PP} = 12.6V, CMOS Level (spec = 15 mA)							
4.35V	7.02	0.264	5.96	0.184	5.24	0.129	mA
4.50V	7.01	0.237	5.95	0.182	5.22	0.112	mA
5.00V	7.04	0.254	5.95	0.180	5.25	0.137	mA
5.50V	7.02	0.250	5.95	0.168	5.25	0.108	mA
5.65V	7.01	0.269	5.95	0.181	5.26	0.127	mA
9) V_{CC} Erase Verify Current, V_{PP} = 12.6V, TTL Level (spec = 15 mA)							
4.35V	7.76	0.306	6.70	0.223	6.10	0.184	mA
4.50V	7.76	0.296	6.69	0.238	6.09	0.183	mA
5.00V	7.75	0.294	6.67	0.193	6.07	0.176	mA
5.50V	7.75	0.289	6.69	0.214	6.11	0.164	mA
5.65V	7.76	0.300	6.68	0.230	6.09	0.174	mA
10) V_{CC} Erase Verify Current, VPP = 12.6V, CMOS Level (spec = 15 mA)							
4.35V	6.62	0.241	5.78	0.171	5.29	0.147	mA
4.50V	6.61	0.243	5.79	0.199	5.28	0.140	mA
5.00V	6.63	0.259	5.78	0.186	5.28	0.128	mA
5.50V	6.62	0.260	5.77	0.171	5.31	0.148	mA
5.65V	6.61	0.246	5.79	0.164	5.29	0.149	mA
11) V_{PP} Standby Current, V_{PP} = V_{CC} (spec = 10 µA)							
4.35V	0.00	0.000	0.00	0.000	0.00	0.000	µA
4.50V	0.00	0.000	0.00	0.000	0.00	0.000	µA
5.00V	0.00	0.000	0.00	0.000	0.00	0.000	µA
5.50V	0.00	0.000	0.00	0.000	0.00	0.000	µA
5.65V	0.00	0.000	0.00	0.000	0.00	0.000	µA
12) V_{PP} Standby Current, V_{PP} = 12.6V (spec = 200 µA)							
4.35V	2.50	1.890	2.64	1.506	1.75	0.871	µA
4.50V	2.43	2.058	2.30	1.392	2.32	1.366	µA
5.00V	5.26	1.189	5.61	1.053	6.00	0.376	µA
5.50V	6.13	0.322	6.20	0.000	6.20	0.000	µA
5.65V	6.20	0.000	6.20	0.000	6.20	0.000	µA
13) V_{PP} Active Read Current, V_{PP} = 12.6V, TTL Level (spec = 200 µA)							
4.35V	15.25	1.341	11.16	0.521	8.09	0.445	µA
4.50V	15.53	1.283	11.33	0.455	8.20	0.407	µA
5.00V	16.53	1.369	11.98	0.552	8.63	0.612	µA
5.50V	17.70	1.313	12.81	0.602	9.27	0.518	µA
5.65V	18.15	1.351	13.02	0.596	9.51	0.584	µA

V_{CC}	–40°C AVG	–40°C STD	25°C AVG	25°C STD	125°C AVG	125°C STD	UNIT
14) V_{PP} Active Read Current, V_{PP} = 12.6V, CMOS Level (spec = 200 μA)							
4.35V	15.07	1.317	11.10	0.499	8.17	0.503	mA
4.50V	15.33	1.21	11.22	0.493	8.23	0.406	mA
5.00V	16.50	1.215	11.85	0.454	8.60	0.556	mA
5.50V	17.65	1.334	12.81	0.510	9.21	0.455	mA
5.65V	18.09	1.203	12.99	0.457	9.45	0.592	mA
15) V_{PP} Program Verify Current, TTL Level (spec = 5 mA)							
4.35V	1.86	0.091	1.50	0.056	1.23	0.029	mA
4.50V	1.86	0.091	1.50	0.056	1.23	0.031	mA
5.00V	1.86	0.094	1.50	0.054	1.23	0.031	mA
5.50V	1.86	0.094	1.50	0.055	1.23	0.033	mA
5.65V	1.86	0.094	1.50	0.054	1.23	0.031	mA
16) V_{PP} Program Verify Current, CMOS Level (spec = 5 mA)							
4.35V	1.87	0.093	1.50	0.054	1.24	0.035	mA
4.50V	1.87	0.093	1.50	0.054	1.24	0.034	mA
5.00V	1.86	0.094	1.50	0.054	1.24	0.034	mA
5.50V	1.87	0.093	1.50	0.054	1.23	0.033	mA
5.65V	1.87	0.093	1.50	0.054	1.23	0.033	mA
17) V_{PP} Erase Verify Current, TTL Level (spec = 5 mA)							
4.35V	1.69	0.071	1.40	0.48	1.14	0.038	mA
4.50V	1.69	0.070	1.40	0.48	1.14	0.036	mA
5.00V	1.69	0.070	1.39	0.49	1.14	0.036	mA
5.50V	1.69	0.068	1.39	0.49	1.14	0.038	mA
5.65V	1.69	0.070	1.40	0.48	1.14	0.038	mA
18) V_{PP} Erase Verify Current, CMOS Level (spec = 5 mA)							
4.35V	1.69	0.070	1.40	0.048	1.14	0.038	V
4.50V	1.69	0.068	1.40	0.048	1.15	0.039	V
5.00V	1.69	0.068	1.40	0.048	1.14	0.038	V
5.50V	1.69	0.070	1.40	0.048	1.14	0.038	V
5.65V	1.69	0.067	1.40	0.048	1.14	0.038	V
19) V_{CCMAX}, 120 ns Compare Strobe (spec = 5.50V)							
	8.03	0.377	8.00	0.359	8.03	0.360	V
20) V_{CCMIN}, 120 ns Compare Strobe (spec = 4.50V)							
4.35V	3.60	0.137	3.73	0.143	3.35	0.063	V

V_{CC}	–40°C AVG	–40°C STD	25°C AVG	25°C STD	125°C AVG	125°C STD	UNIT
21) V_{IL} Input Low Voltage (spec = 0.80V)							
4.35V	1.25	0.006	1.21	0.006	1.14	0.007	V
4.50V	1.31	0.008	1.24	0.007	1.17	0.010	V
5.00V	1.38	0.011	1.31	0.007	1.25	0.010	V
5.50V	1.43	0.015	1.39	0.006	1.32	0.011	V
5.65V	1.44	0.014	1.41	0.008	1.34	0.011	V
22) V_{IH} Input High Voltage (spec = 2.00V)							
4.35V	1.43	0.009	1.35	0.008	1.28	0.012	V
4.50V	1.46	0.009	1.38	0.009	1.30	0.013	V
5.00V	1.54	0.008	1.47	0.011	1.40	0.009	V
5.50V	1.62	0.010	1.56	0.010	1.50	0.009	V
5.65V	1.65	0.010	1.59	0.010	1.53	0.008	V
23) t_{AC} Access Time (spec = 120 ns)							
4.35V	54.73	2.011	63.00	2.280	77.53	2.446	ns
4.50V	53.87	1.899	62.00	2.117	75.60	2.372	ns
5.00V	51.53	1.775	58.69	2.112	72.07	2.132	ns
5.50V	49.60	1.841	56.54	2.005	69.60	2.253	ns
5.65V	49.13	1.788	56.23	1.986	69.13	2.080	ns
24) t_{CE} Access Time (spec = 120 ns)							
4.35V	51.97	1.574	59.85	1.994	72.70	2.830	ns
4.50V	50.33	1.709	57.77	2.122	70.47	2.529	ns
5.00V	46.63	1.567	53.77	1.728	65.40	2.207	ns
5.50V	44.20	1.260	50.73	1.710	61.70	2.037	ns
5.65V	43.63	1.521	49.96	1.843	60.87	2.161	ns
25) t_{OE} Access Time (spec = 50 ns)							
4.35V	15.20	0.378	19.58	0.504	24.50	0.630	ns
4.50V	14.63	0.493	18.38	0.496	22.50	0.731	ns
5.00V	11.13	0.402	14.88	0.326	18.73	0.583	ns
5.50V	9.03	0.182	12.31	0.679	15.33	0.479	ns
5.65V	9.00	0.000	11.27	0.452	15.00	0.000	ns
26) $t_{dis(G)}$ Hold Time, Output Enable (spec = 30 ns)							
4.35V	18.83	0.405	28.88	0.326	19.90	0.481	ns
4.50V	18.63	0.485	19.00	0.400	19.80	0.484	ns
5.00V	18.37	0.463	18.85	0.368	19.70	0.466	ns
5.50V	18.43	0.493	18.96	0.344	20.00	0.587	ns
5.65V	18.50	0.497	19.38	0.496	20.17	0.592	ns

V_{CC}	AVG	STD	AVG	STD	AVG	STD	UNIT
27) $t_{dis(E)}$ Chip Disable Time (spec = 55 ns)							
4.35V	19.67	0.663	20.81	0.402	22.90	0.607	ns
4.50V	19.30	0.583	20.58	0.578	22.63	0.615	ns
5.00V	18.57	0.674	19.81	0.402	21.90	0.712	ns
5.50V	18.17	0.756	19.58	0.643	21.67	0.547	ns
5.65V	18.20	0.785	19.58	0.578	21.73	0.640	ns
28) $t_{h(A)}$ Address Hold Time with CE Controlled Writes (spec = 75 ns)							
4.35V	26.43	0.000	34.15	0.675	45.87	0.730	ns
4.50V	25.43	0.000	32.54	0.647	44.03	0.765	ns
5.00V	22.80	0.182	28.77	0.514	38.77	0.679	ns
5.50V	20.67	0.253	26.31	0.549	34.87	0.507	ns
5.65V	20.07	0.475	25.62	0.496	33.87	0.681	ns
29) $t_{h(A)}$ Address Hold time with WE Controlled Writes (spec = 55 ns)							
4.35V	22.83	0.663	29.92	0.392	40.50	0.731	ns
4.50V	21.97	0.583	28.81	0.402	38.87	0.571	ns
5.00V	19.50	0.674	25.77	0.430	34.17	0.592	ns
5.50V	17.73	0.756	23.38	0.496	30.77	0.568	ns
5.65V	17.17	0.785	22.85	0.368	29.93	0.521	ns
30) $t_{su(D)}$ DATA Set-up Time with CE Controlled Writes (spec = 50 ns)							
4.35V	5.00	0.000	6.73	0.452	9.00	0.000	ns
4.50V	5.00	0.000	6.00	0.000	8.57	0.504	ns
5.00V	4.03	0.182	5.42	0.504	7.50	0.509	ns
5.50V	3.97	0.253	5.00	0.000	6.93	0.254	ns
5.65V	3.33	0.475	5.00	0.000	6.30	0.466	ns
31) $t_{su(D)}$ DATA Set-up Time with WE Controlled Writes (spec = 50 ns)							
4.35V	5.00	0.000	6.62	0.496	9.00	0.000	ns
4.50V	5.00	0.000	6.00	0.000	8.33	0.479	ns
5.00V	4.03	0.182	5.46	0.508	7.50	0.509	ns
5.50V	3.87	0.378	5.00	0.000	6.97	0.183	ns
5.65V	3.30	0.463	5.00	0.000	6.37	0.490	ns

Chapter 6

Circuit Data

6.1 TMS28F512A Address Decode

The TMS28F512A is organized as 64K bits × 8.

- **Columns**
  - There are 8 outputs. Each output has 8 sticks. Addresses 10, 14, and 15 decode the sticks.
  - Each stick has 16 columns. Addresses 0, 1, 2, and 3 decode the columns.
- **Rows**
  - There are 512 rows.
  - Addresses 4 through 9, and 11 through 13 decode the rows.

Figure 6-1 on page 6-3 shows the TMS28F512A bitmap.

Table 6-1. Row × Decode (1 of 512 Wordlines)

A13	A12	A11	A09	A08	A07	A06	A05	A04	Select	
0	0	0	0	0	0	0	0	0	WL (0)	Top
0	0	0	0	0	0	0	0	1	WL (1)	
0	0	0	0	0	0	0	1	0	WL (2)	
0	0	0	0	0	0	0	1	1	WL (3)	
0	0	0	0	0	0	1	0	0	WL (4)	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	1	1	1	1	1	1	1	0	WL (510)	
1	1	1	1	1	1	1	1	1	WL (511)	Bottom

Table 6-2. Y Decode (1 of 16 Bitlines)

A03	A02	A01	A00	Select
0	0	0	0	BL (0)
0	0	0	1	BL (1)
0	0	1	0	BL (2)
0	0	1	1	BL (3)
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	1	0	BL (14)
1	1	1	1	BL (15)

Table 6-3. Z Decode (1 of 8 Sticks)

A15	A14	A10	Select
0	0	0	Z (0)
0	0	1	Z (1)
0	1	0	Z (2)
0	1	1	Z (3)
.	.	.	.
.	.	.	.
.	.	.	.
1	1	0	Z (6)
1	1	1	Z (7)

Figure 6-1. TMS28F512A Array Organization

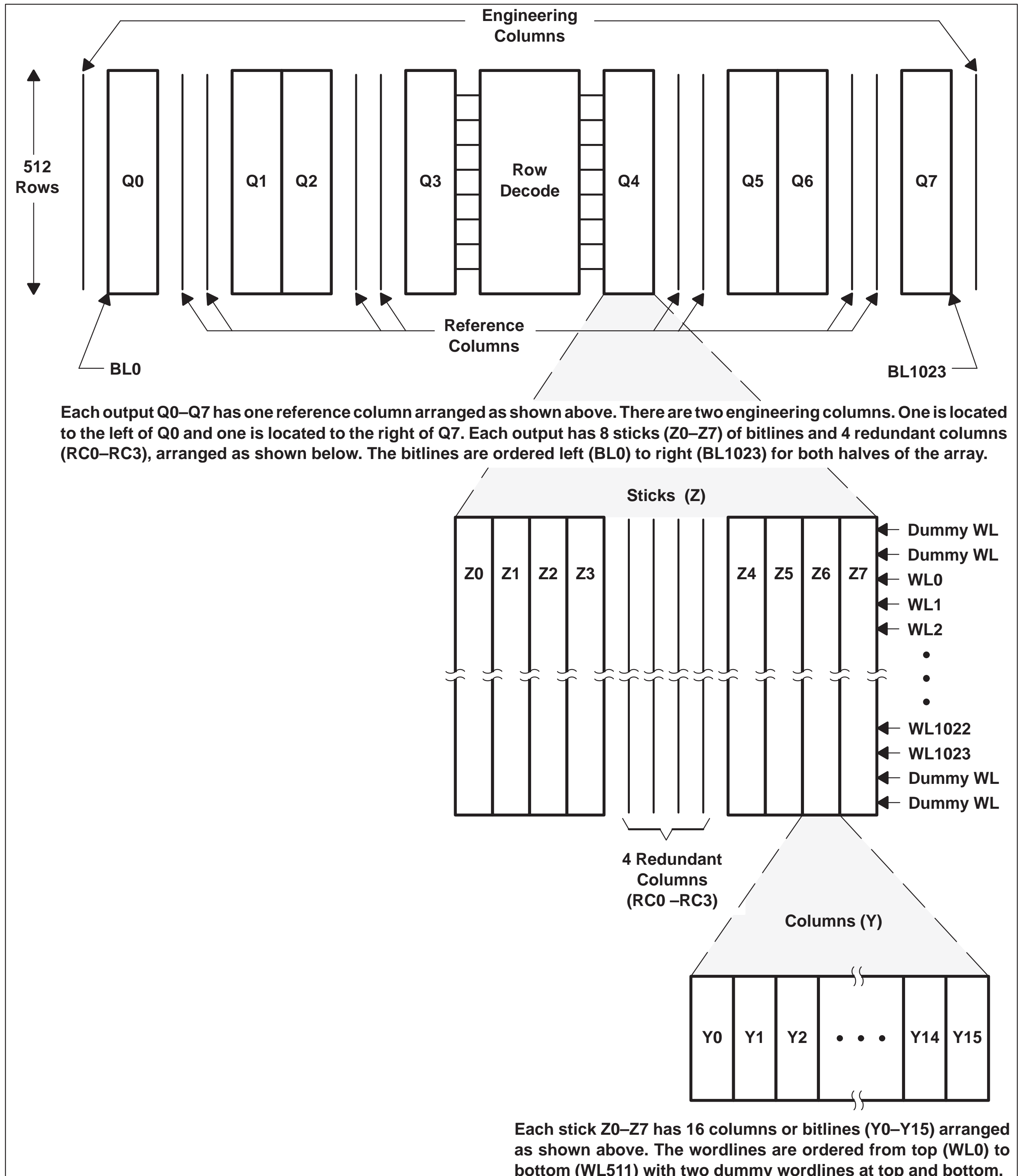


Figure 6-2. TMS28F512A Logic Diagram

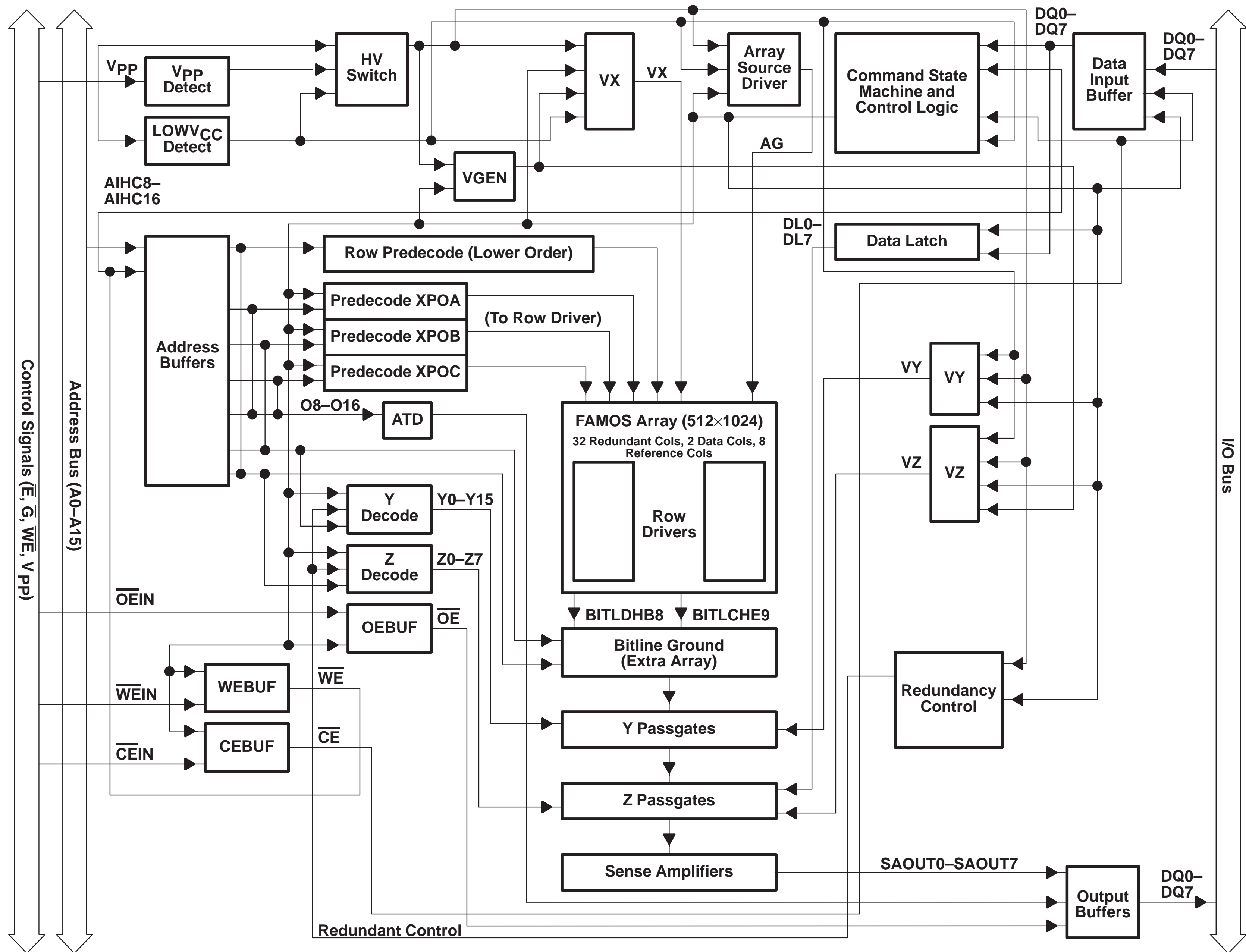


Figure 6-4. TMS28F512A Input ESD Protection

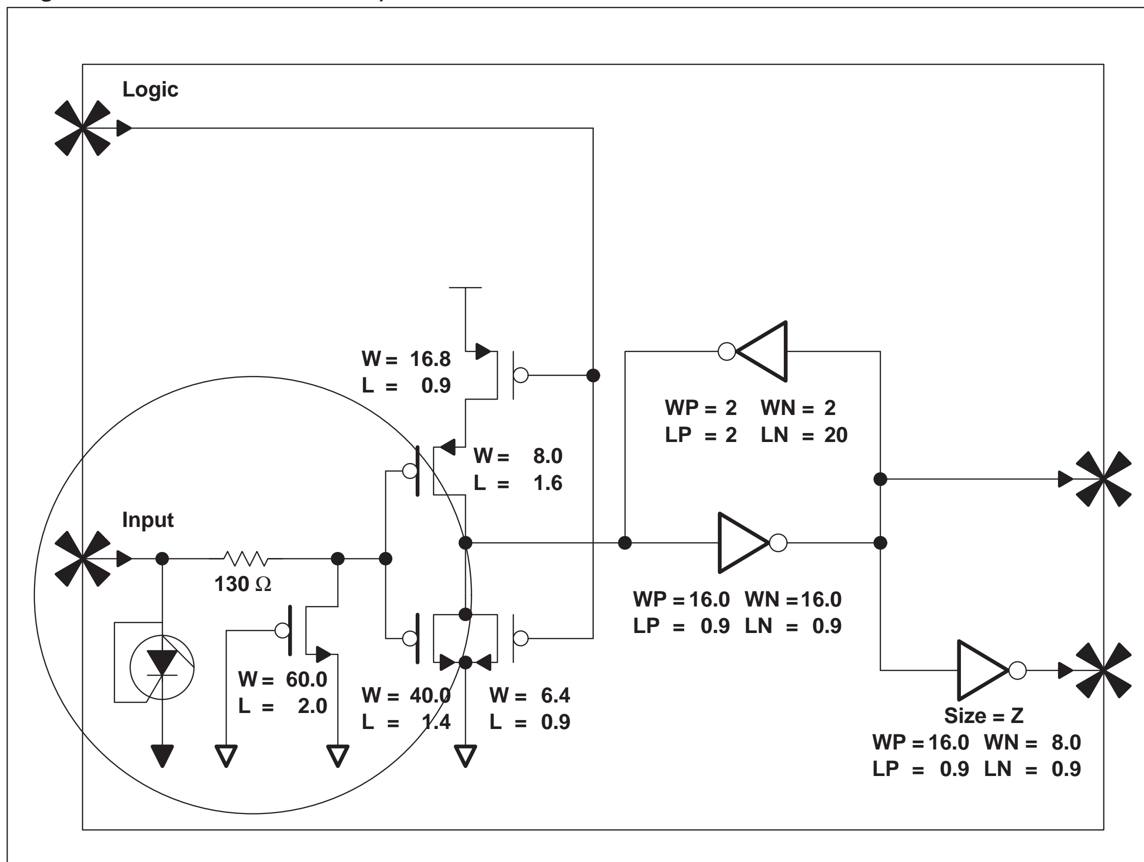
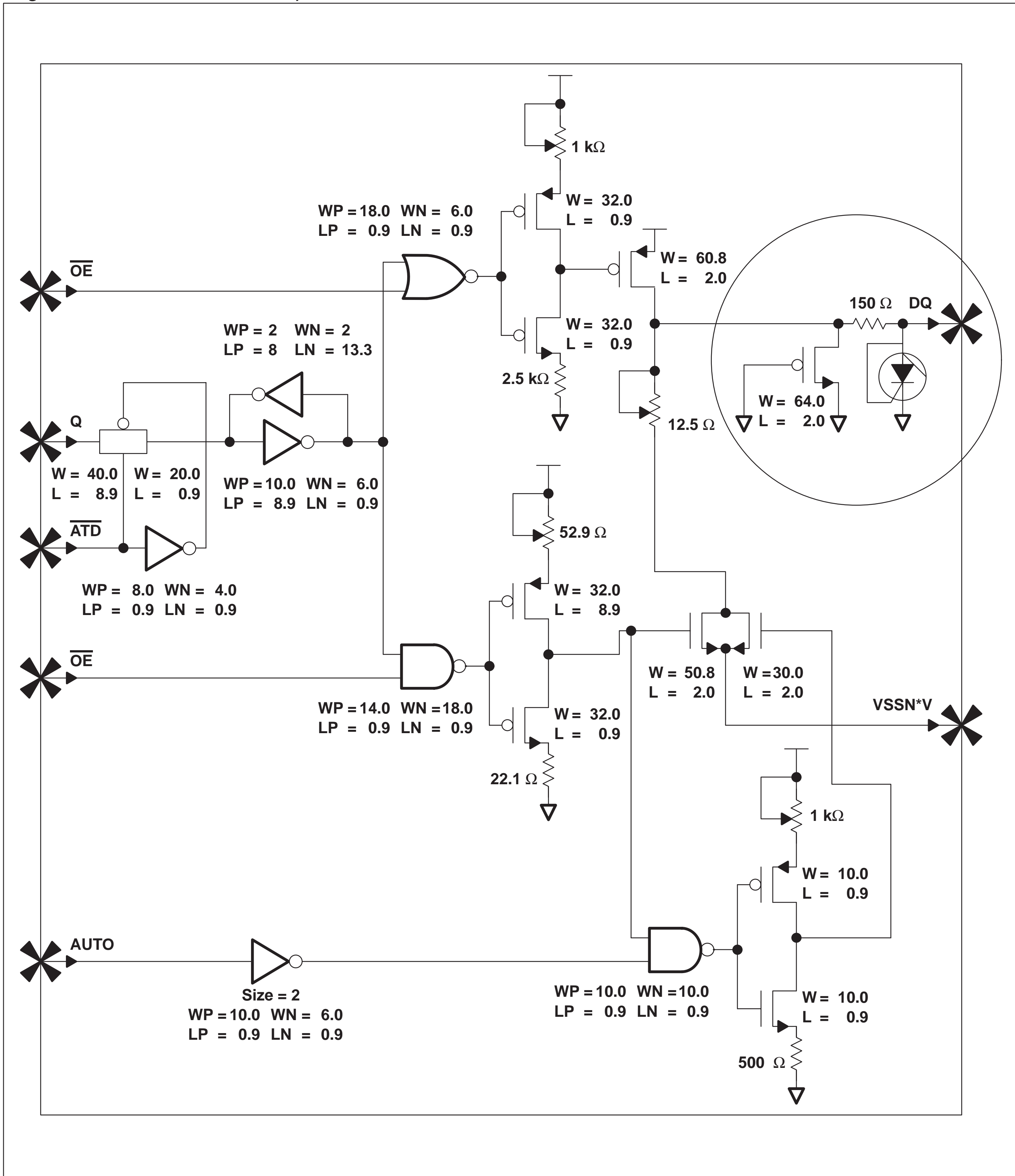


Figure 6-5. TMS28F512A Output ESD Protection



Chapter 7

Flash Memory Programmer Support

By June 1993, Texas Instruments notified the following EPROM programmer vendors of the new 1-megabit Flash memory device. All necessary programming information was provided to each vendor.

Supporting TMS28F512A	Vendor	Parallel Erase
Now	Advin Systems	Y
Now	B & C Microsystems, Inc.	Y
Now	BP Microsystems	N
Now	Bytek Corporation	Y
Now	Computer Service Tech.	N
Now	Data I/O	Y
November1993	Elan Digital Systems	Y
Now	International Micro Systems	Y
Now	GTEK	Y
November 1993, wk4	Logical Devices	Y
March 1994	Minato	model 1930 only
Now	Red Square	N
Now	Stag	Y
Now	Sunrise Electronics	Y
Now	System General	Y
December 1993	UEC-Promac	Y
Now	XELTEC	N