DAC0800

AN-597 Current Feedback Amplifiers

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Current Feedback Amplifiers

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Hans Palouda
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CURRENT FEEDBACK AMPLIFIERS

This application note will discuss the LH4117, LH4118, and LH4200 amplifiers, their properties, and the current feedback principles involved.

Current feedback amplifiers offer advantages over conventional operational amplifiers, but there are important differences which have to be taken into account. To understand why and how a current feedback amplifier works it is helpful to start with a conventional amplifier.

CONVENTIONAL vs CURRENT FEEDBACK AMPLIFIERS

Conventional Amplifiers

The conventional op-amp has three stages: an input stage configured as a differential amplifier, a gain stage, and an output stage *(Figure 1)*. The diff-amp provides two symmetrical inputs. The open loop gain is independent of the set gain and we have the situation of the gain-bandwith product being constant. This means when the op-amp is set for higher gains the rolloff starts at a lower frequency *(Figure 4)*.

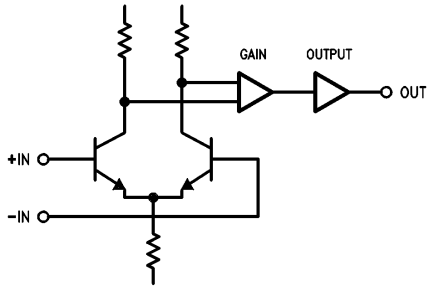

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FIGURE 1. Conventional Amplifier

Current Feedback Amplifiers.

Topology

The current feedback amplifier *(Figure 2)* has an input stage configured as an emitter follower (or source follower for a FET input). This makes for an inherently faster response, because the input stage runs at unity voltage gain and therefore has less Miller capacitance.

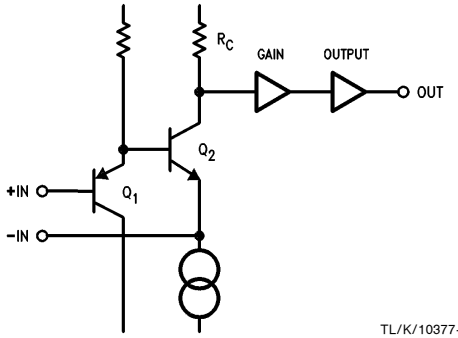

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FIGURE 2. Current Feedback Amplifier

The inverting input feeds into the emitter of the second stage. This is a low impedance node, and the feedback function is accomplished by injecting current into the emitter. This current then flows through the collector resistor and produces a voltage proportional to the injected current.

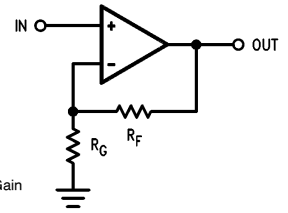
The feedback does not reach around the very first stage. This stage operates as an open loop buffer with a voltage gain close to one.

Gain

Current feedback amplifiers are optimized for speed and have comparatively low open loop gain. Therefore most of them have a recommended gain range.

The basic equations for the gain are the same as for a conventional operational amplifier (see *Figure 3*):

Inverting gain $A_V = -R_F/R_G$,
Non-inverting gain $A_V = R_F/R_G + 1$



Non-Inverting Gain

$$A_V = 1 + \frac{R_F}{R_G}$$

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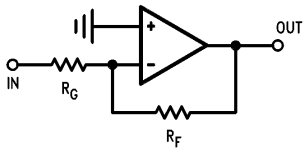

Inverting Gain

$$A_V = -\frac{R_F}{R_G}$$

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FIGURE 3. Setting the Gain for Current Feedback Amplifier

The non-inverting gain of the second stage is determined by the ratio of collector resistor R_C over the emitter resistance. The emitter resistance is determined by the paralleling of three resistors (*Figure 2* and *Figure 3*): the feedback resistor R_F, the gainsetting resistor R_G and the resistance of the current source, which, at frequencies below the rolloff, is high compared to R_F and R_G and can be neglected.

If R_F is held constant, R_G becomes smaller as the amplifier is set for higher gains. Thus the node resistance in the emitter is decreased and the gain of the stage increased, and with it the open loop gain. This higher A_{OL} is the reason why the bandwidth of current mode amplifiers is almost independent of the set gain A_V *(Figure 4)*.

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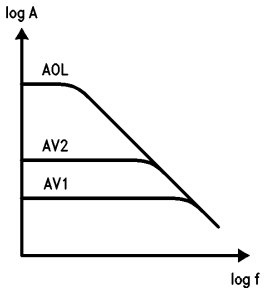
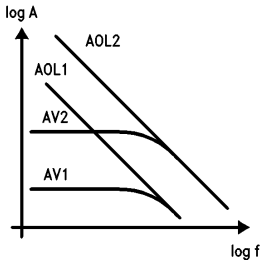


Conventional TL/K/10377–5



Current Feedback TL/K/10377–6

FIGURE 4. Gain Characteristics of Conventional vs Current Feedback Amplifiers

The inverting input of a current mode amplifier is inherently sensitive to capacitance. The reason is that at higher frequencies the gain of the stage is increased and at this high gain the amplifier tends to become unstable. Peaking the amplifier with a small capacitor from the inverting input to ground will work, since the increase in gain is held small. However, a capacitor across the feedback resistor to reduce peaking will almost always result in instabilities, because it increases the gain of the stage and in addition affects the phase margin.

Equations for Voltage Gain

The connection between gain and bandwidth can be shown in the basic equations as well.

For the conventional amplifier the voltage gain is determined by

$$1/A_V = (1/A_{OL}) + (1/G), \qquad \text{(eq. 1)}$$

with the non-inverting gain set to

$$G = (R_F/R_G) + 1 \qquad \text{(eq. 2)}$$

Equation 1 is written in reciprocal values because this makes the interrelations between the parameters easier to understand. For low G the term 1/G dominates and A_V becomes approximately equal to G and independent of frequency until at higher frequencies A_{OL} drops drastically. For higher G this crossover from a frequency independent characteristic following G to a rolloff characteristic following A_{OL} occurs at lower frequency. Therefore: the higher the set gain G the lower the bandwidth.

For the current feedback amplifier (see *Figure 2* and *3*) the open loop gain can be set to

$$A_{OL} = \left(\frac{Rc}{R_G \times R_F/(R_G + R_F)}\right) \times A1 \qquad \text{(eq. 3)}$$

The first factor describes the gain of the feedback stage and A1 the open loop gain of the stages following it. Equation 3 substituted into eq. 1 becomes

$$\frac{1}{A_V} = \frac{1}{G}\left(\frac{R_F}{Rc \times A1} + 1\right) \qquad \text{(eq. 4)}$$

Equation 4 consists of two factors. The first one, 1/G, is independent of frequency, the second one is independent of gain. This shows that the pole structure and the rolloff characteristic of the second factor, which includes A1, are preserved independent of G. The factor 1/G only scales the gain characteristic. This shows that the bandwidth becomes independent of the set gain G, because bandwidth is defined as the frequency at which the gain drops by 3 dB, no matter how large the gain is.

Gainsetting Resistors

As in conventional op-amps the gain is set by R_F and R_G *(Figure 3),* but with the provision that the resistor values be right for the amplifier. This is necessary because the gain of the feedback stage is set by the impedance on the inverting input. Normally a value of R_F is recommended for any given amplifier and very often R_F is built in.

Over-Compensation

To over-compensate means to reduce the bandwidth. One reason why this is done is to reduce excessive peaking and associated ringing when pulses are amplified. On a current feedback amplifier this reduction of bandwidth can be accomplished by increasing R_F. For a given voltage gain this increases R_G as well and the inverting input sees a higher impedance. This reduces the open loop gain (see section on Gain), and with it A_{OL} and the bandwidth.

In amplifiers where inverting input and output are internally connected through R_F this method cannot be used. Here it will be necessary to use an external filter to reduce the bandwidth.

Excessive Peaking

When the set gain G is low, on some current mode amplifiers the gain vs. frequency curve tends to peak at high frequencies. This is especially prevalent in current mode amplifiers which are optimized for high gains.

The reason for this is as follows: For lower gains the gain setting resistor R_G is larger and at some frequency the stray capacitance of the inverting input node, in parallel with R_G, becomes dominant and increases the gain of the amplifier. When R_G is low, as it is for high gain settings, this crossover frequency becomes so high that it falls outside the amplifier's frequency range and therefore is of no consequence.

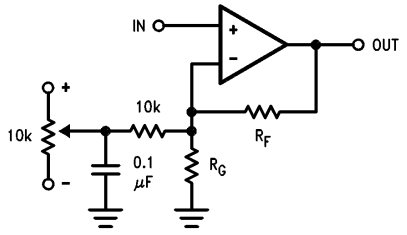
Reducing the bandwidth slightly by increasing the value of R_F (see section on ''Reducing the Bandwidth'') will reduce the peaking. An R-C filter in the non-inverting input will compensate the peaking with rolloff and thereby also reduce peaking, but it will reduce the ringing associated with the peaking response only to a degree, because the frequency rolloff is outside the feedback loop.

Offset Voltages

For a DC coupled current mode amplifier there are two offset voltages. One is the output offset: it is the input voltage required on the non-inverting input to make the output 0V. This offset voltage varies for different gain settings G. The other offset is the input offset, which is the voltage between inverting and non-inverting input. It, too, is dependent on the gain setting.

To adjust the input-to-output offset to zero, a current can be injected into the inverting input *(Figure 5a),* or a voltage can be added to the non-inverting input *(Figure 5b).*

The method of adding a voltage to the non-inverting input can also be used to zero the offset voltage between the inputs, while injecting a current into the inverting input will not accomplish this well. The reason is that the input offset is the difference in voltage drop of two base-emitter diodes (transistors Q1 and Q2 in *Figure 2*). Because of the exponential characteristic, a large percentage change in current is needed to shift a diode-drop to the required value.



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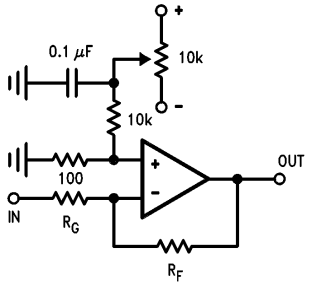
a) Non-Inverting Amplifier



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b) Inverting Amplifier

FIGURE 5. Adjusting Offset Voltage

Capacitive Loads

Care has to be taken when driving capacitive loads. Since the current feedback amplifiers have a wide bandwidth, even small capacitors of 200 pF or less need attention.

One limitation is the charge current, which the amplifier has to supply:

$$I = C \times dV/dt$$

Usually more stringent is the question of stability. The capacitor shifts the phase because the output voltage lags the output current and the phase margin of the amplifier deteriorates because the phase angle of the amplifier was negative to start with.

Very small capacitors (e.g., 10 pF) have significant phase shift only at high frequencies beyond the amplifier's rolloff and therefore do not cause problems. Larger capacitances can be paralleled with a resistive load to improve the phase angle of the load. For large capacitive loads a series resistor is recommended (about 10Ω to 50Ω). The amplifier will be stable, but the frequency response will be slower.

LH4117

The LH4117 is a current feedback amplifier with a FET input. It is optimized for gains from 5 to 50. It has typically 150 MHz bandwidth, 6000 V/μs slew rate, and 9 ns settling time to 0.2% (typical values).

The LH4117 *(Figure 6)* has a FET input stage with Q1 working as a source follower and another FET providing bias and V_{OS} drift compensation (Q2). The rest of the stages are symmetrical. Two stages of emitter followers (Q3–Q6) amplify current with close to unity voltage gain. The emitters of the complementary pair Q5 and Q6 are the node for the inverting input. The feedback network injects current into this node. A feedback resistor R_F of 1500Ω is built into the device. Q7 and Q8 form the gain stage, which is followed by a push-pull emitter follower output pair.

Using the LH4117 as a Transimpedance Amplifier for DAC Outputs

The LH4117 is an excellent match to amplify the output of DACs like the DAC0800. The fast settling time of 9 ns to 0.02% does not degrade the performance of the DAC. On the other hand, the DAC0800 provides complimentary current outputs, which are current sinks and do not need a fixed voltage (like virtual ground) to work accurately.

Figure 7 shows one of several possible ways to connect the DAC to the LH4117. It transforms the 8 logic input signals to a 256 step analog signal ranging from −3V for all bits LOW to +3V for all bits HIGH.

Operation

The DAC0800 is fed a reference current of $I_{REF} = 2$ mA into pin 14 *(Figure 7)*. This is achieved by the LH0070 voltage reference with 10V output. A resistance of 5 kΩ (R1 + R2) is connected to pin 14, which is a virtual ground, thus providing the reference current of 2 mA. The grounded pin 15 provides the reference voltage for pin 14 (for details see the DAC0800 datasheet).

The DAC has eight current sinks, each set for half the current of the previous one. Through switches, controlled by the input logic levels, their open collectors are connected to one of the two outputs. The sum of the output currents I1 and I2 equals the reference current of 2 mA. Because of the open collector configuration the outputs do not have to be tied to a fixed voltage level.

The outputs of the DAC0800 are connected to the inputs of the LH4117 through 100Ω resistors (R4 and R5). This is to decouple the inputs of the amplifier from the output capacitance of the DAC, which is typically 23 pF to 30 pF. Especially the inverting input is sensitive to capacitance. The gain of the input stage is set by the impedance of the node, and at high frequencies the capacitor has low impedance,

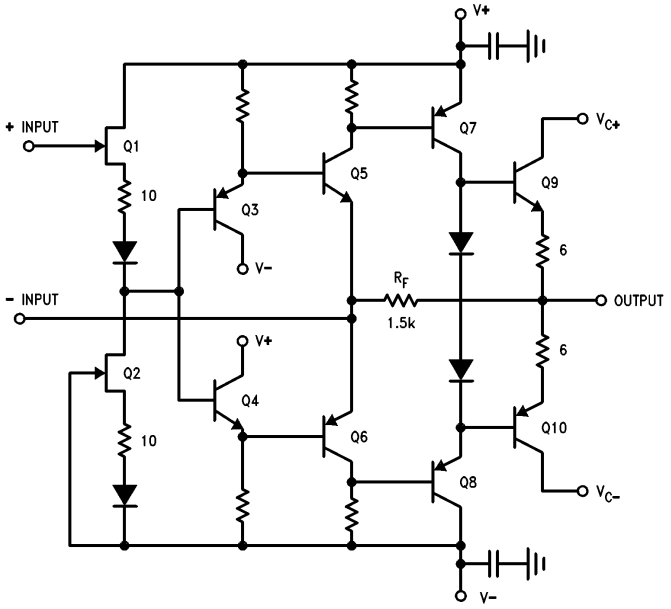

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FIGURE 6. Simplified Schematic of the LH4117

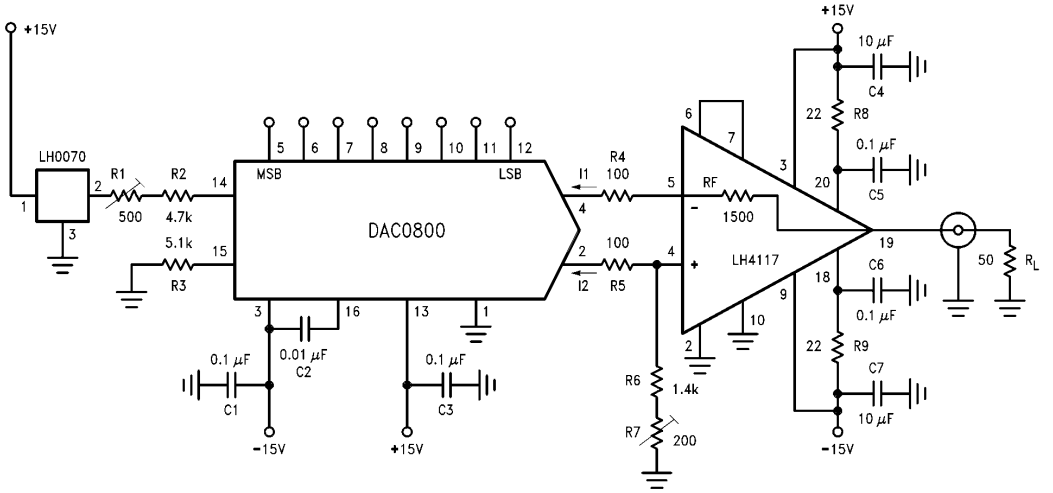

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FIGURE 7. Fast Current-to-Voltage Current Mode DAC Amplifier

thereby increasing the gain of the stage. The LH4117 is not compensated for such high gain, and therefore tends to become unstable.

The output voltage of the LH4117 is derived in the following way: The DAC's output current I1 also flows through the feedback resistor R_F of 1500Ω, which is built into the LH4117, driving the output of the amplifier high in relation to the inverting input. The non-inverting input, pin 4, is driven low by the voltage drop which is generated by the current I2 flowing through R6 + R7 = 1500Ω. Since the amplifier causes inverting and non-inverting input to have the same voltage, the voltage at its pin 4 is added to the output:

$$V_{OUT} = I1 \times R_F - I2 \times (R6 + R7).$$

With

$$I1 + I2 = I_{REF}$$

and

$$R6 + R7 = R_F$$

this can be written as

$$V_{OUT} = 2 \times R_F \times I1 - I_{REF} \times R_F$$

With I_{REF} = 2 mA and R_F = 1500Ω, it can be seen that for I1 = 0 the output is −3V (all logic inputs LOW), and for I1 = 2 mA the output is +3V (all logic inputs HIGH).

Trimming

Due to inaccuracies of resistors and offset voltage in the amplifier the circuit will need trimming. This is accomplished by setting the maximum output voltage to +3V (logic inputs HIGH), and the minimum output voltage to −3V (logic inputs LOW).

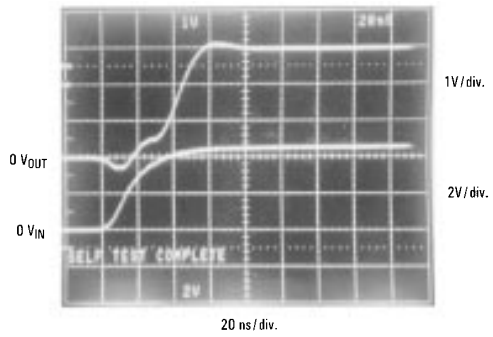
R1 will change the reference current I_{REF} and with it both extremes of the output voltage. The resistor R7 will influence only the negative extreme.

The trim procedure is to set all logic inputs HIGH and trim R1 until the output voltage is +3V, then set all inputs LOW and trim R7 until V_{OUT} = −3V.

Results

After trim the linearity was tested and shown to be within ±10 mV from the ideal value. This corresponds to 0.17% of full scale or less than ½ LSB.

Settling time is below 135 ns. The settling time of the LH4117 is 9 ns and does not contribute noticeably to the total settling time. *Figure 8* shows the output waveform when the MSB is switched.



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Lower Curve: Logic Input

Upper Curve: Analog Output

The MSB is switched.

FIGURE 8. Pulse Response of the DAC0800-LH4117 Combination

LH4118

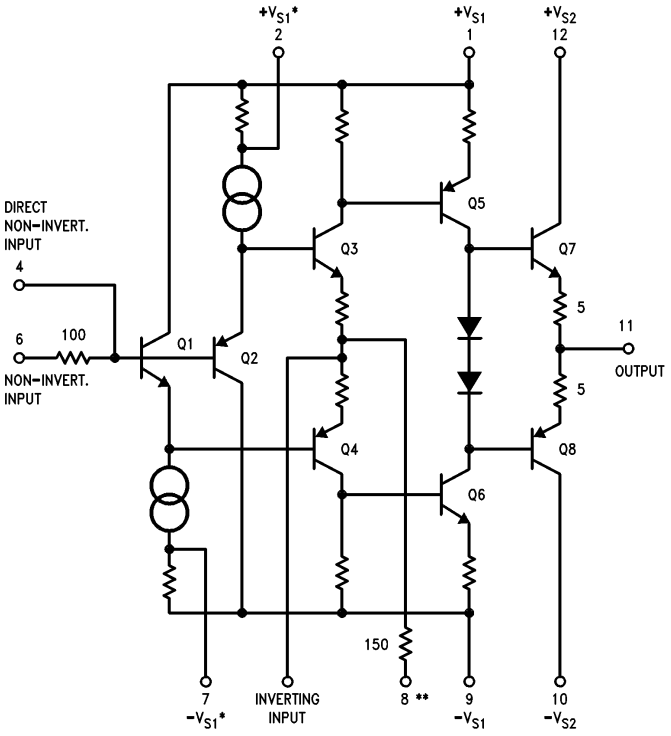
The LH4118 is a current feedback amplifier optimized for gains from 1 to 9. It has bandwidth of over 200 MHz, good noise characteristics (typical 1.3 nV/V Hz) and 125 mA output current capability.

The topology of the LH4118 is close to what has been discussed for current feedback amplifiers, except that the device is symmetrical throughout *(Figure 9)*. The input has an NPN and a PNP transistor which feed their emitter currents into a push-pull feedback stage. Gain and output stages are in push-pull configuration as well. The input has a small series resistor which helps the stability of the amplifier making sure that the real part of the input impedance is always positive. The direct non-inverting input is fed out as well. It can be used to limit the bandwidth of the amplifier by connecting a small capacitor to ground.

Fiber Optic Receiver Using the LH4118

Figure 10 shows the LH4118 as a photo diode receiver. The pin diode is excited by the incoming light (*Figure 11* shows the optical transmitter which was used in the test setup). The current generated in the PIN diode causes a voltage drop across resistor R1. This voltage is then amplified by the LH4118.

It is important to hold the capacitance at the input small. This capacitance consists of the diode, amplifier input and wiring capacitance. Together with the load resistor R1 it determines the frequency rolloff at the input. This is also the reason for choosing a small value for R1.



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*Pins 2 and 7 can also be left disconnected (floating).

**The built-in 150Ω can be used as feedback resistor for $A_V = 1$.

FIGURE 9. LH4118 Simplified Schematic

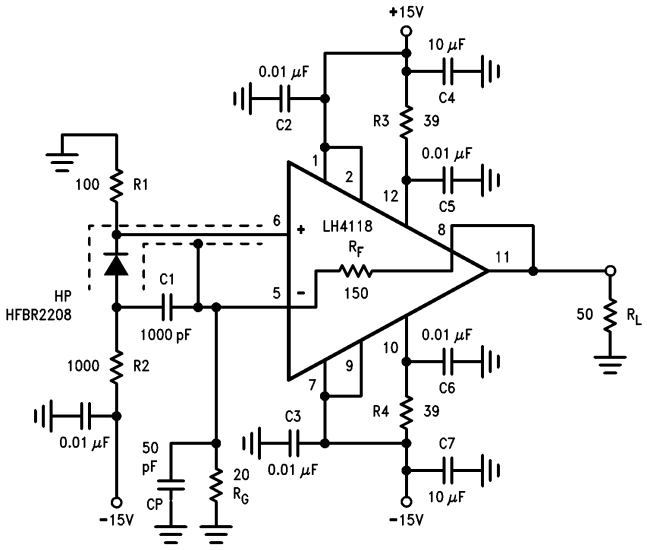

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FIGURE 10. Fiber Optic Receiver Using the LH4118

A guard around the input node driven from the feedback point helps to reduce the input capacitance. If the PIN diode has a metal case it should also be connected to the driven guard. If this constitutes too much capacitance for the inverting input and therefore causes the gain characteristic to peak, a separate voltage divider from the output can be used to drive the shield.

For the same reason the anode of the PIN diode (Hewlett Packard HFBR2208) is connected to the inverting input. This connection is made through a 1000 pF capacitor C1 because of the different DC potentials.

The resistor R2 is needed to decouple the bias supply from the inverting input. For high frequencies it is parallel with the input and therefore needs to be high compared to R_G.

The gain of the amplifier is set to $A_V = 8.5$, with R_F the recommended value of 150Ω. Because the amplitudes are small, the built-in resistor was utilized. $R_G = 20\Omega$, with a peaking capacitor of $C_P = 50$ pF in parallel.

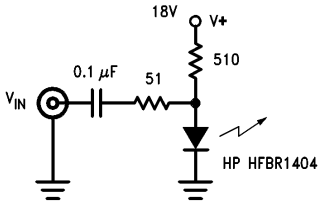

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FIGURE 11. Simple Optical Transmitter Used for the Evaluation of the Optical Receiver

Normally, the LH4118 does not need a peaking capacitor. In this case the peaking capacitor is used to extend the bandwidth of the PIN diode-amplifier combination *(Figure 11).* Although the gain of this combination is flat, the gain of the feedback amplifier itself is slightly peaked, and therefore some ringing occurs in the pulse response (*Figure 13* and *14*). This ringing can be alleviated by reducing the peaking capacitor C_P, but as a tradeoff the bandwidth is lowered.

The power gain of the receiver can be written as

$$P_G = 10 \log \frac{(R_P \times R1 \times A_V)^2}{R_L}, \text{ with}$$

R_P—responsitivity of the PIN diode, typically 0.384 A/W,
R1—the diode's series resistor, 100Ω
A_V—non inverting voltage gain of the amplifier, 8.5
R_L—output load of the amplifier, 50Ω

With the above values the expected power gain becomes 33.3 dB. This is well in keeping with the actually measured values (see *Figure 12*).

Figure 13 shows input and output signal for a 20 MHz squarewave, and *Figure 14* shows the same for a 100 MHz squarewave.

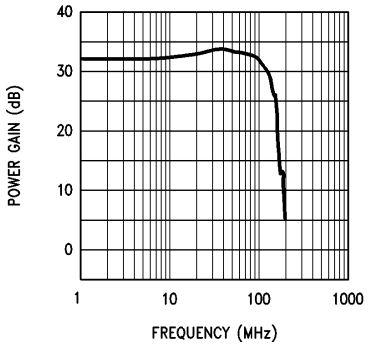

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FIGURE 12. Gain (Output Power/Input Power) of the Fiber Optic Receiver

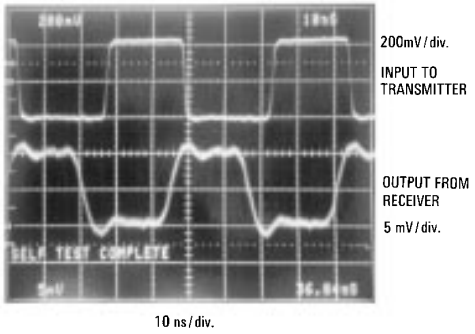

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FIGURE 13. Pulse Response of the Opto Receiver Utilizing the LH4118 for a 20 MHz Squarewave

Like with all high frequency circuits, care has to be taken with proper layout. Lead lengths should be short, a copper clad PC board needs to provide a ground plane, the power supplies should be bypassed with 0.01 μF (C2, C3, C5, C6) no more than ⅜ inch from the pins.

R3 and R4 protect the output from momentary overload. In this application this is not critical, but it is good practice since it is easy and does not affect the performance.

LH4200

The LH4200 is a current feedback amplifier with an operating range from about 1 MHz to 1 GHz. Its input is a dual gate GaAs-FET and it uses a single 10V supply. It is therefore especially useful in video and R_F applications. It has a low noise figure of 3 dB at 50Ω source resistance and can supply 40 mA. Power supply bypass capacitors are built into the device.

Figure 15 shows the schematic of the LH4200. The first stage is constructed with a dual gate GaAs-FET. Therefore caution has to be exercised with electrostatic discharge (ESD).

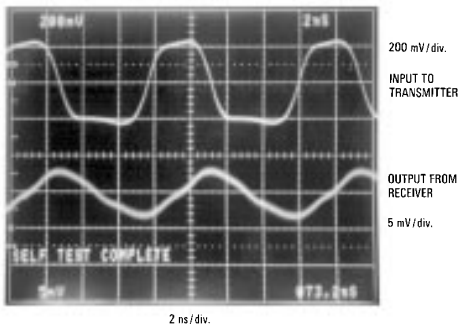

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FIGURE 14. Pulse Response of the Opto Receiver Utilizing the LH4118 for a 100 MHz Squarewave

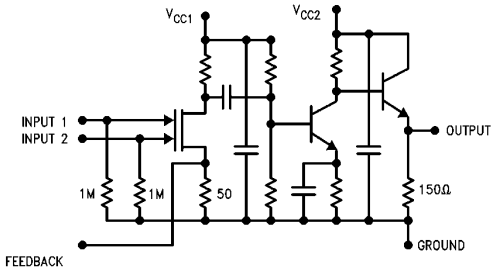

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FIGURE 15. LH4200 Simplified Schematic

The first stage differs from other current mode amplifiers in that the insulating input buffer is missing. The GaAs-FET has voltage gain and therefore Miller capacitance, but it is an inherently fast device with very low gate capacitances. The input impedance is best expressed in S-parameters *(Figure 16)*.

Frequency	S11		S21		S12	S22	
MHz	Mag	Ang	dB	Ang	dB	Mag	Ang
10	0.96	−0.5	50	−49	−48	0.99	181
100	0.97	−15	36	−130	−45	0.93	152
250	0.86	−32	26	150	−43	0.93	115
500	0.64	−62	18	39	−40	0.82	73
750	0.41	−105	10	70	−33	0.7	52
1000	0.23	168	3.5	−160	−37	0.71	42

FIGURE 16. Typical S-Parameters for the LH4200 $V_{CC1} = V_{CC2} = 10V$, $V_{INPUT2} = 1.5V$

Both gates are non-inverting inputs and are internally biased to ground. Input 1 is intended for the signal. Input 2 sets the gain and needs to be biased to approximately +1V for optimal gain and bandwidth. It can also be used to regulate the gain of the amplifier in AGC applications. It needs to be bypassed with 0.01 μF close to the pin. The voltage range on gate 1 is from −4V to +1.4V, on gate 2 from −4V to +2.5V.

The inverting input is connected to the source of the GaAs-FET. The source load resistor is 50Ω and is fixed. This is also the gain setting resistor. In using a fixed R_G the LH4200 differs from most current feedback amplifiers which have a fixed R_F and set the gain with different values of R_G. The feedback resistor R_F is external and, because of the difference in DC potential, needs to be AC-coupled through a 0.01 μF capacitor (see *Figure 16*).

Another characteristic of the LH4200 is that it is permissible to bypass the inverting input with a capacitor to ground. The amplifier is compensated in a way that this results in stable operation, and the open loop gain is increased, which is beneficial for AGC operation.

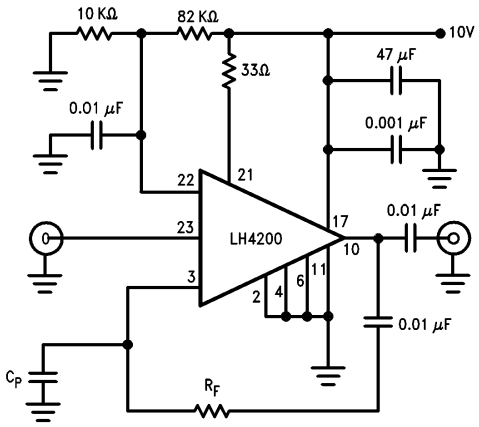
First and second stage are capacitively coupled. The low corner frequency is about 2 MHz. Both input and output stages have built-in power supply bypassing.

A gain stage drives the output stage which is single ended, configured as an emitter follower with 150Ω connected to ground.

Feedback Amplifier Using the LH4200

The feedback amplifier in *Figure 17* works in a 50Ω system. Gate 2 is DC-biased to +1V. The 33Ω in series with pin 21, together with the built-in power supply decoupling capacitor of the input stage, act as a filter. The power supply is additionally bypassed with a 47 μF and a 1000 pF capacitor. Because pin 17 has DC bias it is connected to the output of the amplifier through a 0.01 μF capacitor.

The table included in *Figure 17* shows values for R_F and C_P for three different gain settings. At high gain settings (R_F = 1500Ω, A_V = 33 dB) the gain vs. frequency characteristic rolls off in a rounded fashion (*Figure 18,* curve a); a peaking capacitor C_P will extend the flat response (curve b). For R_F = 860Ω the gain becomes 25 dB and at this setting a peaking capacitor is not needed (curve c).

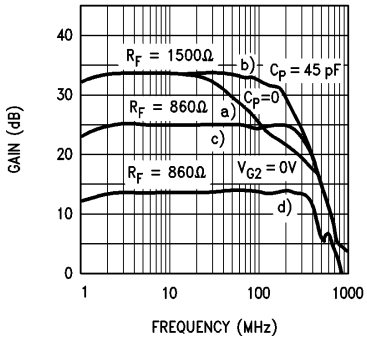


TL/K/10377–19

Note: Pinout shown for D24D package.

Gain	Bandwidth	R_F	C_P
30 dB	150 MHz	1.5k	9–50 pF
25 dB	300 MHz	860Ω	<8 pF
20 dB	500 MHz	430Ω	<1 pF

FIGURE 17. Feedback Amplifier Using the LH4200



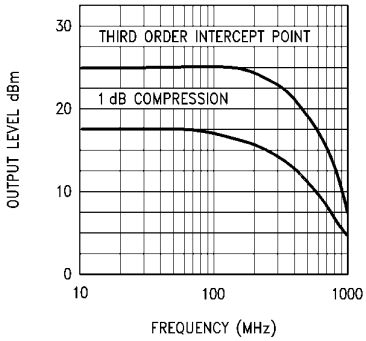
TL/K/10377–20

If not otherwise noted, $C_P = 0$ and $V_{G2} = 1V$.

FIGURE 18. LH4200 Typical Amplifier Response

For still lower R_F the amplifier tends to peak. Low gains without peaking can be obtained by using $R_F = 860\Omega$ and adjusting the DC voltage at gate 2 from +1V to a lower value (*Figure 18,* curve d). This causes the g_{fs} of the GaAs-FET to decrease, and with it drops the gain of the input stage. The gain of the input GaAs-FET is outside the feedback loop and therefore the gain of the amplifier is reduced. This way flat gain characteristics can be achieved to as low as about 10 dB, with bandwidths above 400 MHz.

With a supply voltage of +10V the gain vs. frequency characteristics of the LH4200 stay the same up to output voltages of about 3.2 V_{PP} (14 dBm). Above this level the signal gets clipped. (For more information see the graph on 1 dB compression, *Figure 19*).



TL/K/10377–21

FIGURE 19. Signal Handling Capabilities of the LH4200

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
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13th Floor, Straight Block,
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Hong Kong
Tel: (852) 2737-1600
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National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
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Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
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