Application Report
SNAA045A–May 2007–Revised May 2013

AN-1645 LM4702 Driving a MOSFET Output Stage

ABSTRACT

This application report provides supporting design information regarding Texas Instruments newest offering of high-performance, ultra high-fidelity audio amplifier driver ICs.

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1 Introduction

The LM4702 and its derivatives provide a highly reliable, fully integrated, ultra high-end input stage solution for audio power amplifiers. The LM4702's wide-bandwidth, fully-complementary bipolar design enables superior distortion performance throughout the audio spectrum. Its ±100V operating voltage range allows for power levels up to 450W into 8Ω and 900W into 4Ω.

This unique IC solution provides a quick and easy way to manufacture an ultra high-fidelity amplifier solution, with the piece-of-mind obtained from a fully optimized, stable design.

The LM4702 is available in two grades of performance. The C version has an operating voltage up to ±75V, while the B version operates up to ±100V. The LM4702 is available in a 15-lead TO-220 non-isolated power package. Additional topics regarding the LM4702 can be found in the *AN-1490 LM4702 Power Amplifier Application Report* (SNAA031).

2 Overview

This application report will cover the design of a 2 × 125W, 8Ω with ≤ 1% THD + N amplifier solution using the LM4702 directly driving an output stage that uses a complimentary pair of MOSFETs. Basic information on how to choose a suitable MOSFET device, setting bias levels, performance optimizations, and performance results will be covered. The complete test schematic is included.

The choice of device type and the design of the output stage of a power amplifier are determined by the design requirements and the preference of the designer. A MOSFET device has some preferred features compared to a BJT device. MOSFETs do not suffer from second breakdown allowing the safe operating area (SOA) protection circuitry design to be less complicated. Thermal runaway issues are also much less of a concern with less sensitivity to temperature than a BJT device. MOSFET devices do not have charge storage (minority carriers) reducing switch-off distortion effects. Some just prefer the sound of a MOSFET output stage compared to other devices, a highly subjective criteria but one that is important in the evaluation of an amplifier's performance.

3 How To Choose A MOSFET

The choice of the MOSFET device is limited by the characteristics of the LM4702. The most important limitation is the bias voltage typical of 6V between the SINK and SOURCE pins. This voltage is also the voltage from Gate/Base to Source/Emitter (V_{GS} or V_{BE}) of both devices in the output stage and any degeneration resistors. This limitation restricts MOSFET type to those with a V_T low enough to allow proper bias and performance. A MOSFET device with high threshold voltage cannot be biased correctly and crossover distortion will dominate. For correct biasing the MOSFET must fully conduct at a minimum drain current of 100mA with a V_{GS} of 3V or less. The MOSFET should be able to supply all the necessary output current at V_{GS} = 10V with some headroom. The required output current is 5.6A peak for a 125W/8Ω output. The device needs to be able to supply more than 5.6A with a V_{GS} of less than 10V.

The other performance constraint of the LM4702 is the minimum output drive current of 3mA (5.5mA typical). Although an additional driver stage can be employed to remove the LM4702's drive current limitation, the design in this application report will be done with the LM4702 driving the output stage directly. Devices with lower input capacitance are preferred but are not critical to a well performing design. The amount of drive current from the LM4702 limits the number of devices in parallel that can be driven with a acceptable slew rate. Additional devices in parallel will not be covered in this application report.

An obvious drawback of driving a MOSFET output stage compared to a BJT output stage with the LM4702 is the loss of voltage swing relative to the supply rails. Unless the LM4702 is driven from higher supply rails, the maximum voltage swing with a MOSFET output stage may be lower than a BJT output stage. This is a result of the difference in V_{GS} compared to V_{BE}. The difference in output swing can be minimized through MOSFET selection and the elimination of degeneration resistors.

The MOSEFET devices listed in Table 1 are devices from three suppliers that will meet the design criteria based on the LM4702 limitations for direct drive and the target output power specification into a resistive load. Table 1 is not an exhaustive listing but represents those devices which are commonly used in MOSEFET amplifier designs, were available at the time of writing, and provide good audio performance. All devices listed have a 140V minimum break down voltage rating (V_{DSS}) or higher and drain current (I_D) maximum of 7A or higher. The V_{DSS} and the I_D are the requirements to meet the supply voltage and output current specifications with some headroom to spare. The Drain Current verses Gate to Source Voltage graph (I_D vs. V_{GS}) is used to determine if correct bias can be achieved with 3V or less. This design and device selections may not be suitable for all speaker loads without violating the device's Safe Operating Area (SOA) curves. Proper SOA design must be taken into account for a commercial amplifier product.

Table 1. Devices Pairs

Device Pair	Manufacturer
2SK1057 / 2SJ161	Renesas
2SK1058 / 2SJ162	Renesas
BUZ900 / BUZ905	Magnatec
BUZ901 / BUZ906	Magnatec
2SK1529 / 2SJ200	Toshiba
2SK1530 / 2SJ201	Toshiba
IRFP240 / IRFP9240	International Rectifier

Only one pair from each supplier, the higher voltage or higher current versions, will be tested with performance curves. In addition, an example of high V_T devices, the popular International Rectifier IRFP240/IRFP9240 pair, is also shown. Crossover distortion is the dominant distortion, yet this performance may be acceptable for some market segments.

4 MOSFET Amplifier Design

Figure 1 shows the basic block diagram of an amplifier using the LM4702. The amplifier consists of three building blocks, the LM4702, the bias stage, and the output stage (there are no protection circuits). Each stage will be covered in detail. The power supply design will not be covered as a basic unregulated supply consisting of a transformer, a bridge rectifier, with noise and reservoir capacitors is well known and common.

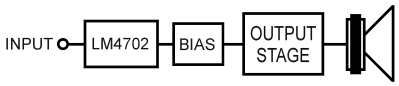

Figure 1. Amplifier Block Diagram

The LM4702 is a high voltage driver that includes the input stage and voltage amplifier stage (VAS) of a power amplifier. The LM4702, with feedback from the output stage, sets the gain and is externally compensated to set the slew rate. The outputs of the LM4702 drive the top and bottom sides of the bias and output stages. The LM4702 performance details are limited to basic recommendations on ranges for gain, slew rate, and the component types that achieve the best performance.

The bias stage performs two functions. First, it sets the DC bias voltage and resulting bias current in the output stage for Class A, AB or B operation. Second, it allows thermal compensation that maintains steady bias current as the output stage devices vary in temperature. As will be shown, certain devices do not need temperature compensation and the bias stage becomes as simple as a resistor. Other devices will need thermal tracking and temperature compensation controlled by the bias stage.

The output stage is a basic Source-Follower stage using a single pair of complementary N-channel and P-channel transistors for simplicity. The same output stage design will be used for all devices listed in Table 1.

5 LM4702 Stage

The LM4702 operates similar to an op amp. The circuit shown in Figure 2 is a non-inverting configuration. Resistors R_i and R_F set the gain to A_V = 1+ R_F/R_i (V/V). The C_i capacitor sets DC gain to unity and the low frequency response by creating a high-pass filter with a -3dB point at $f_{-3dB} = 1/(2\pi C_i R_i)$ (Hz). For sonic quality, the design does not use an AC coupling, DC blocking capacitor. The C_N capacitor shunts high frequency noise present at the input to ground. The compensation capacitor, C_C, sets the slew rate and phase margin to ensure oscillation-free operation.

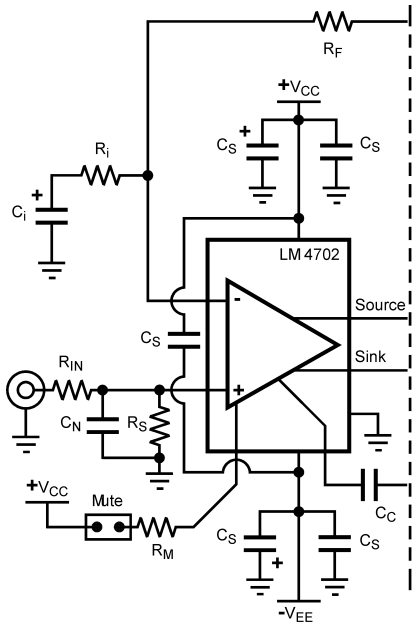

Figure 2. LM4702 Stage

The following are general recommendations for the LM4702 stage:

- Set the gain in the range of 10V/V to 50V/V using low values of metal film resistors for lowest noise. A gain of 30V/V will give excellent results.
- Use a heat sink for the LM4702. For best results, the heat sink temperature should not rise above 55ºC.
- The values of the gain setting resistors and the input resistors should be equal. $R_S = R_F$, $R_{IN} = R_i$. R_S should not be set too low as to cause loading of the source. Setting the resistors to equal values in the associated pairs ensures that the input bias currents will have negligible effect on the input offset voltage.
- Use a silver mica type capacitor for the compensation capacitors, C_C capacitors on the COMP pins, placed close to the LM4702.
- The slew rate should be set to the highest possible while maintaining stability through the power and frequency ranges of operation.
- DC blocking input capacitors affect the low frequency response and their value must be chosen accordingly. An additional film capacitor used in parallel may improve the sonic quality. Eliminating the input capacitor will give the best sonic performance.
- The feedback capacitor, C_i, sets the gain at DC to unity and also affects the low frequency response in relation to the value of the R_i resistor. This capacitor's value should be set using the same recommendations given to selecting the input capacitor's value.
- The input noise capacitor, C_N, is used to filter high frequency noise that may be present on the input signal. This capacitor may be any type and the value is typically 15pF - 47pF.

- Supply bypassing and PCB design each have a significant effect on harmonic distortion levels. Large value current reservoir capacitors in parallel with smaller film capacitors are recommend at the power supply and at the PCB supply terminals. In addition, film capacitor bypassing is recommended at each supply pin of each active device.

6 Bias Stage

This section will cover two different bias stages; a basic, non-temperature compensated bias design and one with thermal tracking and temperature compensation. Whether Class A, Class AB or Class B, the level of bias voltage is independent of the bias stage design.

A non-compensated design involves a simple resistor (or potentiometer for easy bias adjustment) and a capacitor. Figure 3 shows the simple bias stage design. The additional resistor, R_{B2}, is used to set a minimum bias voltage while the potentiometer is used to adjust the bias level as desired. C_{BIAS} may be more than one capacitor, such as the parallel combination of a high value (µF) electrolytic with a small value (pF) film type capacitor. R_{BG} helps to reduce the 2nd harmonic.

For thermal tracking with temperature compensation, the very useful V_{BE} multiplier is used as shown in Figure 4.

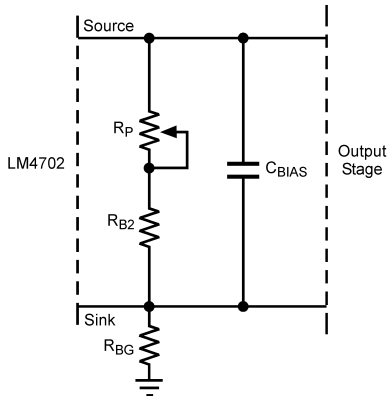

Figure 3. Resistor Bias Stage

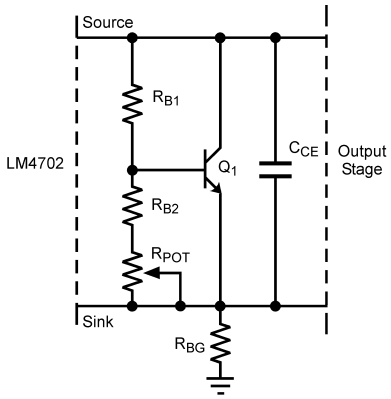

Figure 4. Resistor Bias Stage

A V_{BE} multiplier works by using the voltage across the Base-Emitter junction of a BJT transistor, Q_1, to set the bias voltage. The R_{B2} resistor and R_{POT} potentiometer are in parallel with the V_{BE} voltage of Q_1. Using Ohm's Law, the current through R_{B2} and R_{POT} will be:

$$I = V_{BE} / (R_{B2} + R_{POT}) \text{ (A)} \quad (1)$$

Ignoring the small amount of current that flows into the base of Q_1, this same current flows through R_{B1}. Using Ohm's Law again, the voltage across R_{B1} is equal to:

$$V_{B1} = R_{B1} * I \text{ (V)} \quad (2)$$

The total bias voltage is equal to the Collector to Emitter voltage, V_{CE}, of Q_1, which is also the same as the voltage across R_{B1}, R_{POT}, and R_{B2}. Combining the voltage across R_{B2} and R_{POT}, which is the same as the V_{BE} voltage of Q_1, and the voltage found above across R_{B1} results in:

$$V_{BIAS} = V_{CE} = R_{B1} * I + V_{BE} \text{ (V)} \quad (3)$$

Substituting for the current, I, results in:

$$V_{BIAS} = R_{B1} * [V_{BE}/(R_{B2} + R_{POT})] + V_{BE} \text{ (V)} \quad (4)$$

Simplifying and arranging results in the well known V_{BE} multiplier equation:

$$V_{BIAS} = V_{BE} * [1 + R_{B1}/(R_{B2} + R_{POT})] (V) \quad (5)$$

As can be seen, the bias voltage will track the V_{BE} voltage of Q_1 at a fixed ratio. The bias voltage will change with temperature when Q_1 is mounted to the same heat sink as the output devices. The thermal feedback and temperature compensation works as follows. For a given bias voltage, the output stage's bias current will increased as the temperature increases. However, since Q_1 is mounted along side the output devices, its (Figure 4) V_{BE} voltage will decrease with increased temperature. This reduces the current through resistors connected to Q_1's base, which results in a reduction of bias voltage. This negative feedback produces a bias voltage that changes in order to maintain a stable bias current in the output stage.

6.1 Determining Output Stage Bias Current

For a Class AB amplifier design, bias current is chosen such that crossover distortion is minimized while also keeping quiescent power dissipation low. Higher bias current reduces harmonic distortion levels. At some point there is little reduction with increased bias current and resulting power dissipation. A tradeoff in the bias current level must be made between THD performance and power dissipation.

MOSFET output stages typically need higher bias current than BJT output stages for good performance in a Class AB amplifier design. Using the Magnatec BUZ901/BUZ906 pair and the resistor bias circuit shown in Figure 3, different bias current levels are shown in the FFT versus Frequency graphs and oscilloscope views (Figure 5 to Figure 10). For each graph, the output power level is 40W into an 8Ω resistive load. The measurement equipment is set to notch out the fundamental frequency of the test signal. The fundamental is reduced by more than -110dB relative to 0dB. 0dB is set equal to the voltage for 40W into 8Ω.

The first graph, Figure 5, has a bias current of 50mA and shows a case of insufficient bias current. The result is THD that is dominated by crossover distortion. This is indicated by the high level and number of harmonics. Figure 6 shows the residual harmonics on an oscilloscope and clearly crossover distortion is dominant.

Increasing the bias current to 150mA reduces the magnitude of the harmonics as shown in the FFT of Figure 7 and the oscilloscope view in Figure 8.

Figure 9 and Figure 10 show the harmonic content when the bias is pushed all the way to 500mA.

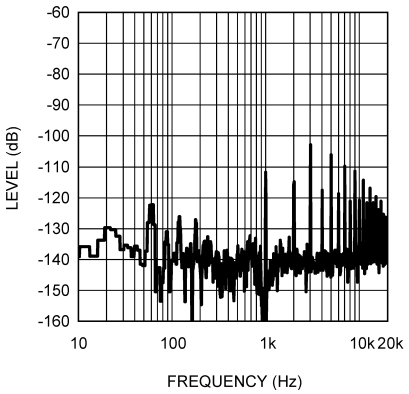

Figure 5. 50mA Bias Current

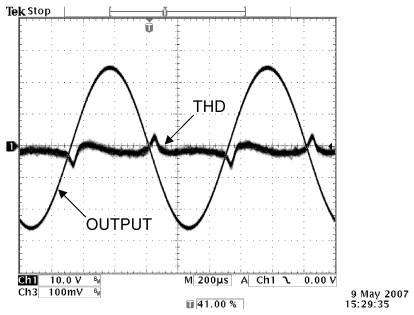

Figure 6. 50mA Bias Current

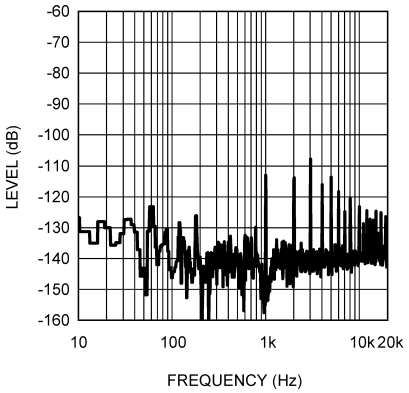

Figure 7. 150mA Bias Current

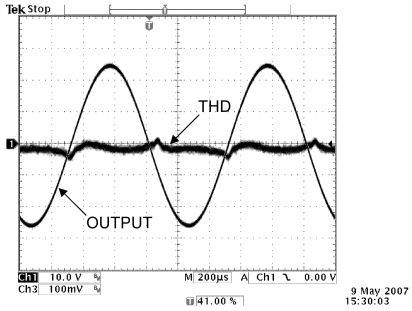

Figure 8. 150mA Bias Current

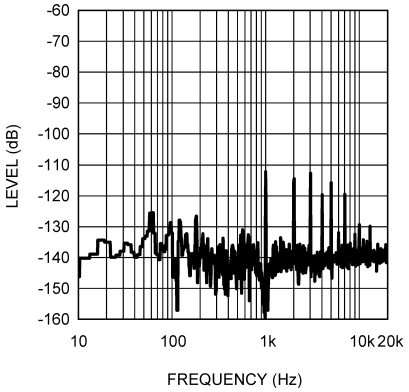

Figure 9. 500mA Bias Current

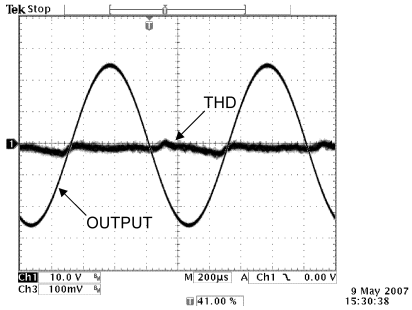

Figure 10. 500mA Bias Current

Figure 11, Figure 12, and Figure 13 show the difference in harmonics with bias levels of 100mA, 200mA, and 300mA, respectively, using the Magnatec BUZ901/BUZ906 pair. Similar results using the same bias current levels can be observed with any of the devices listed in Table 1.

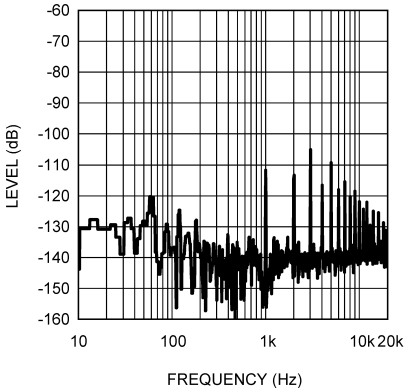

Figure 11. 100mA Bias Current

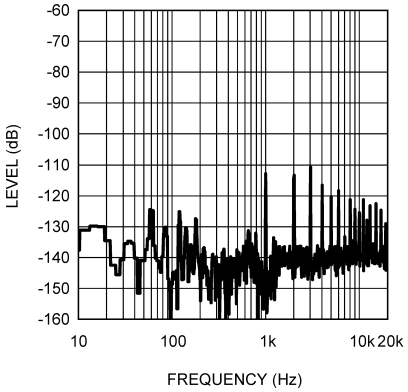

Figure 12. 200mA Bias Current

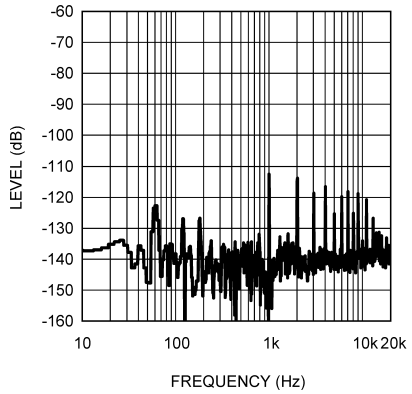

Figure 13. 300mA Bias Current

Table 2, Table 3, and Table 4 list the resulting 1kHz THD + N measurement at 40W into an 8Ω load with a 22kHz measurement bandwidth. The tables show that bias currents above 200mA produce only minor improvements in THD + N at a significant power dissipation cost.

Table 2. Magnatec Bias Current and THD+N

Bias Current	1kHz THD+N at 40W/8Ω Single Channel, 22kHz BW
50mA	0.00129%
100mA	0.00104%
150mA	0.00085%
200mA	0.00068%
250mA	0.00064%
300mA	0.00062%
1A	0.00061%

Table 3. Renesas Bias Current and THD+N

Bias Current	1kHz THD+N at 40W/8Ω Single Channel, 22kHz BW
50mA	0.00129%
100mA	0.00098%
150mA	0.00081%
200mA	0.00074%
250mA	0.00070%
300mA	0.00068%
1A	0.00075%

Table 4. Toshiba Bias Current and THD+N

Bias Current	1kHz THD+N at 40W/8Ω Single Channel, 22kHz BW
50mA	0.00085%
100mA	0.00070%
150mA	0.00067%
200mA	0.00064%
250mA	0.00061%
300mA	0.00057%
1A	0.00055%

The previous graphs and the information in Table 2, Table 3, and Table 4 indicate that the a range of 100mA to 200mA of bias current in the output stage produces low magnitude harmonics and manageable power dissipation.

Because of the higher V_T the IRFP240/IRFP9240 pair cannot be biased correctly to eliminate crossover distortion and THD performance will be affected. The maximum bias voltage obtained was 7.1V with no resistor between the SINK and SOURCE pins of the LM4702 (A 20kΩ resistor may be used with the bias voltage reduced to 7V). The bias current is 25mA under these conditions. Figure 14 shows the THD residual on an oscilloscope indicating crossover distortion is dominant.

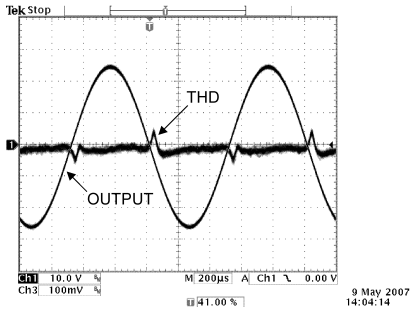

Figure 14. 40W Output and THD Residual

6.2 Determining Bias Circuit Design

Device characteristics and design goals determine whether thermal tracking is needed for stable bias current over temperature. To determine which devices need thermal tracking and which do not, the Drain Current verses Gate - Source voltage (I_D vs. V_{GS}) graph in the device datasheet can be used. Device manufacturers typically have multiple plots on the I_D - V_{GS} graph for different case temperatures. The intersection point of the plots is where stable bias current can be achieved at a fixed bias voltage and without thermal tracking. At higher or lower V_{GS}voltages, the drain current will vary with case temperature.

Inspection of the graphs for the Renesas 2SK1058/2SJ162 pair and the Magnatec BUZ901/BUZ906 pair shows that three different case temperature plots all intersect at low drain current (<0.5A). The Toshiba 2SK1530/2SJ201 pair and International Rectifier IRFP240/IRFP9240 pair graphs have an intersection of the three plots at a very high drain current (>5A). In fact, the 2SJ201 does not appear to have an intersection point on the graph. From these graphs it is determined that the Renesas and Magnatec pairs can be biased in the 100mA to 200mA range previously determined without the need for thermal tracking. A simple bias resistor circuit will give stable bias current over operating temperature.

The Toshiba 2SK1530/2SJ201 pair will require the V_{BE} multiplier circuit for thermal tracking with temperature compensation to achieve stable bias current over temperature. A bias level of 150mA in the output stage will be used for the 2SK1530/2SJ201 pair.

The IRFP240/IRFP9240 would need thermal tracking if properly biased since the intersection point on the I_D - V_{GS} is at high current. The limitation in bias voltage with the LM4702 does not allow for proper bias.

It may be desirable to have higher bias current to reduce distortion harmonics, improve THD performance, affect sonic qualities, or some other design criteria. High bias current levels can be set with a simple resistor bias design. The tradeoff for simplicity is more bias variation over case temperature. The amount of variation can be determined using the device's I_D - V_{GS} graph. Depending on the device and design goal, the amount of variation may be acceptable at a higher bias level. For example, the Renesas 2SK1058/2SJ162 devices could be biased at 250mA without temperature compensation. The bias current will vary much more than if the bias is set at the intersection point but the amount of variation may be acceptable. If bias stability is not acceptable then additional circuitry will be required for temperature compensation. Devices like the Toshiba 2SK1530/2SJ201 pair are not well suited for a resistor bias (fixed bias voltage) scheme because the current will significantly vary with case temperature. The effects of bias instability on sonic performance is not investigated in this application report.

6.3 Bias Stability

The Bias Current versus Time graphs below were created by running the output stage at 40W until steady state case and heat sink temperature are reached. The input signal is turned off (Time = 0) and the bias current recorded over time. It should be reportd that the graph units are not linear as indicated. Bias current is measured at 10 second intervals for the first two minutes after the input signal was turned off then at 30 second intervals up to five minutes. One final measurement is taken at 10 minutes. The time steps are one reason for the different slopes on the time curve, more evident on the higher bias graphs. There are two plots on each graph, one indicating the quiescent steady state bias and the other indicating the bias over time after producing 40W of output power. There are several factors that affect the data such as θ_{JC} of the package and heat sink size which contribute to thermal delay. Device characteristics also affect the slopes of the time curves.

Figure 15 is the Renesas 2SK1058/2SJ162 pair operating at a bias of 100mA for the output stage in quiescent steady state. The power test shows a slightly higher bias when the devices are hot indicating that increasing the quiescent steady state bias would reduce variation caused by increased temperature. Figure 16 shows that at higher bias the slope of the curve and location is are reversed. The power test shows lower bias current when the devices are hot indicating which side of the intersection point of the device's I_D-V_{GS} graph each bias current setting is located. A bias current of 115mA will be used for the Renesas 2SK1058/2SJ162 pair.

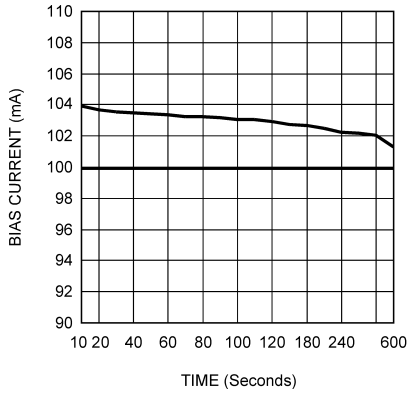

Figure 15. 2SK1058/2SJ162 at 100mA Bias

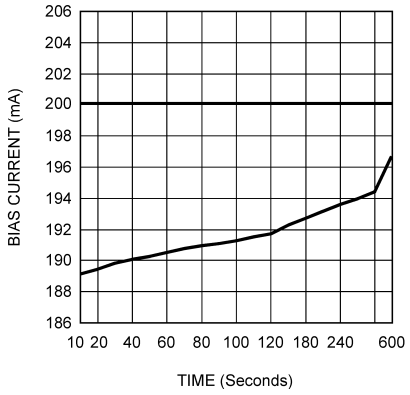

Figure 16. 2SK1058/2SJ162 at 200mA Bias

The same tests and graphs for the Magnatec BUZ901/BUZ906 are in Figure 17 and Figure 18. Because the resolution of the device's I_D-V_{GS} graph is limited the intersection point is not distinguishable. Because of the difference in slope sign on the time curves in Figure 17 and Figure 18, the intersection point is between the two bias settings and appears to be closer to 200mA than 100mA. This is determined by looking at how close the bias current returns to the steady state level after 10 minutes. A bias current of 180mA will be used for the Magnatec BUZ901/BUZ906 pair.

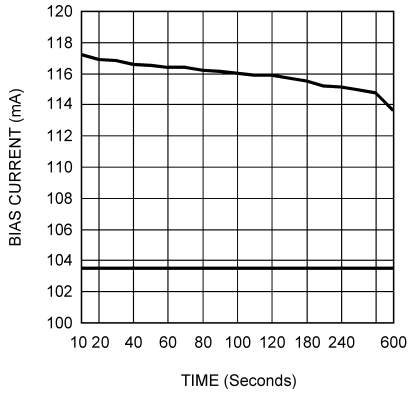

Figure 17. BUZ901/BUZ906 at 100mA Bias

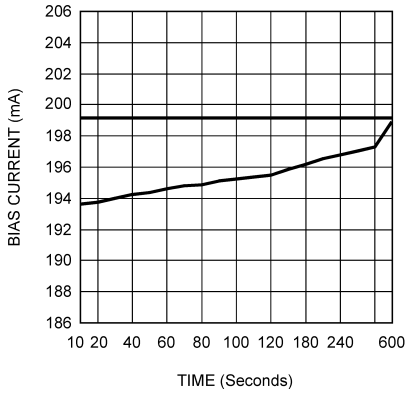

Figure 18. BUZ901/BUZ906 at 200mA Bias

A target bias current of 150mA is chosen for the Toshiba 2SK1530/2SJ201 pair using the V_{BE} multiplier circuit for thermal compensation. The V_{BE} multiplier circuit of Figure 4 has more variation in bias voltage with temperature than needed for the 2SK1530/2SJ201 pair. To reduce the amount of change with temperature the circuit is modified as shown in Figure 19.

Resistor R_{B3} is added to set a temperature independent voltage while the voltage created by the rest of the circuit will vary with temperature (See Equation 5). The correct amount of variation in bias voltage to maintain a target bias current of 150mA over operating temperature is found by using the resistor bias circuit shown in Figure 3. The bias voltage is measured with 150mA of bias current at initial power on when the case temperature of the devices is low. The resistor value is adjusted to maintain 150mA of bias current and the voltage measured as the case temperature changes. Using the V_{BE} voltage change with temperature of 2mV/°C and the amount of voltage change needed across the temperature range, the correct ratio of R_{B1} and R_{B2} can be determined. The values determined are R_{B1} = 1kΩ, R_{B2} = 500Ω, R_{B3} = 390Ω. Figure 20 shows the bias current stability graph. The graph is created the same as done for the other devices.

Figure 20 shows the bias current is slightly over compensated for temperature but sufficiently stable for the needs of this report. Additional refinements to improve bias stability with temperature were not performed.

The International Rectifier IRFP240/IRFP9240 devices are not tested for bias stability with case temperature. With the limitation in bias voltage using the LM4702, the bias voltage is low enough that at the highest operating case temperature the bias current is no more than 100mA in the output stage. The side benefit of this bias current instability is distortion is reduced as the amplifier heats up due to the increase in bias current in the output stages and resulting reduction of crossover distortion.

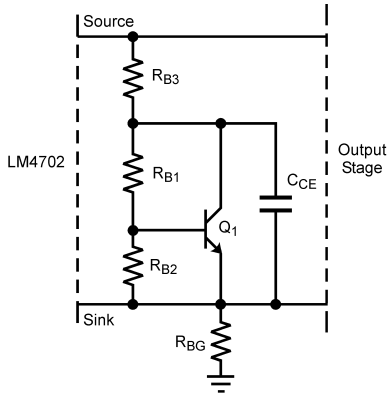

Figure 19. Modified V_{BE} Multiplier Bias Stage

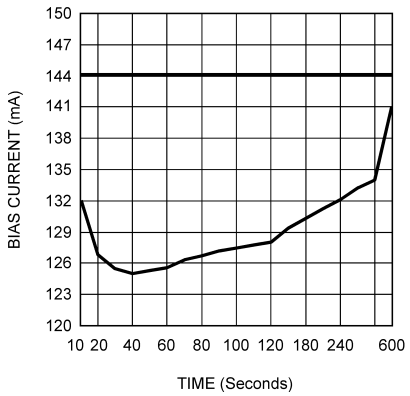

Figure 20. 2SK1530/2SJ201 Bias Stability

7 Output Stage

The output stage is a Source-Follower design. The output stage consists of the gate resistors, R_G, complementary MOSFET devices, and a snubber circuit, R_{SN} and C_{SN}. The output stage is shown in Figure 21. Only the gate resistor and bias voltage level will be varied to determine effect on performance for each of the different devices listed in Table 1. The design is a single pair of complementary devices in the output stage. This also eliminates the need for source degeneration resistors. For a design with multiple pairs of complementary devices in parallel, source resistors are recommended along with V_{GS} matching of devices.

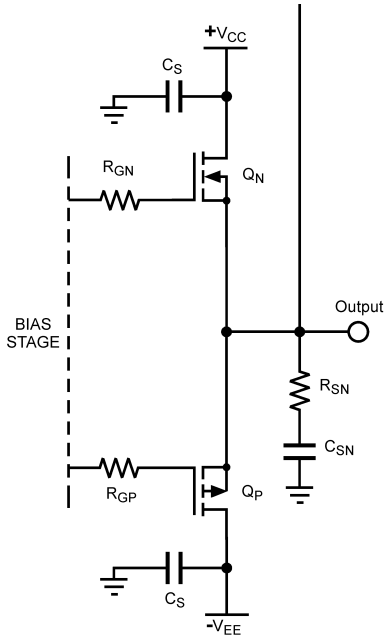

Figure 21. Source-Follower MOSFET Output Stage

7.1 Determining Gate Resistor Values

The gate resistors, R_{GN} and R_{GP}, are necessary for stability, MOSFET devices will often oscillate without them. The value is chosen for best THD performance across the power and frequency range of operation while maintaining stability. The values are determined by trial and error adjustment for each set of devices. In general, the frequency pole location of the low-pass filter created by the gate resistor and the device input capacitance, C_{ISS}, is chosen to be the near the same for both the N-channel FET and P-channel FET. The pole location is found using the formula:

$$f_{-3dB} = \frac{1}{(2\pi \times C_{ISS} \times R_{GATE})} (Hz) \quad (6)$$

The exact pole location is application and device dependent.

One method to determine the right gate resistor value is to overdrive the amplifier with a square wave. The shape of the rise and fall curves will indicate a correct value. Figure 22 and Figure 23 are oscilloscope views showing how a wrong value can affect the rise and fall curves. If the value is too high then a "bump" appears in the rising or falling edge of the output signal. If the value is too low the amplifier will oscillate. Both of the gate resistors affect the rising and falling edges of the output signal requiring a middle point of adjustment for smooth curves. The input signal is a $2V_{RMS}$, 1kHz square wave.

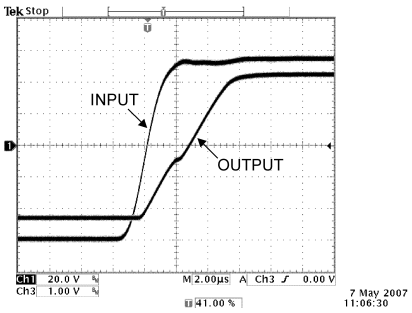

Figure 22. Rise Curve with Incorrect R_{GATE} Value

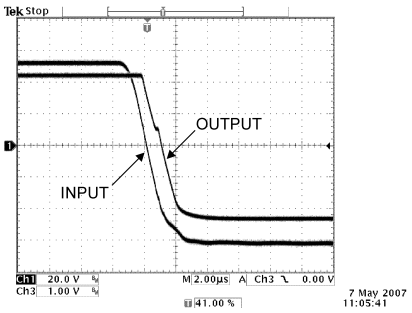

Figure 23. Fall Curve with Incorrect R_{GATE} Value

Compare the output signals in Figure 24 and Figure 25 where the gate resistor values are set correctly with those found in Figure 22 and Figure 23. The rising and falling edges are much smoother and linear. In all cases, stability was maintained. If the value of R_G is too low (especially for the N-channel FET) the amplifier will oscillate.

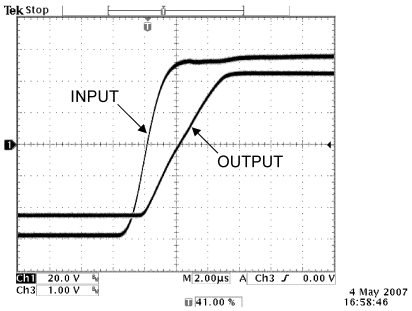

Figure 24. Rise Curve with Correct R_{GATE} Value

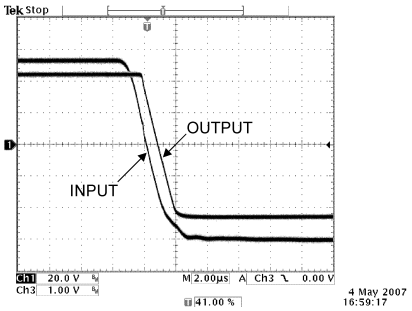

Figure 25. Fall Curve with Correct R_{GATE} Value

7.2 Determining Snubber Circuit Component Values

The Snubber circuit is composed of R_{SN} and C_{SN}. The common value of 0.1µF is chosen for C_{SN} and then a starting value of 10Ω is used for R_{SN}. The pole location created by the circuit is found using:

$$f_{-3dB} = \frac{1}{(2\pi \times R_{SN} \times C_{SN})} \ (Hz) \tag{7}$$

If small, high frequency oscillation is observed on the output then the snubber values need to be adjusted. Leave the value of R_{SN} set to 10Ω and increase the value of C_{SN} until the oscillation ceases.

8 Complete MOSFET Amplifier Schematic

Combining the stages results in the complete MOSFET amplifier circuit shown in Figure 26 (only one channel for simplicity). The other channel is identical in design and values. This is the circuit that will be used for all testing with the only schematic variation being the bias stage. Either the simple bias resistor of Figure 3 or the V_{BE} multiplier of Figure 19 will be used depending on the output devices from Table 1. The gate resistor values were adjusted for each device until smooth rising and falling edges were obtained.

Figure 26 shows the complete board schematic including the power supply bypassing capacitors and all associated values for external components. Potentiometers are used for the gate resistors for easy adjustment for different device characteristics.

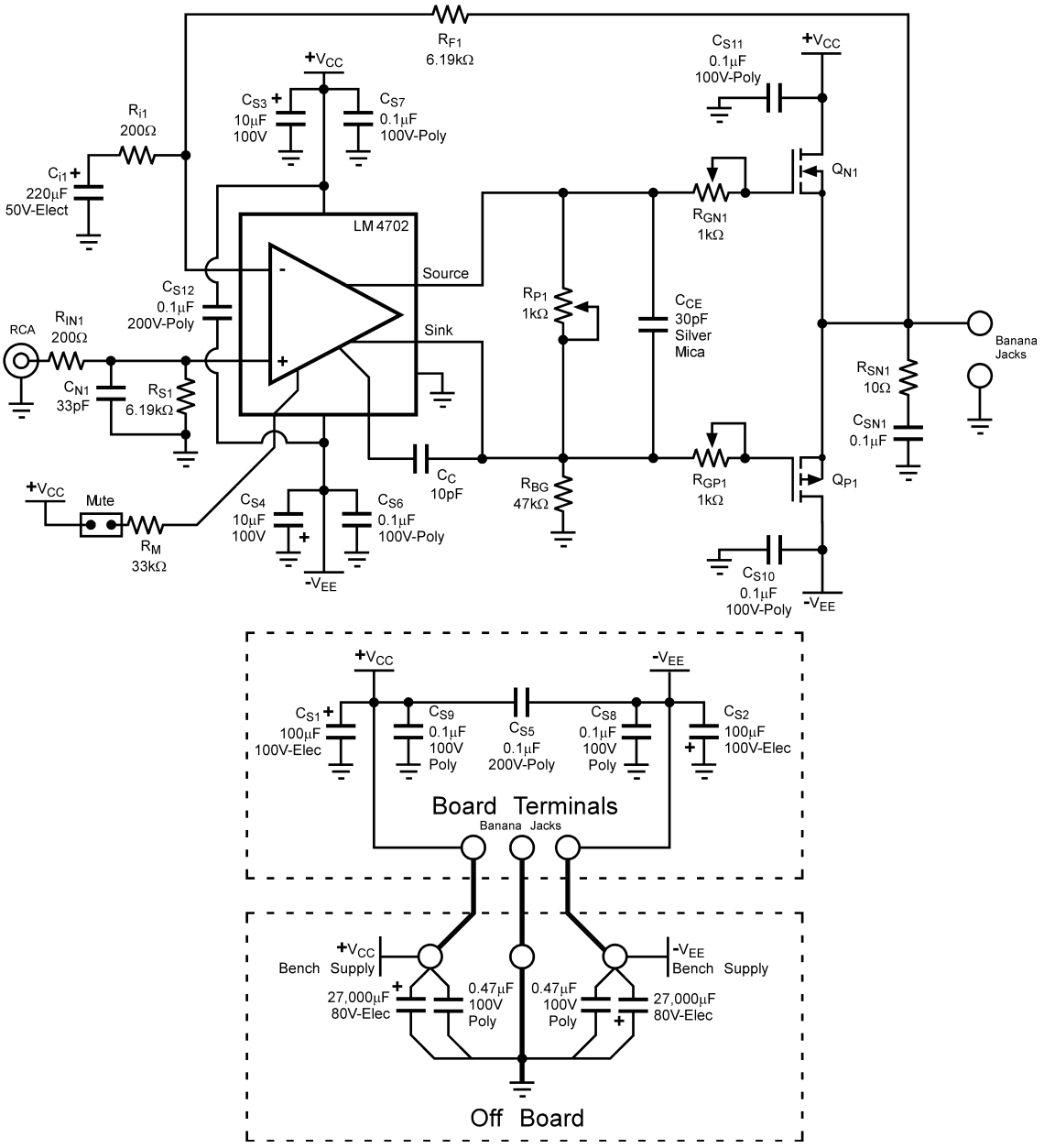

Figure 26. Complete MOSFET Amplifier Circuit

9 THD+N Performance

With the bias levels and circuits now determined, THD + N performance can be measured and compared for the different devices. In all cases, both channels of the LM4702 were on and in phase driven from an Audio Precision System 1. This presents the worse case measurement conditions for the different graphs.

9.1 RENESAS 2SK1058/2SJ162 PAIR

The 2SK1058/2SJ162 pair were biased at 115mA for the output stage. The 115mA bias current was very stable with changes in case temperature. A benefit of these Renesas devices is the integration of gate protection diodes eliminating the need for external gate protection components. The gate resistor values were determined by overdriving with a square wave and adjusting their value until the rising and falling edges were as linear as possible while maintaining stability. For these devices the gate resistors were 190Ω - 210Ω on the N-channel FET and 240Ω - 330Ω for the P-channel FET. The FFT graphs used the Audio Precision System 1's Reading function to remove the fundamental for better resolution. report the scale of the graphs start at -60dB. This is dB relative to the fundamental, or in other words, the fundamental peak is equal to 0dB. The fundamental is notched out by the measurement equipment reducing it's level to -110dB relative. Figure 27, Figure 28, and Figure 29 show the distortion levels of the harmonics at 1W, 40W, and 100W output power levels, respectively, with a 1kHz test signal.

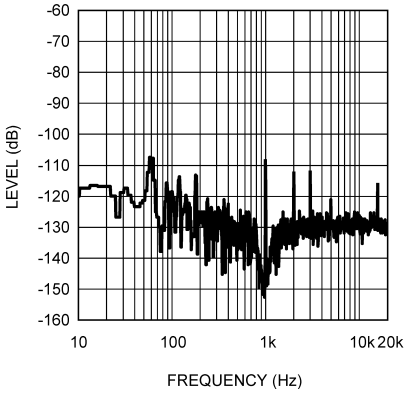

Figure 27. FFT vs Frequency (Reading)
P_{OUT} = 1W/Channel, R_L = 8Ω
2SK1058/2SJ162

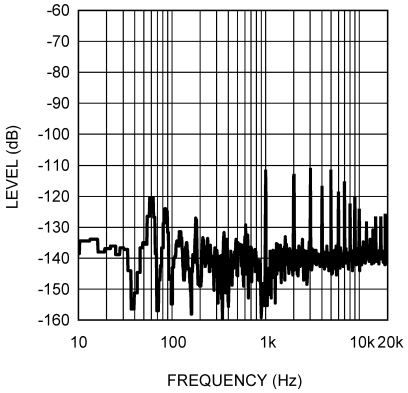

Figure 28. FFT vs Frequency (Reading)
P_{OUT} = 40W/Channel, R_L = 8Ω
2SK1058/2SJ162

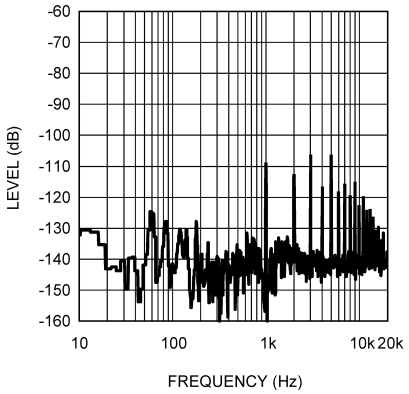

Figure 29. FFT vs Frequency (Reading)
P_{OUT} = 100W/Channel, R_L = 8Ω
2SK1058/2SJ162

Figure 30 and Figure 31 show that high performance is possible over the frequency and power range of interest. Figure 30 has a range of 0.0005% to 1% to increase resolution. The 1% power level is 125.5W/Channel into an 8Ω load.

Figure 32 compares different bandwidth settings on the measurement equipment and the effect on a 1kHz plot during an output power sweep. The difference between the plots and the bandwidth setting shows the increase in THD + N is noise (+N) and not harmonics (THD).

The frequency response at 100W/Channel is shown in Figure 33. The snubber circuit is removed for all frequency response testing. The ±3dB range is quite good. However, notice there is a knee or point of inflection on the plot at approximately 68kHz where response begins to roll off quickly. This point occurs when the slew rate limit is reached. The measured slew rate was 17V/µs with the output stage directly driven by the LM4702. Slew rate may also be calculated by using the inflection point on the frequency response graph and Slew Rate = $[2\pi*f*V_{OPEAK}]/10^6$ (V/µs) where f is the frequency of the inflection point on the frequency response graph and V_{OPEAK} is the peak output voltage.

The low frequency roll off is a result of the high-pass filter created with C_i and R_i. Increasing the values will move the low frequency roll off even lower. Both channels are shown in Figure 33 but are indistinguishable at the resolution and size shown.

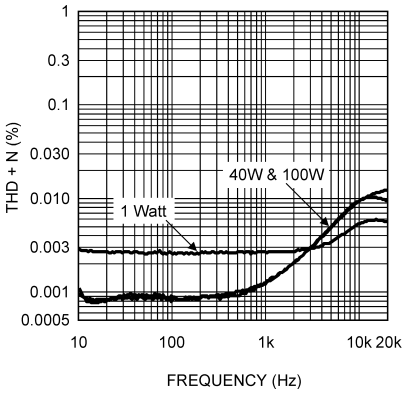

Figure 30. THD+N vs Frequency P_{OUT}/Channel, R_L = 8Ω, 80kHz BW 2SK1058/2SJ162

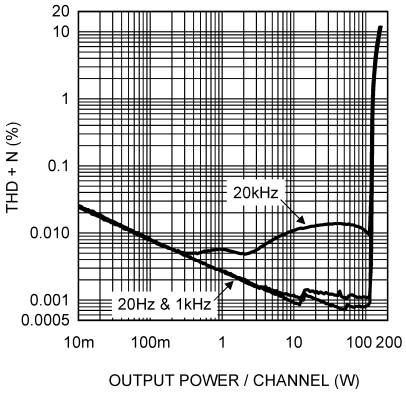

Figure 31. THD+N vs Output Power/Channel R_L = 8Ω, 80kHz BW 2SK1058/2SJ162

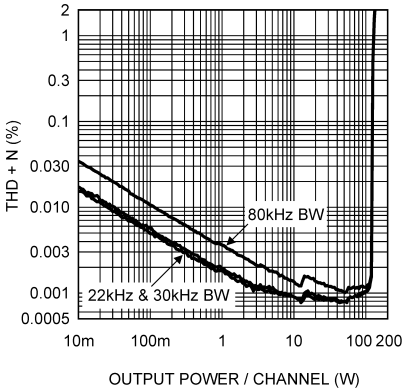

Figure 32. THD+N vs Output Power/Channel R_L = 8Ω, 1kHz 2SK1058/2SJ162

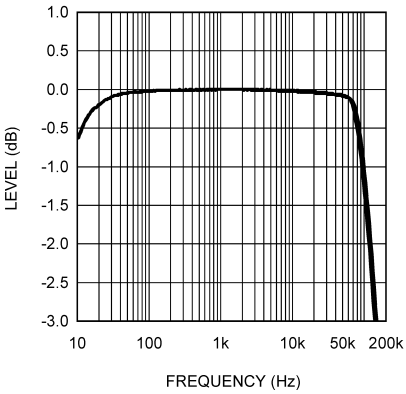

Figure 33. Frequency Response P_{OUT}/Channel = 100W (0dB), R_L = 8Ω, 2SK1058/2SJ162

9.2 Slew Rate

The LM4702's output drive current (3mA minimum, 5.5mA typical) limits the slew rate. MOSFET devices have significant input capacitance making the amount of drive current an issue. Slew rate can be increased using an intermediate driver or buffer stage. To verify that the drive current is the limiting factor for slew rate, a simple driver stage was added to the output stage. This is shown in Figure 34. A supply voltage of +/-40V was used instead of +/-55V because of the voltage limitation of the BD139/BD140 devices (80V).

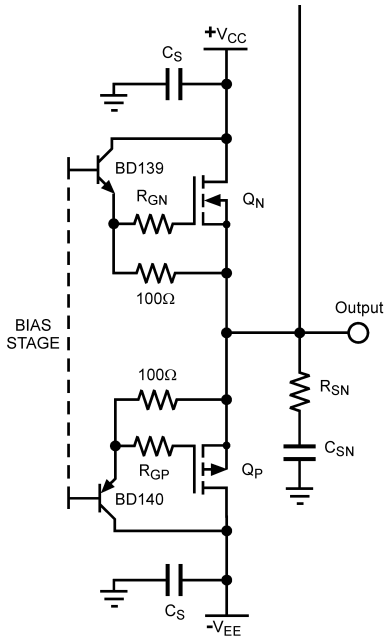

Figure 34. Output Stage with Driver Stage

One channel of the amplifier had the driver stage added while the other channel used direct drive from the LM4702 for easy comparison. The output stage in both channels was biased at the same 115mA. The frequency response graph in Figure 35 compares the two channels delivering 60W of output power into 8Ω resistive loads. As can be easily seen, the channel with the driver stage has much higher bandwidth because of higher slew rate. The channel with a the driver stage has a slew rate of 30V/µs compared to 17Vµs for the channel with direct drive. Optimizations in the driver stage may result in better performance. The apparent difference in the plots for the direct drive channel to the previous direct drive 100W Frequency Response graph above is that the output power is only 60W. As the power level is increased a higher slew rate is needed to maintain the same frequency response curve.

The oscilloscope view in Figure 36 compares the rising edge of the direct drive with an output stage using a driver stage.

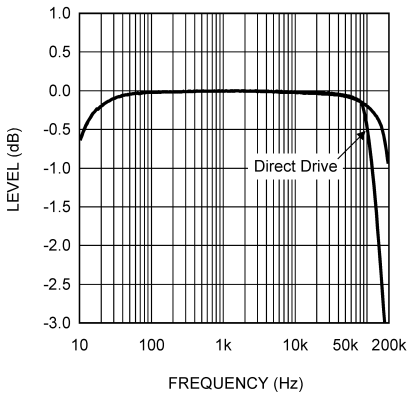

Figure 35. Frequency Response with Driver Stage P_{OUT}/Channel = 60W (0dB), R_L = 8Ω, 2SK1058/2SJ162

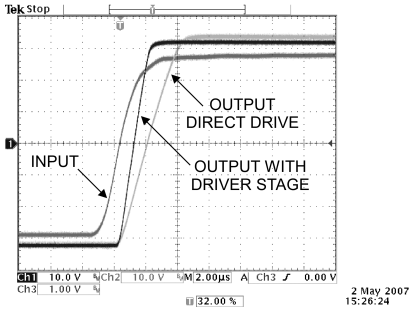

Figure 36. Rise Curve with Driver Stage

9.3 Magnatec BUZ901/BUZ906 Pair

The same tests were performed using the BUZ901/BUZ906 pair in the output stage biased at 180mA. Bias current is very stable with changes in case temperature at 180mA. The gate resistor values were determined by overdriving with a square wave and adjusting their value until the rising and falling edges were as linear as possible while maintaining stability. For these devices, the gate resistors were 175Ω - 220Ω on the N-channel FET and 450Ω - 530Ω for the P-channel FET. The FFT graphs used the Audio Precision System 1's Reading function to remove the fundamental for better resolution. Figure 37, Figure 38, and Figure 39 show the distortion levels of the harmonics at 1W, 40W, and 100W output power levels, respectively, with a 1kHz test signal.

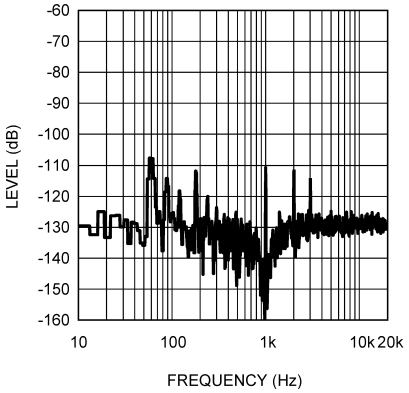

Figure 37. FFT vs Frequency (Reading) P_{OUT} = 1W/Channel, R_L = 8Ω, BUZ901/BUZ906

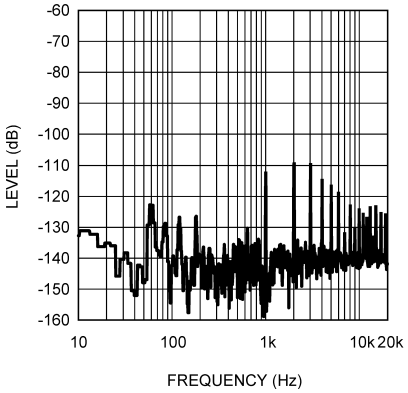

Figure 38. FFT vs Frequency (Reading) P_{OUT} = 40W/Channel, R_L = 8Ω, BUZ901/BUZ906

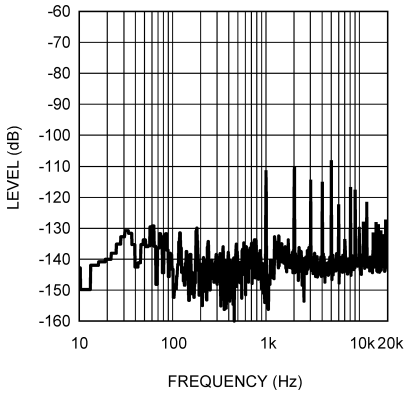

Figure 39. FFT vs Frequency (Reading) P_{OUT} = 100W/Channel, R_L = 8Ω, BUZ901/BUZ906

Figure 40 and Figure 41 show that high performance is possible over the frequency and power range of interest. Figure 40 has a range of 0.0005% to 1% to increase resolution. The 1% power level is 128W/Channel into an 8Ω load.

Figure 42 compares different bandwidth settings on the measurement equipment and the effect on a 1kHz plot during an output power sweep. The difference between the plots and the bandwidth setting shows the increase in THD + N is noise (+N) and not harmonics (THD).

The frequency response at 100W/Channel is shown in Figure 43. The measured slew rate was 16.5V/µs with the output stage directly driven by the LM4702. Both channels are plotted in Figure 43.

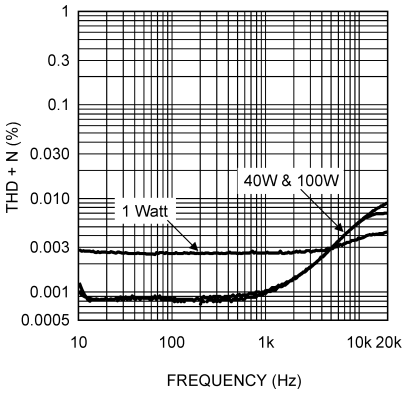

Figure 40. THD+N vs Frequency
P_{OUT}/Channel, R_L = 8Ω, 80kHz BW
BUZ901/BUZ906

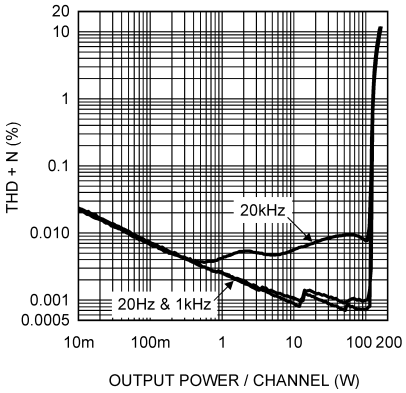

Figure 41. THD+N vs Output Power/Channel
R_L = 8Ω, 80kHz BW
BUZ901/BUZ906

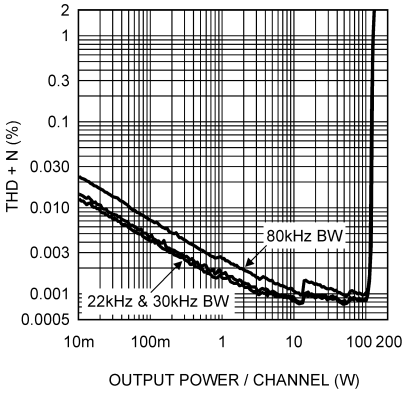

Figure 42. THD+N vs Output Power/Channel
R_L = 8Ω, 1kHz
BUZ901/BUZ906

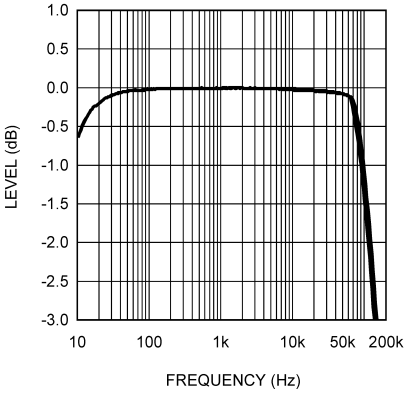

Figure 43. Frequency Response
P_{OUT}/Channel = 100W (0dB), R_L = 8Ω,
BUZ901/BUZ906

9.4 Slew Rate

The driver stage of Figure 34 was used to compare direct drive of the output stage using the Magnatec BUZ901/906 pair. One channel of the amplifier had the driver stage added while the other channel used direct drive from the LM4702 for easy comparison. The output stage in both channels was biased to the same 180mA. The frequency response graph in Figure 44 compares the two channels delivering 60W of output power into 8Ω resistive loads. The results are similar to those achieved by the Renesas 2SK1058/2SJ162 devices with significant improvement in frequency response with a driver stage. The channel with a the driver stage has a slew rate of 32V/µs compared to 16.6Vµs for the channel with direct drive.

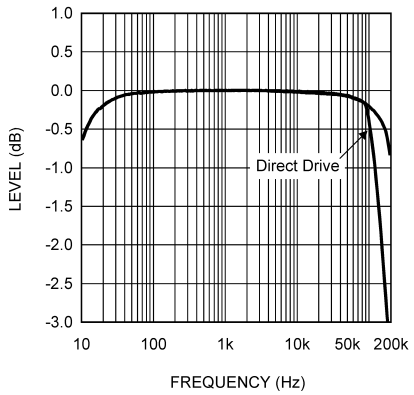

Figure 44. Frequency Response with Driver Stage
P_{OUT}/Channel = 60W (0dB), R_L = 8Ω
BUZ901/BUZ906

9.5 Toshiba 2SK1530/2SJ201 Pair

The same tests were performed using the 2SK1530/2SJ201 pair in the output stage biased at 145mA. The V_{BE} multiplier of Figure 19 was used for bias and thermal compensation to obtain a stable bias current over case temperature. The gate resistor values were determined by overdriving with a square wave and adjusting their value until the rising and falling edges were as linear as possible while maintaining stability. For these devices, the gate resistors were 175Ω on the N-channel FET and 500Ω for the P-channel FET. The FFT graphs used the Audio Precision System 1's Reading function to remove the fundamental for better resolution. Figure 45, Figure 46, and Figure 47 show the distortion levels of the harmonics at 1W, 40W, and 100W output power levels, respectively, with a 1kHz test signal.

Figure 48 and Figure 49 show that high performance is possible over the frequency and power range of interest. Figure 48 has a range of 0.0005% to 1% to increase resolution. The 1% power level is 155W/Channel into an 8Ω load.

Figure 50 compares different bandwidth settings on the measurement equipment and the effect on a 1kHz plot during an output power sweep. The difference between the plots and the bandwidth setting shows the increase in THD + N is noise (+N) and not harmonics (THD).

The frequency response at 100W/Channel is shown in Figure 51. The measured slew rate was 12.5V/µs with the output stage directly driven by the LM4702.

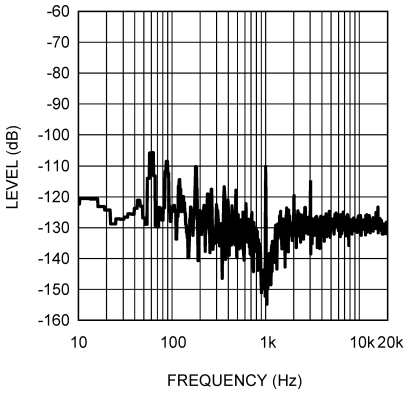

Figure 45. FFT vs. Frequency (Reading)
P_{OUT} = 1W/Channel, R_L = 8Ω
2SK1530/2SJ201

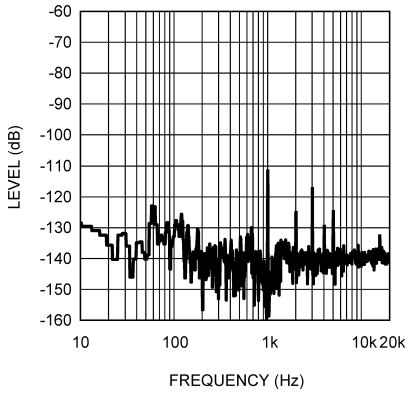

Figure 46. FFT vs. Frequency (Reading)
P_{OUT} = 40W/Channel, R_L = 8Ω
2SK1530/2SJ201

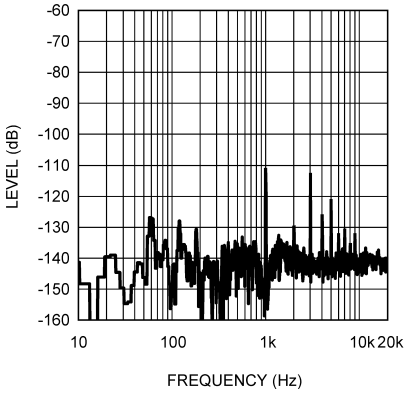

Figure 47. FFT vs. Frequency (Reading)
P_{OUT} = 100W/Channel, R_L = 8Ω
2SK1530/2SJ201

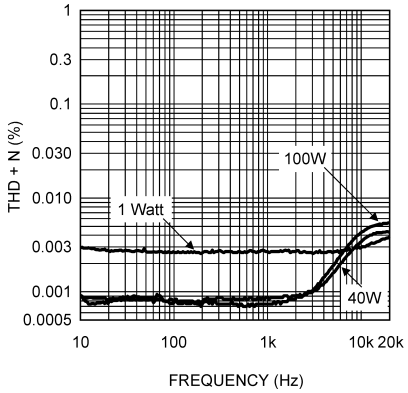

Figure 48. THD+N vs Frequency
P_{OUT}/Channel, R_L = 8Ω, 80kHz BW
2SK1530/2SJ201

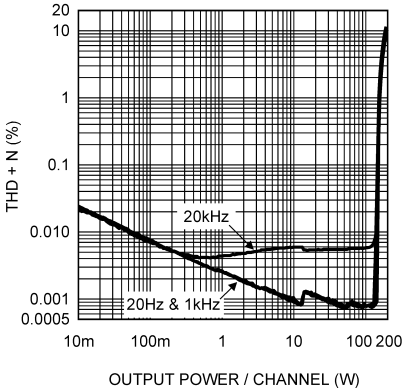

Figure 49. THD+N vs Output Power/Channel
R_L = 8Ω, 80kHz BW
2SK1530/2SJ201

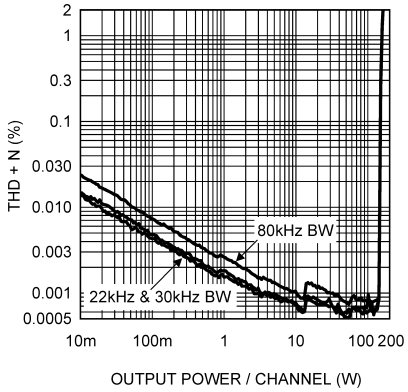

Figure 50. THD+N vs Output Power/Channel
R_L = 8Ω, 1kHz
2SK1530/2SJ201

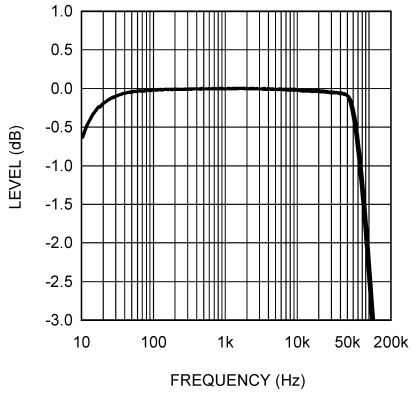

Figure 51. Frequency Response
P_{OUT}/Channel = 100W (0dB), R_L = 8Ω
2SK1530/2SJ201

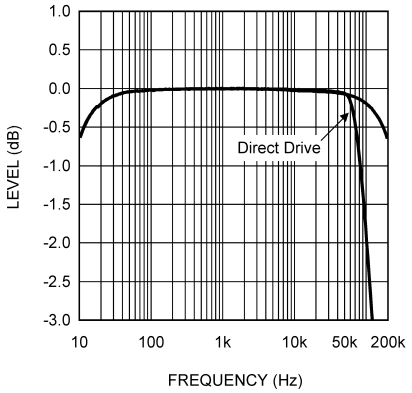

Figure 52. Frequency Response with Driver Stage
P_{OUT} = 60W/Channel (0dB), R_L = 8Ω,
2SK1530/2SJ201

9.6 Slew Rate

The driver stage of Figure 34 was used to compare direct drive of the output stage using the Toshiba 2SK1530/2SJ201 pair. One channel of the amplifier had the driver stage added while the other channel used direct drive from the LM4702 for easy comparison. The output stage in both channels is was biased to the same 145mA. The frequency response graph in Figure 52 compares the two channels delivering 60W of output power into 8Ω resistive loads. The results are similar to those achieved by the other devices with significant improvement in frequency response with a driver stage. The highest slew rate was obtained with the Toshiba 2SK1530/2SJ201 pair using the driver stage. At the same time, the lowest slew rate with direct drive from the LM4702 was obtained with these devices. The channel with a the driver stage has a slew rate of 37.5V/µs compared to 12.5Vµs for the channel with direct drive.

9.7 International Rectifier IRFP240/IRFP9240 Pair

These devices have higher V_T ; therefore, do not meet the bias current criteria of 100mA with a V_{GS} of 3V or less. All other design criteria are exceeded. The testing is included to show what can be obtained with higher V_T devices although they are not optimal for use with the LM4702. Figure 53 , Figure 54 , and Figure 55 show the distortion levels of the harmonics at 1W, 40W, and 100W output power levels, respectively.

Figure 56 and Figure 57 show the performance over the frequency and power range of interest. Figure 56 has a range of 0.0005% to 1% to increase resolution. The 1% power level is 147W/Channel into an 8Ω load.

Figure 58 compares different bandwidth settings on the measurement equipment and the effect on a 1kHz plot during an output power sweep. The difference between the plots and the bandwidth setting shows the increase in THD + N is noise (+N) and not harmonics (THD).

The frequency response at 100W/Channel is shown in Figure 59. The measured slew rate was 14V/µs with the output stage directly driven by the LM4702.

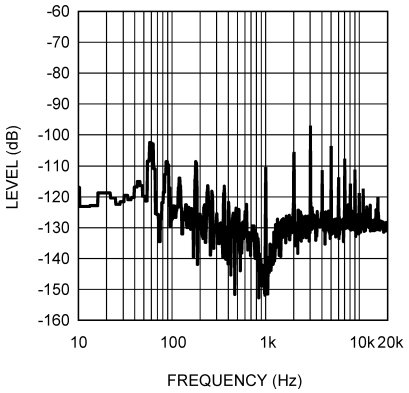

Figure 53. FFT vs Frequency (Reading)
P_{OUT} = 1W/Channel, R_L = 8Ω
IRFP240/IRFP9240

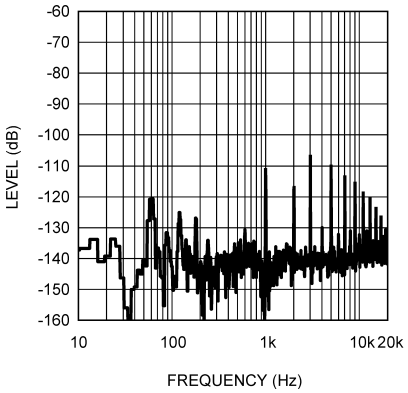

Figure 54. FFT vs Frequency (Reading)
P_{OUT} = 40W/Channel, R_L = 8Ω
IRFP240/IRFP9240

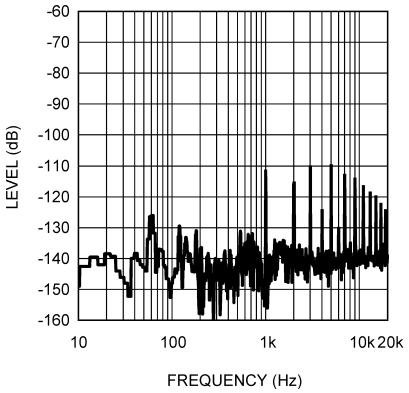

Figure 55. FFT vs Frequency (Reading)
P_{OUT} = 100W/Channel, R_L = 8Ω
IRFP240/IRFP9240

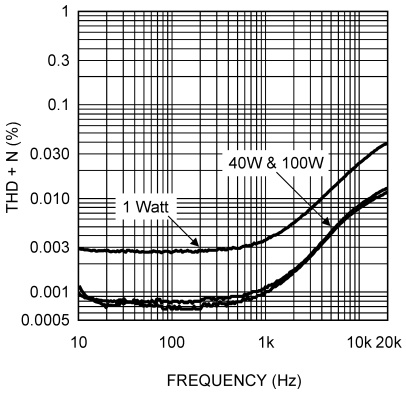

Figure 56. THD+N vs Frequency
P_{OUT}/Channel, R_L = 8Ω, 80kHz BW
IRFP240/IRFP9240

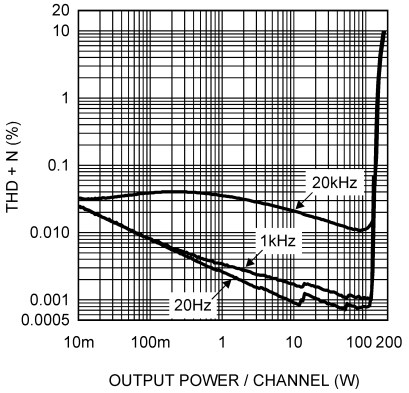

Figure 57. THD+N vs Output Power/Channel
R_L = 8Ω, 80kHz BW
IRFP240/IRFP9240

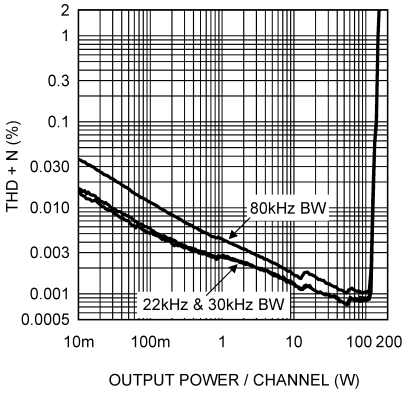

Figure 58. THD+N vs Output Power/Channel
R_L = 8Ω, 1kHz
IRFP240/IRFP9240

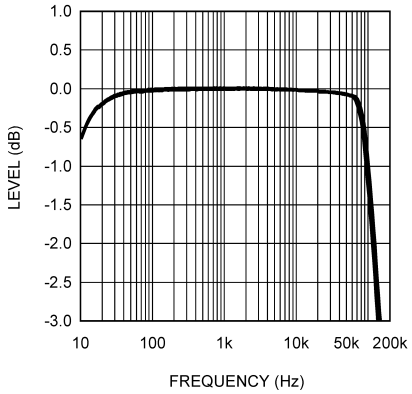

Figure 59. Frequency Response
P_{OUT}/Channel = 100W (0dB), R_L = 8Ω
IRFP240/IRFP9240

9.8 Slew Rate

Adding a driver stage with the IRFP240/IRFP9240 would reduce the already low bias voltage by over 1V. It has been shown with the other pairs of MOSFET devices that adding a driver stage will significantly increase the slew rate. It follows that adding a driver stage with the IRFP240/IRFP9240 devices will result in a significant slew rate increase.

10 Summary

Using the LM4702 and correctly chosen MOSFET devices, a simple yet high performance amplifier can easily be realized. While circuit modifications and additions can improve performance the solution presented has a low part count and simplicity is maintained. Table 5 gives a snap shot look at different data points using the same PCB with a supply voltage of +/-55V driving 8Ω loads.

Table 5. Summary Table

Manufacturer/ Devices	Bias Current	1% Output Power	10% Output Power	1kHz THD+N at 40W/Channel, 22kHz BW	Direct Drive Slew Rate
Renesas 2SK1058 / 2SJ162	115mA	125.5W/Ch.	156W/Ch.	0.00082%	17V/µs
Magnatec BUZ901 / BUZ906	180mA	128W/Ch.	160W/Ch.	0.00088%	16.5V/µs
Toshiba 2SK1530 / 2SJ201	145mA	155W/Ch.	185W/Ch.	0.00071%	12.5V/µs
International Rectifier IRFP240 / IRFP9240	25mA	147W/Ch.	182W/Ch.	0.00090%	14V/µs

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