ADC12EU050

Continuous-Time Sigma-Delta ADCs

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Continuous-time sigma-delta (CTΣΔ) analog-to-digital (A/D) conversion technology shatters the conventional wisdom that pipeline analog-to-digital converters (ADCs) are the only conversion technique available for high dynamic performance, sub-100 MSPS (mega-samples per second) applications. Besides providing more power-efficient operation, CTΣΔ technology also offers unique features that greatly reduce the challenges of deploying such ADCs in high-speed, high-performance systems. In short, CTΣΔ technology means:

- An inherently power-efficient architecture that eliminates the high-speed gain stages required for sampled-input ADCs, such as pipeline or traditional discrete-time (DT) ΣΔ (DTΣΔ) ADCs.
- An essentially alias-free Nyquist band that is made available by exploiting inherent over-sampling, an internal lowpass CT loop filter, and on-chip digital filtering.
- A purely resistive input with no switching, which is easier to drive and couples less noise to the overall system than the switching input capacitors of a sampled-input ADC, such as a pipeline or DTΣΔ ADC.
- An on-chip clock conditioning circuit to provide the over-sampling clock to the internal modulator. This circuit increases the frequency and the quality of the input clock, yielding a low-jitter sampling edge and achieving high-resolution performance without an expensive, high-performance input clock.
- Easier migration to future CMOS process technologies. In a CTΣΔ ADC, the impact of noise and nonlinearity associated with the sampling process is significantly reduced, allowing for the reduced supply voltages required for future CMOS processes.

Taken together, the inherent benefits of CTΣΔ technology and the opportunity to implement an on-chip clock conditioner greatly simplify the signal path design by:

- Reducing power requirements.
- Eliminating the need (or reducing the requirements) for an external anti-aliasing filter.
- Reducing the input driver requirements.
- Mitigating the need for high-quality clock sources without sacrificing performance.

Furthermore, the ability of CTΣΔ ADCs to scale with technology will allow such designs to take full advantage of future CMOS processes.

National's CTΣΔ technology supports high-resolution ADCs up to 16 bits and beyond with data output rates up to 100 MHz. This paper will first review the ADC landscape and explain how CTΣΔ technology is positioned within that space. Next, the details and benefits of CTΣΔ technology as applied to ADCs will be presented, focusing on the advantages and benefits of National's new ADC12EU050 versus competing ADC technologies for high-resolution, sub-100 MSPS applications. Finally, the paper concludes with a summary of the potential of CTΣΔ ADCs.

Data Conversion Fundamentals

ADCs perform two basic, fundamental operations: discretization in time and discretization in amplitude. The two functions are shown conceptually in *Figure 1*, though the actual ADC may not be structured as such.

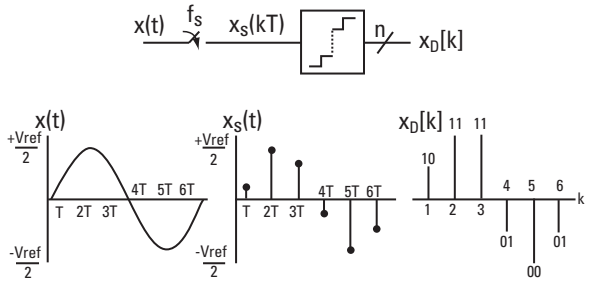

Figure 1: Analog-to-digital conversion

The first operation of the ADC is to discretize in time, or sample, the continually time-varying input analog signal. The input signal is typically sampled at uniformly spaced times at a frequency of f_S, and the samples are thus separated by a period $T_S = 1/f_S$. Once the input signal is sampled, the resultant exists only as impulses at the sampling interval, kT_S. However, this sampled signal is still able to assume an infinite range of values, and therefore cannot be represented precisely in a digital form.

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The second function of the ADC is to discretize the sampled signal in amplitude. That is, the ADC approximates the amplitude of each sample with one of a finite number of possible values. Because the output of the ADC can take on only a finite number of possible values, the amplitude of each sample can be represented by a digital code whose bit length determines the total number of possible converter outputs. The finite number of output values in a converter introduces error into the digital representation of the analog input. This so-called quantization error limits the resolution of the converter.

ADC Architectures

In general, ADCs are divided into two broad categories: Nyquist-rate converters and over-sampling converters. These different converter classes typically offer different compromises between ADC resolution and output sampling rate.

Nyquist-Rate Converters

Nyquist-rate converters are those that operate at the minimum sampling frequency necessary to capture all the information about the entire input bandwidth, and therefore the output data rate of a Nyquist-rate converter can be very high. Three of the most popular Nyquist-rate converters are SAR (successive approximation register), flash, and pipeline ADCs.

SAR ADCs

A successive approximation register (SAR) ADC essentially performs a binary search on the input signal using only a single comparator [1]. That is, the ADC first determines whether the input is greater or less than the midpoint between the reference voltages and the result of that determination is the most significant bit (MSB) in the digital output. The half of the possible values in which the input was not found are then discarded and the ADC next determines whether the input is greater or less than the midpoint of the remaining possible values; the result of that operation is the next bit in the digital word.

This operation continues, approximating the input value with finer resolution each successive cycle, reusing the same comparator each cycle until the least significant bit (LSB) is determined and the digital word is complete. Because the SAR requires N cycles to produce an N-bit resolution output, the speed of state-of-the-art SARs is often limited to several MSPS; however, the accuracy can be high at low power since a single high-resolution (possibly calibrated) comparator can be reused each cycle. National's low-power ADCs employ SAR architectures and achieve up to 14-bit resolution and 1-MSPS operation.

Flash ADCs

A flash ADC features a cascade of parallel comparators connected to a resistor-ladder driven by the most positive and most negative ADC reference voltages [1]. Each resistor-ladder tap is designed to be one LSB away from its neighbors, allowing adjacent comparators to distinguish between inputs that differ by at least one LSB. The outputs of all the comparators form a thermometer code, which is typically converted into a binary-weighted digital output.

For N-bit resolution, 2^N-1 comparators are required for a flash ADC, which limits their applicability to low-resolution applications since every additional bit of resolution doubles the required number and hence, power and area, of comparators [1]. Increased bits also increase the required accuracy of each comparator. For these reasons, flash converters are typically limited to 8-bit resolution. Most design effort in flash ADCs seeks to reduce their power in high-speed conversion by minimizing the number of comparators applied, for example by interpolating and folding designs. National has employed such strategies to realize its industry-leading very low power, gigahertz-rate sampling 8-bit ADCs.

Pipeline ADCs

Pipeline ADCs have become the standard in data conversion applications at 8-bit and higher resolutions for sampling rates from 5 MHz to 100 MHz or more. Indeed, National offers high-speed 8-, 10-, 12-, and 14-bit ADCs based on pipeline architectures that achieve sampling rates up to 200 MSPS and offer very large input sampling bandwidths.

Rather than providing enough comparators to check the input against every possible input value as in a flash ADC, the pipeline architecture employs multiple low-resolution flash conversion stages cascaded in series to form the pipeline. At each stage in the pipeline, the previous stage's quantized output is subtracted from the original input signal and the remainder is sent to the next stage for ever finer quantization [1]. This process is repeated several times as the signal progresses through the pipeline until the LSBs are determined and the output of all the stages in the pipeline are then combined to form the overall digital approximation to the input sample value.

Because the pipeline is able to operate concurrently on many samples, the ADC outputs a complete digital word every clock cycle. This parallel processing allows the pipeline to offer high resolution at the full Nyquist rate of the converter. But the tradeoff for the high output rate is a delay from when the input is first sampled to when its digital approximation is made available. This delay is known as the latency of the pipe, which is typically on the order of ten sample clock cycles. Fortunately for many applications, the latency of a pipeline ADC is acceptable.

Challenges of the Pipeline ADC

As National's high-speed ADC products demonstrate, the pipeline ADC is clearly capable of providing high dynamic performance at sampling rates up to 200 MSPS. Although the pipeline architecture can achieve very high frequency opera-

tion at moderate-to-high resolution, it compromises in other design parameters.

High-Speed Circuits

Because each stage in the pipeline must process the previous stage's output, a constant input during the conversion process is provided in each stage by a sample-and-hold (SHA) circuit [1]. The first-stage SHA must maintain the accuracy of the overall ADC at the full sampling rate, requiring the switched-capacitor circuit to settle within a single clock period [1]. Similarly, the first-stage adder and DAC must be able to settle their outputs within a single period. These speed requirements for the first stage (and to a lesser extent for subsequent stages) typically require large-bandwidth amplifiers and other circuits, which can lead to high power dissipation.

Thermal Noise

The maximum dynamic range of the pipeline ADC is determined at least partly by the thermal noise at the input of the converter, including the kT/C noise of the input sampling capacitor. To reduce kT/C noise, a larger capacitor can be used, but at the cost of increased switching noise at the input and a more difficult-to-drive input, requiring a higher-performance, higher-power ADC driver.

Migration to Future CMOS Processes

As for all sampled-input ADCs, pipeline ADCs are also challenging to migrate to future CMOS processes. This challenge arises from the switched-capacitor input, as a boosted CMOS switch is often used to sample the input signal onto the sampling capacitor. As CMOS processes and their supply voltages shrink, the overdrive voltage available for the CMOS switches also shrinks, greatly reducing the range of input voltages that can be sampled with high resolution. Furthermore, designing switches with reduced threshold voltages that work well in deep sub-micron processes can be difficult.

Input Filtering and Sampling Clock Requirements

A final challenge in using any sampled-input ADC, including pipelines, concerns the external circuitry necessary to drive the converter [2], specifically the input filtering network and the sampling clock. With any sampled-input converter, signals that can be aliased into the band of interest by the sampling operation must be eliminated using an anti-aliasing filter (AAF). Steep filter attenuation characteristics are hard to achieve, leading designers to over-sample the signal of interest. Although over-sampling reduces the range of frequencies that can alias down in-band and hence, lowers demands on the AAF roll-off, over-sampling the ADC wastes the Nyquist bandwidth, which increases system power. In addition, over-sampling increases the processing demands on subsequent digital circuitry.

The sampling clock provided to the ADC is another important determinant of the overall dynamic performance of a sampled-input ADC, especially for high-resolution, high-input frequency applications [2]. The phase noise of a clock source will appear as increased noise at the ADC output and therefore, care must be taken by the system designer to ensure the overall system resolution is not limited by their clock source. Clock quality is especially important for high-speed high-resolution ADCs because the demands on the purity of the clock increase with increasing input frequency and increasing ADC resolution.

It is apparent from the preceding discussion that although they are excellent candidates for high-speed, high-performance applications, pipeline and other sampled-input ADCs do present design challenges for both the ADC designer and the system designer using the ADC. In contrast to these sampled-input ADCs, CTΣΔ ADCs do not require fast-settling circuits or switched capacitors at their inputs and thus avoid the increased ADC power and need for high-performance drivers in high-resolution applications. CTΣΔ ADCs also include significant anti-aliasing filtering, reducing or eliminating the need for an external AAF and preventing the need to waste ADC bandwidth. Finally, CTΣΔ technology is well-suited for migration to future CMOS processes. The advantages of CTΣΔ technology for high-resolution, sub-100 MSPS applications, where both CTΣΔ and pipeline architectures are applicable, is further developed starting on page 5.

Over-Sampling ADCs

Whereas Nyquist-rate converters are generally well suited to achieving moderate resolution at high input bandwidths, over-sampling converters traditionally provided the opposite tradeoff. Over-sampling converters are those for which the sampling frequency is greater than the Nyquist-rate of the input signal bandwidth and therefore, for a given converter sampling rate, the output rate of an over-sampling converter will be lower than that for a Nyquist-rate converter. However, in exchange for Nyquist bandwidth, over-sampling converters can achieve (without calibration) higher resolution than Nyquist-rate converters, regardless of the inherent resolution of the CMOS circuits composing the converter. Two types of such ADCs are over-sampling ADCs and ΣΔ ADCs.

Over-Sampling A/D Converters

Over-sampling an ADC can perhaps best be understood beginning with a review of an N-bit flash ADC whose positive reference voltage is $+V_{REF}/2$ and whose negative reference voltage is $–V_{REF}/2$. The full input range of $[-V_{REF}/2, +V_{REF}/2]$ is subdivided into 2N smaller regions of width one LSB, or $V_{LSB} = V_{REF}/2^N$.

Because the output of the flash ADC assigns only one of a finite set of outputs to an infinite range of inputs, the output digital representation of an input is the sum of the original amplitude plus an error signal due to the digital approximation; this error signal is referred to as the quantization error. Typically, it is assumed that the quantization error power has a white frequency spectrum, distributed equally between all frequencies from 0 to the sampling frequency, fS. The noise power in the ADC output is found by integrating this constant quantization noise density from 0 to fS /2, the Nyquist bandwidth. It can be shown that the SNR in dB of a flash ADC is *SNR = 01.76 + 6N*, where *N* is the number of bits in the output [3].

The preceding discussion concerning the white noise nature of quantization error distributed between DC and f_S /2 suggests a simple way to reduce noise in the ADC output signal. Because the finite-power quantization noise is distributed equally across all frequencies, by restricting the allowable bandwidth of a converter, the total integrated noise in the output can be reduced and hence, the SNR of signals in that bandwidth will be increased. That is, if the input bandwidth is limited to f_S/2M, the total integrated noise will be reduced by a factor of M, known as the over-sampling ratio. Therefore, the achievable SNR in dB of an over-sampling ADC is

$$SNR = 1.76 + 6N + 10\log_{10}(M)$$ [3].

With over-sampling, the SNR increases by one bit (6 dB) for every fourfold increase in M.

Sigma-Delta Modulator ADCs

The efficiency of the bandwidth/resolution tradeoff in over-sampling can be extended by shaping the spectrum of either the input signal or the quantization noise. The former is typically accomplished using a delta modulator, while the latter is accomplished with a ΣΔ modulator [4]. Because ΣΔ modulators are much more robust to circuit non-idealities than delta modulators, they are usually the preferred architecture [4].

The basic principle of operation for a ΣΔ modulator is to enclose a simple quantizer in a feedback loop to shape the quantization noise such that most of the noise is shifted out of the band of interest, where it can later be suppressed by filtering. An example of a simple ΣΔ modulator is shown in *Figure 2*, where the quantizer has been modeled by the additive white noise source, e_i.

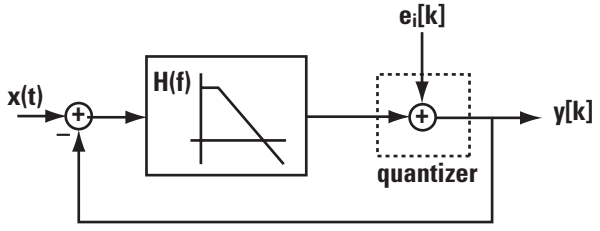

Figure 2: ΣΔ Modulator

Figure 3 shows the transfer function, known as the noise transfer function (NTF), from the quantization noise, e_i, to the modulator output for various loop orders, L [3].

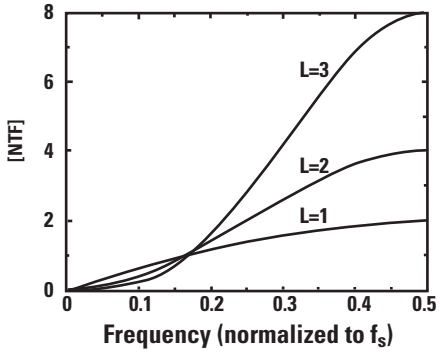

Figure 3: Quantization noise shaping in a ΣΔ modulator

From this figure, it is apparent that the modulator emphasizes the quantization noise at higher frequencies, while suppressing the lower-frequency inband noise. In effect, the quantization noise is shifted to higher frequencies where it can be filtered out later, significantly reducing the total inband quantization noise power in the modulator output. Notice that for higher order modulators, more quantization noise is shaped out of band, leaving less quantization noise inband. However, the loop filter order can not be increased without bound due to the increased difficulty of stabilizing higher-order loops [5].

It can be shown that for a ΣΔ modulator, the achievable SNR in dB is

$$SNR = 1.76 + 6N + (2L + 1)\ 10\log10(M) + 10\log10(2L + 1) - (2L)10\log10(\pi)$$ [3].

Compared to the SNR of a simple over-sampling ADC then, the SNR for a ΣΔ modulator is greater if M>π, which is usually the case. As the over-sampling ratio increases, ΣΔ modulators yield increasingly higher resolution than simple over-sampling. This equation shows that the SNR increase due to the over-sampling ratio is multiplied by *(2L+1)*, and therefore the bandwidth/resolution tradeoff is much more efficient for ΣΔ modulators than for over-sampling alone, especially as the modulator order increases. ΣΔ modulators attain this improved resolution because of the quantization error noise shaping provided by feedback in the ΣΔ loop.

The signal at the output of the quantizer in the ΣΔ modulator contains the input signal and other noise and distortion components in addition to the shaped quantization noise; furthermore, the loop output data rate is M times higher than desired [4]. The final step of the ΣΔ A/D conversion process is to remove the out-of-band quantization noise and downsample the output to the desired data rate: this function is performed by the decimation filter.

Decimation Filter

The digital filter at the output of the ΣΔ modulator must lowpass filter the out-of-band quantization noise and resample the digital data from the loop sample rate, MfS, to f_S, the desired ADC output rate [4]. To reduce implementation complexity, the decimation filter is usually designed in multiple stages [4].

One simple implementation uses a simple accumulate-and-dump or sinc filter as a first stage that is generally limited to a low-order decimation to prevent significant in-band droop; the sinc transfer function prevents signals at multiples of the resampled rate from aliasing down in-band. Such a configuration is then often followed by a lowpass filter that decimates the signal from the intermediate output rate of the sinc-filter to the desired rate of f_S/M. This lowpass filter can also be designed to compensate for the remaining in-band droop of the sinc filter [6]. The decimation filtering in a ΣΔ ADC typically results in longer latencies than those found in a pipeline ADC but many applications can tolerate this increased latency.

Continuous-Time ΣΔ Modulators

The first recognizable ΣΔ modulator, introduced in 1962, was actually implemented as a CT circuit [7]. Indeed, CT implementations of ΣΔ modulators have appeared regularly since then, but when switched-capacitor (SC) circuits were introduced, most ΣΔ modulators were implemented with DT loop filters. SC circuits remain popular because of their insensitivity to signal waveform characteristics. In addition, the time constants of SC integrators scale with sampling frequency, allowing for greater system flexibility [8]. However, interest in CTΣΔ modulators has been renewed because of some of the benefits, such as employing lower-power integrator amplifiers and including inherent anti-aliasing filtering versus sampled-input ADCs [7].

CTΣΔ ADCs differ from sampled-input ADCs, such as pipeline and DTΣΔ ADCs, in two important ways:

- A CTΣΔ modulator uses CT integrators rather than DT integrators or circuits. That is, rather than SC circuits, the CTΣΔ modulator employs continuous-time circuits, often RC or C/gm integrators.
- The sampling operation in a CTΣΔ modulator occurs at the output of the forward loop filter, before the quantizer. In contrast, for a sampled-input ADC, the sampling occurs at the input of the ADC.

These differences between CTΣΔ ADCs and sampled-input ADCs give rise to significant performance differentiation between the two. Specifically, CTΣΔ ADCs operate at lower power, include significant anti-aliasing filtering, and present a much quieter input stage. All of these benefits of CTΣΔ technology are realized in National's new ADC12EU050, as explained in the next section.

Challenges of the CTΣΔ ADC

Of course, as pipeline ADCs offer high speed operation while compromising other design parameters, the benefits of CTΣΔ operation also come at the cost of some design challenges for both the ADC designer and the system architect. A sampled-input, SC ADC can often operate over a wide range of sampling frequencies from near-zero to its maximum rate. However, the dynamics of the CTΣΔ are set by the RC or C/gm product of its component integrators; therefore, the integrator time constants must be tunable to allow for process variation [2]. In addition, the loop dynamics will not scale with sampling frequency, limiting the allowable sampling rate operating range.

The input bandwidth of a ΣΔ is also limited to the ADC's first Nyquist band. In a Nyquist-rate ADC wherein full-rate sampling occurs at the system input, the input bandwidth can be many times larger than the Nyquist rate of the converter, allowing for IF-sampling. Conversely in a ΣΔ ADC, because of the lowpass decimation filtering, signals outside the first Nyquist zone will be removed from the output spectrum. In addition, although a DTΣΔ would allow signals around its loop sampling rate, Mf_S, to fold down inband, the inherent anti-aliasing filtering in a CTΣΔ ADC precludes this from happening. Therefore, input signals must be mixed down into the first Nyquist zone to be digitized by a CTΣΔ ADC.

Finally, because of its over-sampling operation, the output rates of CTΣΔ ADCs are currently limited to less than 100 MSPS while pipeline ADCs are capable of operation up to 500 MSPS and beyond. Indeed, for a given technology, Nyquist-rate converters will always be able to operate faster than ΣΔ ADCs because of the over-sampling necessary in a ΣΔ design.

Fortunately, the benefits of CTΣΔ technology outweigh the drawbacks for high-resolution applications at sampling rates below 100 MSPS. The next section focuses on National's CTΣΔ ADCs, highlighting the performance enhancement achieved versus sampled-input ADCs, such as pipeline and DTΣΔ ADCs.

Advantages of National's CTΣΔ ADCs

National's new ADC12EU050 is the industry's first production-ready CTΣΔ ADC. The product offers performance improvement both because of the inherent advantages of CTΣΔ technology versus sampled-input ADCs and also because of additional circuitry that National has integrated on-chip.

Lower Power

The most significant benefit of the CTΣΔ architecture is its low power consumption relative to comparable sampled-input ADCs in the high-resolution, sub-100 MSPS application space. A common way to compare the performance of ADCs is an energy figure of merit (FOM) which typically measures the ratio of the overall power of the ADC to the resolution and bandwidth of

its output. Aided by the inherent efficiency advantage of CTΣΔ technology, the ADC12EU050 provides excellent performance at extremely low power, yielding an outstanding FOM.

The power advantage of a CTΣΔ implementation arises because of the internal circuitry. In any sampled-input SC circuit – including both pipeline and traditional DTΣΔ ADCs – the internal amplifiers must settle within some target resolution each period. This places significant speed constraints on the internal amplifiers, increasing the power consumption [7] and limiting the maximum achievable sampling rate.

In a CTΣΔ with CT feedback, because the amplifier output never attempts to switch its output voltage instantaneously, there is no output settling required and, hence the amplifier speed constraints are relaxed [7]. Although an exact comparison is difficult, the SC nature of a sampled-input ADC does necessitate higher-speed amplifiers than does a CTΣΔ implementation, leading to higher power dissipation for a pipeline or DTΣΔ ADC in general. The lack of a need for high-speed settling in CTΣΔ ADCs is also the reason they are able to achieve higher sampling rates than traditional DTΣΔ ADCs in a given technology.

Low power, high energy efficiency operation is obviously important for any system but portable devices especially benefit since reduced power extends battery life and reduces heat dissipation, which is particularly important for handheld applications including handheld ultrasound systems. The 1.2-V power supply of the ADC12EU050 also positions the converter well for single battery-powered operation.

Anti-Aliasing Filtering

The CTΣΔ ADC architecture eliminates the need for stringent input filtering because of its inherent anti-aliasing filtering. In the ADC12EU050, many of the performance characteristics of the anti-aliasing filter are set in the digital domain, allowing for a very high level of passband flatness and steep roll-off (high effective order).

The anti-aliasing performance of the CTΣΔ is a result of its implementation as both a ΣΔ modulator and a CT circuit. As is the case for any ΣΔ ADC (CT or DT), the over-sampling and subsequent decimation filtering of the modulator output results in a very sharp roll-off lowpass filter with a cutoff frequency at half the ADC output rate. In contrast, a Nyquist-rate ADC without over-sampling must employ a high-order external lowpass filter before the ADC to prevent signals around multiples of the output sampling rate from aliasing down in-band, as discussed for pipelines in *Input Filtering and Sampling Clock Requirements* on page 3.

However, in addition to the inherent benefit of ΣΔ architectures, the CT offers an additional benefit even over DTΣΔ ADCs. Because the CTΣΔ ADC samples at the output of the forward loop filter, the signal is first lowpass filtered by the loop before sampling, which attenuates signals around the modulator loop sampling rate (Mf_S) that can alias down in-band. Furthermore, because these aliased signals are then injected at the input of the internal quantizer, they are noise-shaped by the loop in the same manner quantization noise is shaped. These two effects enable the CTΣΔ to offer significant anti-aliasing filtering versus the DTΣΔ in addition to the benefits of over-sampling and digital filtering versus a pipeline design. *Figure 4* summarizes the anti-aliasing performance of CTΣΔ ADCs versus pipeline ADCs.

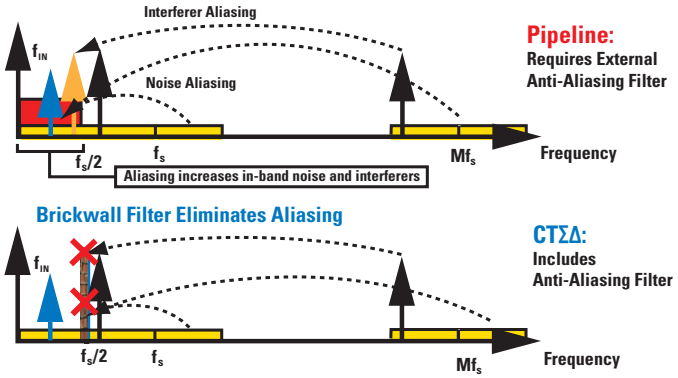

Figure 4: Anti-aliasing performance of CTΣΔ and pipeline ADCs.

This significant inherent anti-aliasing filtering greatly reduces the requirements on or may reduce the need for an external AAF.

The benefit of the anti-aliasing performance of the CTΣΔ cannot be over-stated; the anti-aliasing requirements are dependent upon the application and can be a significant system challenge both in terms of design complexity and overall system form factor and cost. As previously discussed, the anti-aliasing requirements can be relaxed in a pipeline or other Nyquist-rate ADC system by increasing the sampling rate beyond twice the desired input bandwidth but this wastes bandwidth and drives down the overall power efficiency of the system. The design of an analog anti-aliasing filter possessing a steep cut-off characteristic and a very flat passband is a challenging task demanding high-order, potentially high insertion-loss filter networks, which may necessitate additional gain in the signal path to compensate for that loss.

By eliminating the need for additional over-sampling as with a sampled-input ADC, the CTΣΔ allows the system designer to use almost the entire Nyquist bandwidth of the converter, greatly improving power efficiency. Furthermore, by eliminating the need for expensive, lossy external anti-aliasing filters, the ADC12EU050 also reduces the demands on the ADC driver, further reducing system design complexity, cost, and power.

Quiet, Easy-to-Drive Input

The CTΣΔ ADC also offers a much quieter input than a sampled-input ADC because of the CT nature of the internal circuitry. In a sampled-input ADC, such as a pipeline or traditional DTΣΔ ADC, the input stage consists of a switched capacitor that is

usually large to reduce the overall thermal noise of the ADC. Driving this large switching capacitor is difficult, especially in a DTΣΔ whose internal modulator is sampling at several times the output data rate. In addition, the large switching noise from such inputs can couple to a system, reducing the overall system performance. The input voltages that can be applied to a switched-capacitor input are also limited because of the gate-source voltage of the input sampling switches.
As opposed to a SC sampled input, CTΣΔ technology instead presents a constant, resistive input, as illustrated in *Figure 5*.

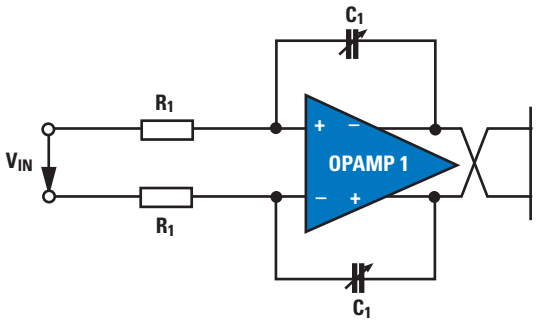

Figure 5: Model of the CTΣΔ ADC input

Because the input of a CTΣΔ is not sampled, there are no switching capacitors and it is easier to drive the input, allowing for the use of cheaper, lower-power driving circuits. In addition, the lack of input switching noise will reduce noise coupling to the system, improving its overall performance. Finally, without any switches at the input to restrict the input voltage swing, the allowable input voltage range can be higher than for a SC sampled-input ADC; indeed, the input voltage can even exceed the supply rails.

Low-Jitter PLL Provides an Accurate Sample Clock

A low-jitter sampling clock is crucial in all high-speed, high-resolution data conversion systems to realize the full resolution of an ADC. The modulator over-sampling clock in National's ADC12EU050 drives the quantizer of the internal ΣΔ loop. This clock is provided by an on-chip clock conditioner, comprising a PLL and VCO. The high-performance PLL uses an on-chip LC-tuned circuit to create a high-Q resonator. This on-chip clock circuit multiplies up the frequency and provides low-jitter sampling edges to the modulator loop, allowing for the benefits of CT ΣΔ ADCs to be realized without requiring a high-performance, high-cost external clock source. The system designer needs simply to provide a moderate-quality, low-cost crystal at the desired output sampling rate (40-50 MSPS), and the ADC12EU050's on-chip clock circuitry takes care of the rest.

A further advantage of the on-chip precision clock is that it can be routed to external circuits and used as a system reference clock for other time-critical parts of the system, potentially eliminating the extra cost of a low-jitter source and saving both design effort and board area.

Instant Overload Recovery

Because the ΣΔ modulator is a feedback loop, it is susceptible to overloading in the presence of large input signals. In a typical ΣΔ modulator, such overloading may require the loop to be reset, losing data previously stored in the loop and causing a large glitch in the ADC output. Instead of resetting the loop, the modulator can be allowed to continue operation, allowing the overload condition to simply work its way out of the loop—but waiting to clear the overload condition can require several clock cycles, during which time the ADC output data is corrupted.

The ADC12EU050 includes circuitry that recovers immediately from an overload condition. When this instant overload recovery (IOR) circuitry is enabled, the ADC maintains signal integrity in the event of an input overload condition, allowing it to recover faster than even a pipeline ADC.

Technology Scaling

Finally, CTΣΔ technology is capable of scaling well with future technologies, ensuring a lengthy presence in the ADC marketplace. As discussed above, because the sampling operation in a CTΣΔ occurs at the output of the loop filter, the performance impact due to errors in the sampling operation will be greatly reduced. In sampled-input ADCs such as pipeline or DTΣΔ ADCs, the sampling occurs at the ADC input and therefore, any sampling errors are significant. It is for this reason that CTΣΔ ADCs are more amenable to future, scaled CMOS processes. Non-idealities in the sampling circuit caused by reduced overdrive, leakage, or other effects in future processes will impact pipeline, DTΣΔ, and other sampling-input ADCs much more than CTΣΔ ADCs.

National's New CTΣΔ ADC

The ADC12EU050 12-bit, ultra-low-power, octal CTΣΔ ADC offers an alias-free sample bandwidth of 20 to 25 MHz and a conversion rate of 40 MSPS to 50 MSPS. The device features 68 dB of signal-to-noise and distortion (SINAD) and a signal-to-noise ratio (SNR) of 70 dB full scale (dBFS). Operating from a 1.2V supply, it consumes 44 mW per channel at 50 MSPS for a total power consumption of only 350 mW, 30% lower than currently available competitive pipeline products (see *Figure 6*).

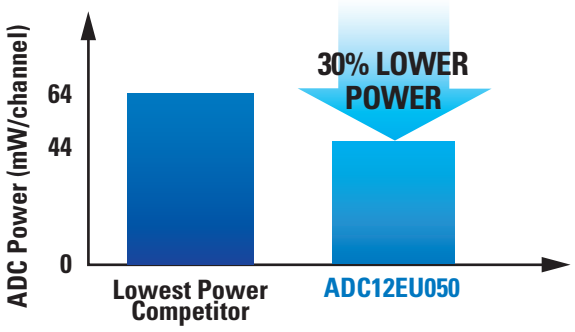

Figure 6: Power Consumption Comparison for ADC12EU050

The ADC12EU050 reduces interconnection complexity by using programmable serialized outputs, which offer industry-standard low-voltage differential signaling (LVDS) and scalable low-voltage signaling (SLVS) modes. The ADC12EU050 operates over the -40 degrees C to 85 degrees C temperature range and is supplied in a 68-pin LLP® package.

Conclusion

National's advanced ADC12EU050 ADC solution finally realizes the leap in performance that CTΣΔ ADCs have promised for more than 40 years, successfully migrating the technology from the research lab to the production line. The power dissipation is 30% lower than for any of the competitive pipeline products and it offers 12-bit resolution at an output rate up to 5 times the fastest currently available DTΣΔ ADC.

The CTΣΔ technology on which the ADC12EU050 is based also offers significant inherent anti-aliasing filtering and provides a low-noise, easy-to-drive input stage. To fully exploit these considerable benefits of CTΣΔ technology, the ADC12EU050 also includes an on-chip clock conditioner that eliminates the need for a high-performance, expensive clock. Finally, the ADC12EU050 avoids the hazards of input overload present in ΣΔ ADCs by offering a means for recovering immediately from an input overload event.

Beyond the ADC12EU050, National is developing additional CTΣΔ ADCs for high-resolution applications at sampling rates below 100 MSPS. Their many benefits and ability to scale well with technology ensure these types of ADCs will find increasing adoption in future systems. National's expertise in CTΣΔ ADCs ensures we will continue to be at the forefront of industry adoption. ■

For more information on CTΣΔ ADCs, visit: national.com/adc

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