Application Report
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EMI Suppression of FPD-Link Device In Automotive Application (II)

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ABSTRACT

Electromagnetic interference (EMI) is a complicated system problem for a vehicle entertainment control unit that uses a high-speed device such as LVDS serializer/deserializer. In such a system, the component-level EMI suppression function is not always sufficient for a robust design. This series of application notes contains two reports to discuss how to reduce EMI of FPD-Link display system in different aspects when using the FPD-Link device from TI. In the first paper, component-level solution spread spectrum clock generation (SSCG) was discussed. This second report focuses on system-level EMI suppression, and presents several practical techniques to solve the EMI issue in the dual-channel FPD-Link LCD displayer. HSPICE and electromagnetic (EM) simulation software are also used.

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1 Introduction

In the automotive industry, it is necessary to view EMI suppression of an electronics module from the entire system level and consider all aspects of the issue. When the EMI issue is addressed in its early stage, higher performance and lower cost are achieved. In the first paper, TI's SSCG, which is a component-level EMI solution in the FPD-Link series products, was thoroughly discussed and validated in a vehicle entertainment terminal by using DS90UH926Q. Although this catalog device has enhanced functions to reduce EMI, it is still not sufficient to pass the EMI test in the case of an unqualified system design. For a design to pass the rigorous automotive EMI special radiated emission (RE) test, a robust PCB design is required. A robust PCB design is a major contribution when combined with SSCG and other component-level suppression functions.

2 Design Consideration of System-Level EMI Suppression

Presently, many LCD panels of vehicle entertainment terminal must be able to accept both DVI and HDMI (HDCP-High Bandwidth Digital Content Protection inside). For such a system, two LVDS deserializers are needed. Typically, DS90UR906Q is recommended as DVI input and DS90UH926Q is recommended as HDMI input. Figure 1 shows a simple block diagram.

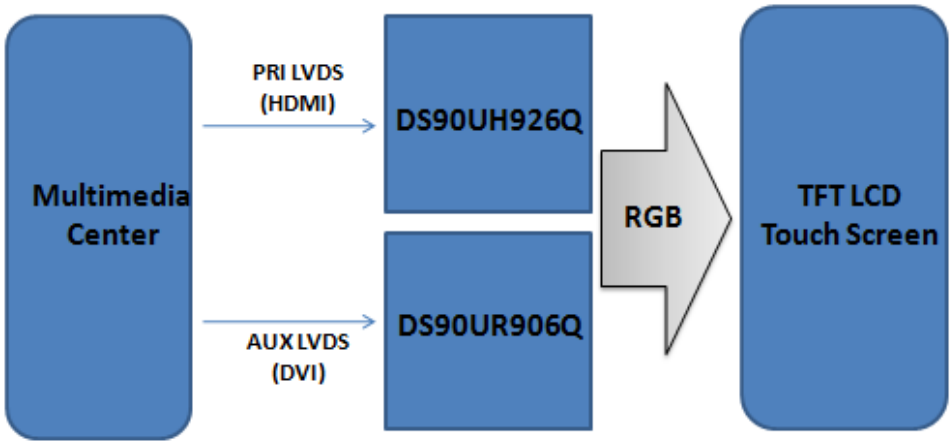

Figure 1. Two Typical LVDS LCD Panels

In this system, the main RE sources should be:

- LVDS interface (high-speed signal path). In DS90UH926Q, PCLK supports 5- to 85-MHz clock. Because LVDS is 35 bits wide (RGB, HDCP, DCA, PCLK), thus, DS90UH926Q LVDS is capable of 175 Mbps to 2.975 Gbps; PCLK of DS90UR906Q supports 5 to 65 MHz and LVDS is capable of 140 Mbps to 1.82 Gbps.
- LVCOMS interface (low-speed signal path), which includes RGB (24 bits), HS (horizontal sync), VS (vertical sync), and PCLK (clock).

This kind of design certainly creates more radiation problems because there are two groups; and therefore, the LVDS and LVCOMS signals must be carefully designed.

3 LVDS Interconnect Design

Based on differential pair technique, LVDS is driven by low differential voltage (300 mV) with the use of current mode driver (soft transitions and reduced spikes). Differential pair also has its own parallel and closing return path. The current (differential mode) flows opposite with the same amplitude, so the differential mode signal offset each. Therefore, low EMI and power is achieved at high-speed data rate. However, there is still common mode signal (V_{CM}) in LVDS (don't carry information). Any change or violation in the PCB interconnect design causes differential to common mode conversion, thus resulting in a common mode RE issue.

To gain the maximum benefits of LVDS in FPD-Link, high-speed PCB and interconnect design is required to provide a low-emission LVDS interface. Several key low-EMI design principles follow:

1. It is of utmost importance to maintain a uniform cross-section down the length of the LVDS trace to provide constant impedance (100Ω). Keeping the trace in the same layer and using fewer vias ensures minimal reflections, distortions, and less EMI.
2. Time delay of the LVDS driver between each line must be matched and each line must have the same length. Any time delay difference between the two lines, or skew between them, causes a differential to common mode conversion.
3. When using an unbalanced cable between serializer and deserializer, CM chokes should be put on the TX and RX sides to filter out common mode radiation caused by common mode signal.

4 Impedance Match of Single-Ended Transmission Line

Normally, an engineer pays more attention for how to deal with the LVDS path and gives less effort to the low-speed path. A low-speed signal is no longer low speed because the rising and falling edge (dv/dt or di/dt) of LVCOMS has entered the world of nanosecond (approximately 1.5 ns for FPD-Link). As the rule of thumb, the edge of a periodic signal is close to ns or less; it must be considered as a high-speed signal and consider potential EMI, noise, simultaneous switch noise (SSN), and so forth.

For single-ended LVCOMS path, because of larger unit interval (UI), less bit error is produced than LVDS if impedance is unmatched. Also, there is more error margin for jitter and ring. However, compared to LVDS, a single-ended signal more easily radiates RF because it has intrinsic disadvantages:

- Larger voltage amplitude than LVDS, typical 3.3 V or 1.8 V for a LVCOMS, while LVDS is 300 mV.
- Does not have its own return path, only refers to the system ground. If an improper ground plane is used, severe PCB radiation occurs. A loop antenna is created by the signal and return path if the return path is not close to the signal path, and a larger loop always means more radiation.

Therefore, in terms of reducing RE, impendance match for single-ended signal path is even more important than LVDS. The severe ring, including overshot and undershot caused by impedance mismatch, is the main RE source for an LVCOMS system.

Like a differential pair, for a complete matched single-ended signal path, the three main factors that must be designed carefully are:

- Source impedance
- Characteristic impedance uniformity of transmission line
- Termination impedance

Ideally, equivalent impedance of the driver and receiver should be designed to 50Ω to match the 50Ω transmission line. However, output impedance of the COMS driver is always from 5Ω to 30Ω due to COMS technology. A series resistor must be added at the output of the driver to achieve 50Ω matching at the driver side. This resistor plus parasitic capacitor of transmission line also acts as a high-frequency attenuator to slow rising and falling edge to ease sharp RE edge.

4.1 IBIS Model: Output Impedance of LVCOMS Driver

Many data sheets of the serializer/deserializer do not provide the LVCOMS driver impedance. The answer can be determined quickly by using the IBIS model. IBIS is a behavioral model that describes the electrical characteristics of the digital inputs and outputs of a device through V/I and V/T data without disclosing proprietary information. IBIS contains inherent impedance information.

Assume the source impedance is R_{OUT}, $R_O = R_S + R_{OUT}$ (R_O is 50Ω, R_S is an added series resistor). So, driving current is about $I_{driver} = V_{DD}/2Z_O$ ($Z_O = R_O = 50\Omega$, assuming the transmission line is terminal matched).

Based on the IBIS pullup and pulldown curve, find the voltage of V_{driver} (driving at the rising and failing edges) correspond to the driving current, get $R_{OUT} = V_{driver}/I_{driver}$. When $V_{DD} = 3.3V$, so $R_{OUT} = 33\Omega$ and $R_S = 17\Omega$. As $V_{DD} = 1.8V$, $R_{OUT} = 30\Omega$ and $R_S = 20\Omega$. R_S must be put as closely as possible to the LVCOMS pin.

4.2 HSPICE Simulation: Impedance Match

In some cases, characteristic impedance of PCB trace is not uniform (with vias or turns) due to layout limitations, and COMS receiver impedance is not very accurate. Under such circumstances, implementing a low-pass filter by adding a capacitor with the proper value right after R_S can help filter out the rings and harmonic. The following simulation by HSPICE and IBIS shows the improvement.

Simulation is under the following conditions:

1. $V_{DD} = 3.3V$ (33Ω internal output impedance); PCLK = 33 MHz (1.5 ns of rising and falling time from the DS90UH926Q data sheet)
2. Using the DS90UH926Q IBIS model and the RLGC model of single-ended microstrip-line (50Ω, FR4 of ε = 4.4, width = 4 mil, thickness = 0.6 mil, height = 2.3 mil, length = 12000 mil)

RLGC model in HSPICE: A transmission line can be represented as an infinite series of cascaded identical 2-port networks by using R (distributed resistance), L (distributed inductance), G (conductance), C (capacitance). See detail in *HSPICE Elements and Device Models Manual.*

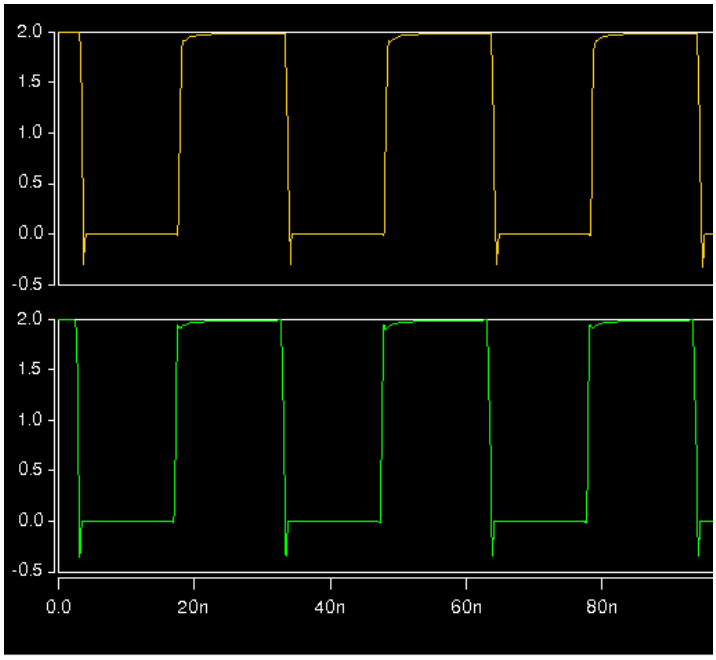

Figure 2. Without RC Filter (Driver Side, Yellow; Receiver Side, Green)

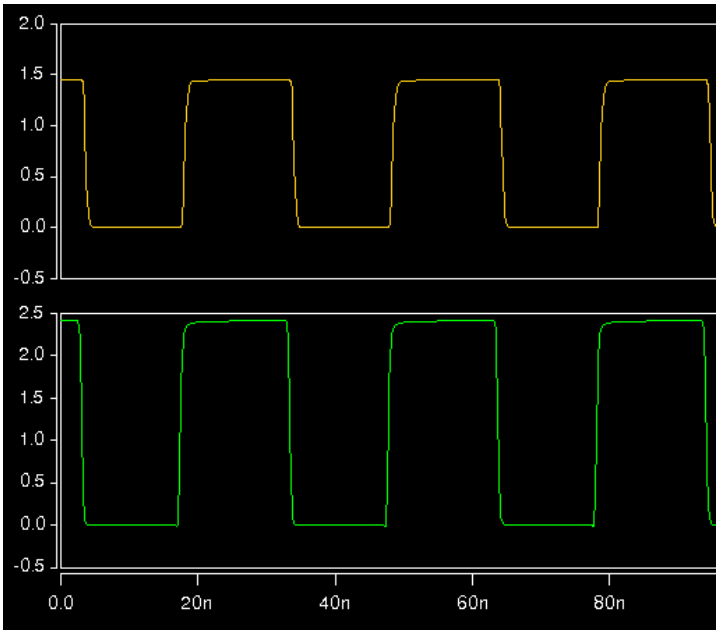

Figure 3. With RC Filter (Driver Side, Yellow; Receiver Side, Green)

Figure 2 shows DS90UH926Q driver 50Ω trace to a 50Ω loading without the output RC filter, square waveform has a 0.4-V undershot at the driver and receiver sides, which results in harmonic radiating.

After adding a 17Ω series resistor so that 33Ω driver is matched to 50Ω, and also puting a 5-pF capacitor with the resistor, undershot is gone at both sides, as shown in Figure 3. At the same time, swing at the receiver side increases to 2.5 V.

Sometimes, to get sufficient swing at the receiver side it it necessary to add a larger value resistor (according to Thevenin theorem); however, it this results in a mismatch at the driver side. Add a capacitor with the proper value to ease the rings.

5 Transmission Lines Stub Effect

To fan out the signal to reach multiple termination, a branch (stub) is often added to a uniform transmission line. The stub breaks the signal intergrity on both paths and brings many reflections (RE) on the driver, receiver, and interconnection of the branch. To determine the impact of the stub on signal quality, the two main factors are the length of the stub and the rising time of the signal.

As a rule of thumb, if the stub length is shorter than 20% of the rise time, the impact from the stub may not be important; however, if the stub is longer than 20% of the rise time, it may have an important influence on the signal. The impact from the stub is too complicated to be analyzed for all the reflections must be considered. The practical way to evaluate the impact of a stub is by using a simulation tool (HSPICE, IBIS, or others).

In the 2-channel LVDS FPD-Link receiver system, DS90UR906Q and DS90UH926Q share one RGB path to the only LCD panel, thus LVCOMS traces of one device is the stub relative to the path of the other device. For example, when a user turns on the PRI LVDS channel to receive an HDMI signal, the AUX channel is powered down and the AUX path acts as an open stub for the signal path of DS90UH926Q, and vice versa when the AUX LVDS channel is turned on.

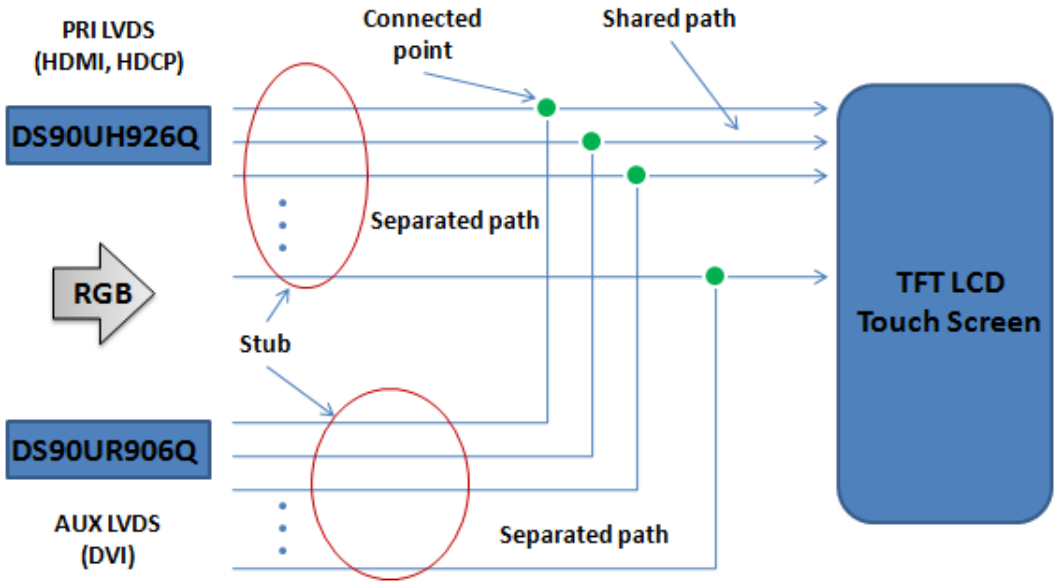

Figure 4. Stub In Dual-LVDS System

5.1 HSPICE Simulation: Stub Effect

In terms of signal integrity, this kind of configuration destroys each signal path and causes radiated emission (rings) at both the receiver and transmitter sides. More importantly, the open stub acts as an antenna to radiate RF. In Figure 5, HSPICE simulation shows the distorted signal at the end of the stub (yellow), driver (purple), and receiver (green). The distortion at the end of the stub has the largest overshot and undershot (about 1 volt) compared to the driver and receiver sides. Obviously, the open circuit stub tends to radiate more RF than the driver and receiver.

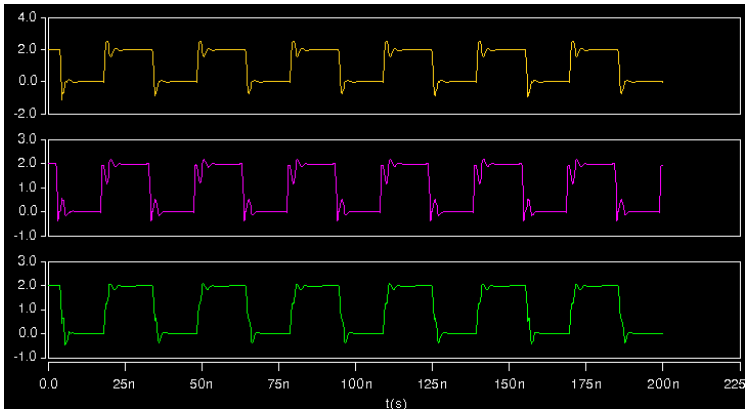

Figure 5. Stub Influence Simulation In HSPICE

Ideally, the stub interconnection should be as short as possible to minimize the stub impact. However, because there are so many LVCOMS signal paths (more than 20 for each deserializer device) that must be dealt with and PCB layout limitations (other external components around a device prevent short paths, although more layers can make short traces occur, but also mean higher cost), it is difficult to shorten all of the traces of the branch.

The practical trade-off to all the preceding factors is to add a pulldown resistor at the LVCOMS pin to absorb the radiation energy. To have enough attenuation and match the transmission line, the resistor should be 50Ω. It is acceptable to add such a small pulldown resistor at the LVCOMS driver side when it is powered down; however, this small pulldown cannot drive enough voltage to the input of LCD when this driver is powered on. As a compromise, $1K\Omega$ is used.

5.2 Stub Effect Reduction

Because in all LVCOMS signals of DS90UH926Q or DS90UR906Q, PCLK is the primary RE source, take PCLK trace design from a real case, for example. As shown in Figure 6, port 3 is the PCLK output of DS90UH926Q, port 1 is the PCLK output of DS90UR906Q, and port 2 is the input of the LCD panel.

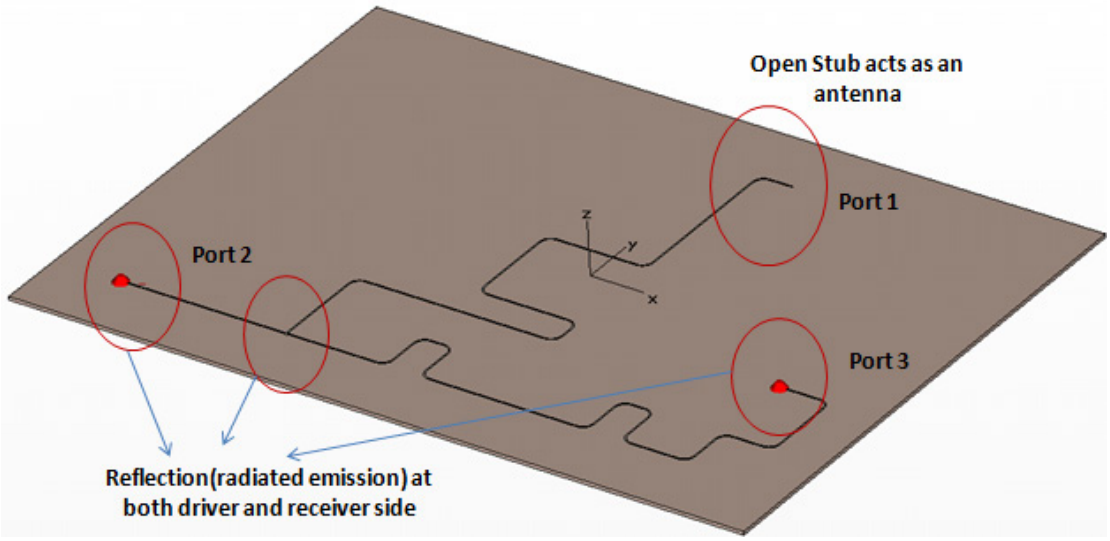

Figure 6. PCLK Trace Modeling In CST

This simulation is done in CST (MICROWAVE STUDIO), which is a popular EM simulation software, by using Finite Difference Time Domain (FDTD). The PCB trace is a 50Ω microstrip (a ground plane is under the trace); a 50Ω resistence is loaded at port 2 to simulate ideal LCD panel input impedance. Port 3 is excited by Gaussian pulse to simulate the PCLK. Gaussian pulse is a typcal excitation that calculates all frequency responses, including a square wave clock. Port 1 simulates another turn-off PCLK (another device), thus, the trace of port 1 is a stub. Refer to the trace from port 3 to port 2. Different value resistances are put at port 1 to simulate how RE of this stub varies with different loading.

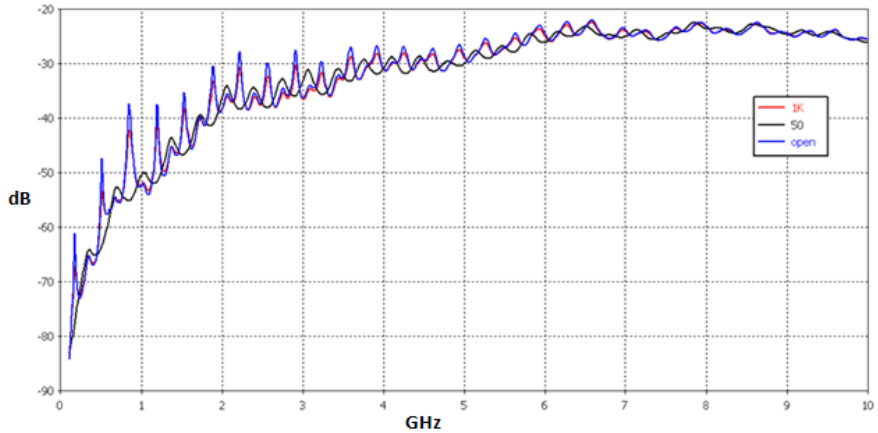

Figure 7. PCLK Stub RE Simulation In CST

Figure 7 shows the RE result of this PCB with different loading at port 1 (open, 50Ω, $1K\Omega$). In the high frequency (freq > 7 GHz), the EM radiation is almost the same with different loading. However, in the low frequency (freq < 3 GHz), the change is obvious; 50Ω can do the best match and filter out peak RE as expected, and $1K\Omega$ brings about 5 dB decreasing from the peak (open stub). Although adding $1K\Omega$ cannot attenuate all harmonics, it still has a 5-dB improvement, which might be enough to pass the final RE test.

6 Conclusion

Because EMI suppression is a complicated system problem, this application report discusses how to implement several practical system-level solutions in a dual-channel FPD-Link LCD displayer. RE reduction is achieved through source impedance matching and demonstrated by HSPICE and the IBIS models. Also, to estimate the PCB stub radiation effect, EM software is used to simulate EMI in real system design. Engineers can use these effective solutions during design to address these issues, which apply to most LVDS systems and are not limited to FPD-Link products.

7 References

1. *EMI Suppression of FPD-Link Device In Automotive Application (I)* , SNAA204
2. *HSPICE Signal Integrity Guide, Release W-2004-09, September 2004*
3. *HSPICE Elements and Device Models Manual, Release W-2004-09, September 2004*
4. *IBIS Cookbook for v4.0 (Sept 16, 2005)*

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