Application Report
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Designing 4- to 12-GHz Direct Conversion Receiver With LMX8410L IQ Demodulator

Hao Zheng

ABSTRACT

For C- and X-band applications, a direct conversion receiver has many advantages over other types of receivers. This receiver is flexible, highly integrated, cost-effective, and free of image signals. The core component of a direct conversion receiver is an IQ demodulator that can directly convert a RF signal to DC-centered complex baseband. This application report discusses when to choose a direct conversion type and why, what to consider when choosing an IQ demodulator, the performance of LMX8410L, and how the device compares to others.

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1 Receiver Architecture Overview

1.1 Traditional Superheterodyne Receiver

A typical traditional superheterodyne receiver (Figure 1) employs two stages of down-conversion, due to the tradeoff between image rejection and channel selection.

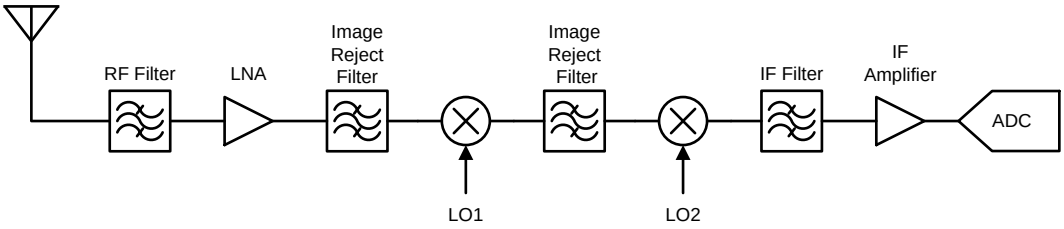

Figure 1. Traditional Superheterodyne Receiver

The traditional superhet is reliable and has been used for decades. However, a traditional superhet receiver suffers from image problems and requires multiple bulky off-chip filters for image suppression. The system is therefore usually over-sized, inflexible, and difficult to integrate. For modern applications that require high integration and flexibility, this type of architecture is typically not suitable.

1.2 Modern Heterodyne Receivers

Modern heterodyne receivers avoid using passive off-chip filters. However, the RF pre-select filter preceding the LNA is usually kept to limit noise power bandwidth, provide preliminary filtering, and serve as image reject filter for the first IF.

1.2.1 Zero Second-IF and Sliding-IF Receiver

Zero-second IF architecture (Figure 2) uses a quadrature down-conversion to remove the image from the second IF without the need for an image reject filter.

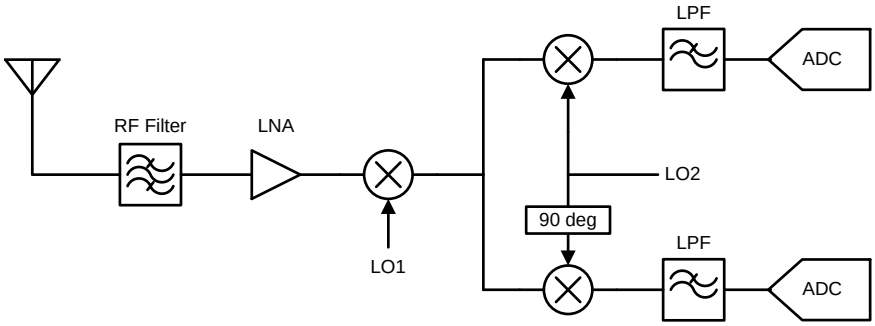

Figure 2. Zero Second-IF Heterodyne Receiver

The basic idea of quadrature down-conversion is that the cos and sin of the LO effectively form a complex exponential. According to Modulation Property of Fourier Transform, this complex exponential moves the signal band from RF to DC. Now the signal band is the same from DC – BW/2 to DC + BW/2, and only low pass filtering is required. The two ADC channels for I and Q paths sample data from DC to DC + BW/2 separately, and digital processing can fully recover the signal.

Quadrature down-conversion theoretically removes the image, but in reality, how well the image is rejected depends on whether or not the I and Q channel outputs match. Since IF is centered at DC, RF = LO, and the image of the signal is a flipped version of signal itself. If the image rejection is not adequate, the signal can corrupt itself.

A modern zero second-IF heterodyne receiver divides down the first LO to form the second LO so that only one synthesizer is required. This type of structure is called a 'sliding-IF receiver' [1].

1.2.2 High-IF Heterodyne

Figure 3 shows a receiver that can directly sample the signal at a relatively high IF frequency. In this example, the tradeoff between image rejection and channel selection for traditional superhet is eliminated and the second mixing stage is no longer required.

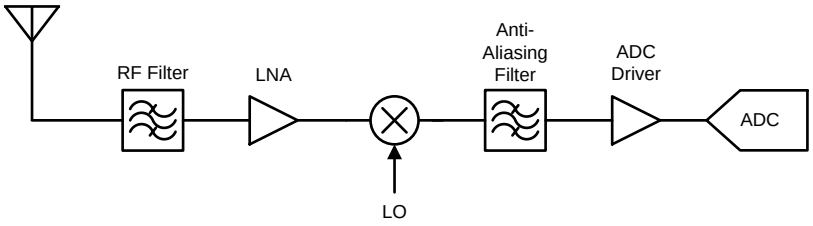

Figure 3. High-IF Receiver

With this architecture, however, the signal quality is very sensitive to spurs that are aliased into a signal band by ADC. The combination of LNA and mixer generates mixing spurs, harmonics, and intermodulation products that range from very low to very high frequency. On the other hand, an anti-aliasing filter can be used before ADC, but this off-chip bandpass filter will take up more board space and make the system inflexible.

This type of receiver still suffers from the first mixing stage image, and sampling at high frequencies can lead to high ADC cost and low ADC performance.

1.3 Direct Conversion Receivers

Figure 4 shows a direct conversion receiver that can directly convert the signal from RF to DC using a quadrature down-conversion.

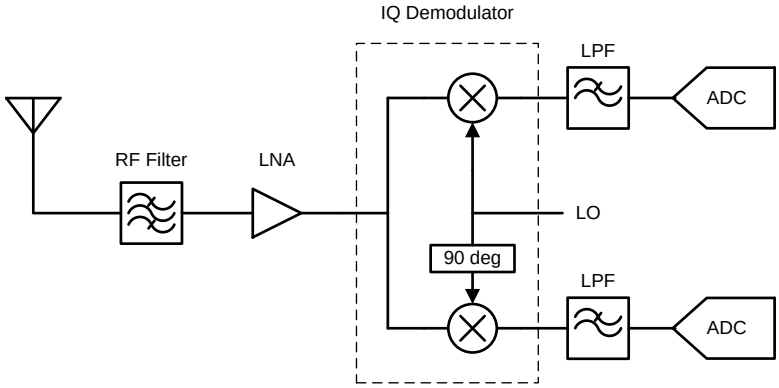

Figure 4. Direct Conversion Receiver

For C- and X-band applications, a direct conversion receiver is usually preferred over heterodyne receivers.

The advantages of a direct conversion receiver over a zero-second IF heterodyne receiver are that a direct conversion receiver can remove the first mixing stage and is free of mixing spurs and image signals, which can greatly simplify the design process and improve signal quality.

Compared to a high-IF heterodyne, a direct conversion is free from images. A direct conversion also has the following advantages:

1. Spur management and interference aliasing:

   As mentioned earlier, the designer must check all of the spurs in the entire frequency range of high-IF heterodyne receivers, because the spurs could be aliased as part of the signal band. An anti-aliasing filter can be bad for integration and system flexibility, but a direct conversion only requires a low pass filter to filter out any aliasing interference.
2. System flexibility:

   Without image signals and mixing spurs, a direct conversion receiver can be very flexible. A designer can easily change the LO/RF frequency without affecting other parts of the system.
3. ADC performance:

   A direct conversion receiver samples signals at DC, so the input frequency to ADC is very low. For a typical ADC, the SNR (Signal to Noise Ratio) and SFDR (Spurious Free Dynamic Range) drop with the increase of input frequency. Therefore, the best ADC performance is used in direct conversion receivers.

1.4 Direct Sampling Receivers

Figure 5 shows a direct sampling receiver the does not require any frequency mixing stage. Most of the work can be done in digital processing, which makes this receiver more flexible and reliable.

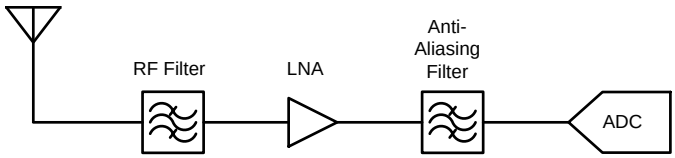

Figure 5. Direct Sampling Receiver

With today's ADC technology, however, direct sampling receivers are mostly limited to L band and S band applications, and as the RF frequency goes up, the price increases and the ADC performance drops quickly.

1.5 Low IF Receiver

A low IF receiver has the same structure with direct conversion receiver. The only change is that the IF is moved from DC to a lower frequency to avoid the drawbacks of working at DC, mainly the DC offset and 1/f noise from IQ demodulator.

However, a low IF receiver typically has a much higher requirement for IRR (Image Rejection Ratio). This is because the image is no longer the flipped version of signal itself, or there could be some out-of-band interferers that may have much higher power than the signal, and therefore must be sufficiently suppressed.

1.6 Summary of Receiver Architectures

As discussed above, direct conversion is usually a better choice compared to heterodyne receivers for C-band and X-band applications. Direct conversion is flexible, free from image signals, highly integrated, and requires less filtering. The comparison between direct conversion and direct sampling is done in the next section, and the focus is on 4-GHz through 12-GHz applications.

2 Comparison Between Direct Conversion and Direct Sampling

2.1 RF Frequency, Signal Bandwidth and Cost

The RF frequency and signal bandwidth decide which type of receiver is suitable for the application. In general, direct sampling is limited to low-frequency applications. For C-band and X-band systems, direct conversion is usually a better choice.

For example, if the RF frequency is 6 GHz and the signal bandwidth is 120 MHz, then the sampling rate of ADC must be at least 4040 MSPS to sample RF directly, assuming that it operates in the 3rd Nyquist zone. In this example, the ADC has a bandwidth of 2020 MHz, but the signal only uses 120 MHz. 94% of its bandwidth is wasted and only 6% is utilized. This is clearly an overkill, especially considering that 4-GSPS ADCs are expensive. On the other hand, direct conversion can fully use the ADC bandwidth because IF is centered at DC.

In the same example, if direct conversion is used, then the two quadrature outputs are both from DC to 60 MHz. Therefore, only a dual-channel 120-MSPS ADC is required. See Table 1 for the comparison.

Table 1. Example for Direct Conversion and Direct Sampling Comparison

ARCHITECTURE	RF FREQUENCY	COMPLEX SIGNAL BANDWIDTH	REAL SIGNAL BANDWIDTH	ADC SAMPLING FREQUENCY	ADC BANDWIDTH UTILIZATION	ADC NYQUIST ZONE	ADC SNR	ADC SFDR	ADC COST
Direct Sampling	6 GHz	120 MHz	120 MHz	4040 MSPS	6%	3rd	Poor	Poor	High
Direct Conversion	6 GHz	120 MHz	60 MHz	120 MSPS	100%	1st	Excellent	Excellent	Low

Through this example for C-band and X-band applications, if the signal bandwidth is not comparable to ADC sampling frequency, then the majority of ADC bandwidth is wasted and direct sampling is an overkill. Table 1 also indicates that in direct sampling, ADC SNR and SFDR are very poor compared to direct conversion. This is discussed in Section 2.2

2.2 Nyquist Zone and ADC Performance

As mentioned in the previous example, one major drawback of direct sampling is that the ADC must usually operate in higher orders of Nyquist zone. However, performance of ADC in 2nd or 3rd Nyquist can be much worse than that in the first Nyquist. In fact, the noise and linearity performance drop quickly with the increase of input RF frequency.

Direct conversion, on the other hand, always operates ADC in the first Nyquist zone and at the lowest possible input frequency, where the ADC performance is the best. For that reason, direct conversion has significantly better ADC performance than direct sampling in C-band and X-band applications.

2.3 Interference and Filtering

In direct conversion receivers, the RF filter is used for pre-selection and noise power bandwidth limitation. In direct sampling, however, the RF filter must also clean up interference in alias bands of the ADC. Therefore, the RF pre-select filter itself may not be adequate, and an extra stage of filtering is usually required (see Figure 5). This is called an anti-aliasing filter [3]. The filter is placed after the LNA to also suppress the distortions and harmonics produced by LNA. This requires a sharp roll-off, which can be difficult to implement at high frequency.

Direct conversion, on the other hand, does not have similar problems. The ADC input is at baseband, and a low pass filter can easily clean up the interference in alias bands.

2.4 Implementation Challenges

Ideally, the IQ demodulator can remove the image signal completely. In practice, however, exact matching between I and Q channel is not achievable in analog design, and the Image Rejection Ratio indicates how well the image signal is suppressed.

This type of implementation challenges limit the performance of IQ demodulators. Other design difficulties include DC offset, 1/f noise, LO leakage to antenna, even-order distortion, and mixing spurs.

However, as we will see in the next section, with the high-performance IQ demodulator LMX8410L, these implementation difficulties will cause minimum trouble to the system, and will be negligible for most applications.

3 Implementation Challenges for IQ Demodulator and Performance of LMX8410L

As discussed in the previous section, the biggest implementation challenge for the IQ demodulator is the limiting factor of direct conversion. The design challenges include: DC offset, 1/f noise, LO leakage to antenna, even-order distortion, mixing spurs, and IQ imbalance. This section discusses each of these challenges and examines the performance of LMX8410L.

3.1 Brief Introduction to LMX8410L

The LMX8410L is a high-frequency IQ demodulator primarily aimed at direct conversion applications. See *LMX8410L High-Performance Mixer With Integrated Synthesizer* (SNAS730) for more information.

The RF frequency range of LMX8410L is between 4 GHz to 10 GHz, and the upper limit can potentially go up to 12 GHz. The IF bandwidth is from DC to 1350 MHz, which means that the available complex gain bandwidth is 2.7 GHz from –1350 MHz to +1350 MHz.

The LMX8410L integrates a low-noise RF synthesizer that serves as the internal LO. The internal synthesizer can be powered down and bypassed if an external LO is preferred. In other words, the LMX8410L supports both internal and external LO mode. The integrated LO can be phase synchronized among multiple devices, which makes the LO a valuable feature in many applications.

3.2 DC Offset

Several mechanisms can cause severe DC offset at the output of an IQ demodulator[2]. Although DC component by itself does not affect signal quality, a large DC offset could saturate the baseband circuits and degrade system dynamic range.

An AC-coupling capacitor or High Pass Filter (HPF) is usually not the best choice for DC offset cancellation. If the stopband of the HPF is too wide, it filters out useful signals. If the bandwidth is too narrow, it requires a large capacitor. As a result, the HPF responds slowly to an abrupt change at the input, and could fail to block the DC component. A sudden transition in DC offset may occur when LO frequency varies or LNA gain changes.

For LMX8410L, however, the DC offset is not an issue. TI provides automated DCOC (DC Offset Correction), which automatically corrects DC offset. The corrected DC offset achieved is less than ±2 mV.

3.3 1/f Noise

The 1/f noise of IQ demodulator adds extra noise to the signal. To quantify the penalty of 1/f noise, Flicker Noise Penalty is defined as the ratio of total noise power (P_{n1}) and noise power with the absence of 1/f noise (P_{n2}), integrated from $f_{BW}/1000$ to f_{BW} [1]. Use Equation 1 to calculate the Flicker Noise Penalty.

$$\frac{P_{n1}}{P_{n2}} = 1 + (5.9 + ln\frac{f_c}{f_{BW}})\frac{f_c}{f_{BW}} \quad (1)$$

where

- P_{n1} is total noise power
- P_{n2} is noise power with the absence of 1/f noise
- f_{BW} is signal bandwidth
- f_c is the corner frequency where 1/f noise power equals thermal noise power

The f_c of the LMX8410L is less than 200 kHz. Consider the case where signal bandwidth (real bandwidth) is 10 MHz. The Flicker Noise Penalty is 1.04 when f_c = 200 kHz, which means that the 1/f noise only adds a little extra noise to the signal. On the other hand, the flicker noise penalty is 16.4 if the signal bandwidth is 100 kHz, which means the 1/f noise is dominating [1].

Therefore, for wide-band applications where signal bandwidth is greater than 10 MHz, the 1/f noise of LMX8410L adds negligible penalty. For narrow-band applications, low-IF receiver should be considered.

3.4 LO Leakage to Antenna

In a transceiver where the receiver and transmitter share the antenna, the LO component can be leaked to the RF port then back to the antenna, where the LO may be transmitted in transmitter mode. For this reasoning, isolation from LO to antenna is required. Typical acceptable values range from –50 to –70 dBm measured at the antenna [1].

The LMX8410L LO to RF leakage is below –52 dBm at 6 GHz with the internal LO enabled. Figure 6 is a typical performance plot that shows the extremely low LO leakage of LMX8410L. A typical LNA provides reverse isolation of at least 30 dB. In this case, the LO leakage at the antenna will be well below –70 dBm.

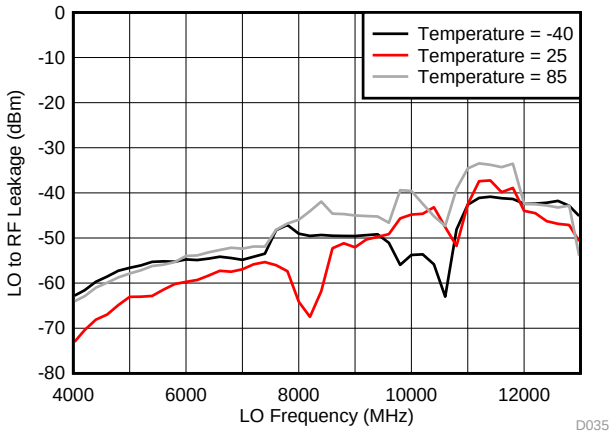

Figure 6. LO to RF Leakage Level: Internal LO Mode

3.5 Even-Order Distortion

IIP2 (Input-referred second order Intercept Point) is a measure of distortion due to second order intermodulation. High IIP2 means that higher input power is allowed without raising any beat frequency spurs above noise floor. The requirement of IIP2 depends on the type of application [6].

IIP2 of LMX8410L is above 46 dBm at 6 GHz. Figure 7 shows the IIP2 across LO frequency when IF = 65 MHz.

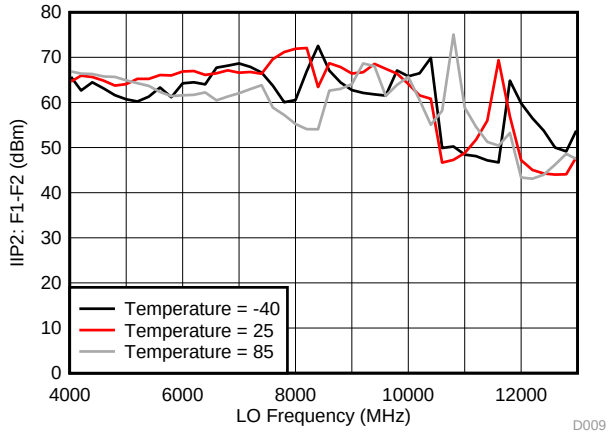

Figure 7. IIP2: F1-F2 Across LO Frequency for Internal LO Mode

3.6 Mixing Spurs

Mixing spurs refers to the mixing products of RF and LO harmonics. For example, a 2x2 spur is the mixed product of the second RF harmonic and the second LO harmonic. Therefore the 2x2 mixing spur frequency is twice the IF frequency. For wide band applications, a 2x2 spur or 3x3 spur may fall into the IF band. For the LMX8410L, however, mixing spurs are not a concern. In fact, the mixing spurs from the LMX8410L are almost negligible. Figure 8 and show the 2x2 and 3x3 mixing spur level (in dBc) versus frequency, respectively.

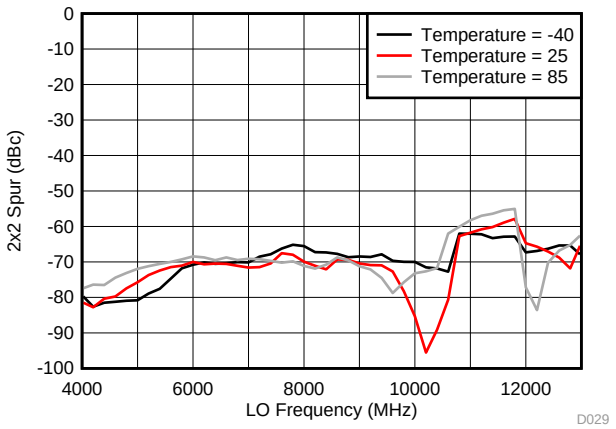

Figure 8. 2x2 Spur for Internal LO Mode

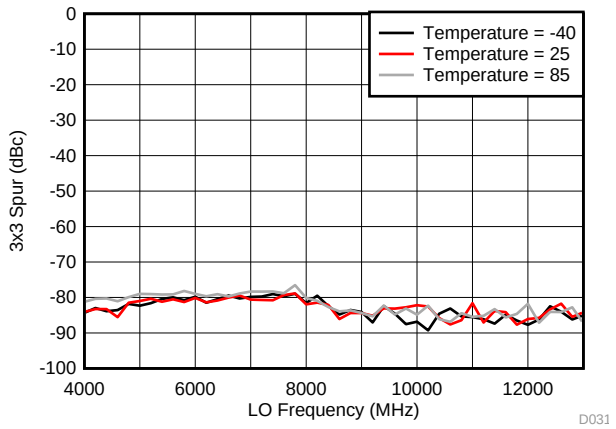

Figure 9. 3x3 Spur for Internal LO Mode

3.7 IQ Imbalance

In previous sections, it is mentioned that the imperfect image rejection of real-world IQ demodulator is due to a mismatch between I and Q channels. This mismatch is often called an IQ channel imbalance. More specifically, there are gain imbalance and phase imbalance that are used to describe the mismatches in gain and phase. Equation 2 defines the spec 'IRR' or 'IMRR' (Image Rejection Ratio) to quantify the relationship between IQ imbalance and image rejection [1][7].

$$\mathrm{IRR} = \frac{\gamma^2 + 2\gamma\cos\Delta\theta + 1}{\gamma^2 - 2\gamma\cos\Delta\theta + 1} \tag{2}$$

where

- gamma is the IQ gain imbalance defined as the ratio of I and Q output voltage
- $\Delta\theta$ is the phase error between IQ phase difference and 90 deg
- 10logIRR is used to calculate IRR in logarithmic scale.

IRR/IMRR quantifies the equivalent image level compared to the signal power. For example, if the IRR is 20 dB, then the image power is 20 dB lower than the signal after digital processing. From another point of view, the IQ mismatch impacts the EVM (Error Vector Magnitude) [1] [8].

The requirements for IRR are usually high, and can be very difficult to achieve in analog design. Therefore, the LMX8410L has the capability to tune the gain and phase of IQ channel individually to help compensate for analog mismatches.

The calibration step size for gain is 0.05 dB, and the step size for phase is 0.25 deg or 0.45 deg depending on which mode is selected. The calibrated IRR of LMX8410L is above 44 dB when RF is 6 GHz and IF is 65 MHz. Figure 10 shows the calibrated and uncalibrated IMRR versus LO frequency when IF equals 65 MHz. Note that positive and negative IRR / IMRR are used interchangeably.

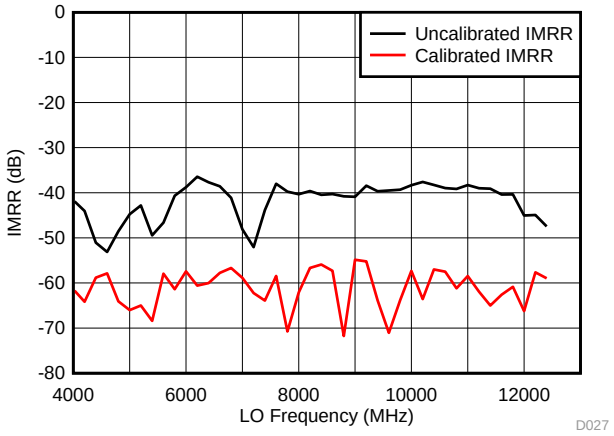

Figure 10. IMRR for Internal LO Mode: Calibrated and Uncalibrated

Although LMX8410L provides calibration to compensate for IQ mismatch, some applications with strict EVM requirements may find this compensation not enough, and a much higher IRR may be required. In that case, additional power-on or continuous digital calibration can be used. Refer to the *Direct Down-Conversion System With I/Q Correction* (SLWU085) for the detailed descriptions of IQ mismatch correction using FPGA.

4 Key Specs and Overall Performance Evaluation for Mixers

NF (Noise Figure), conversion gain, and IIP3 (Input-referred third order Intercept Point) are the key specs for a mixer. These specs are used for mixer performance evaluation.

4.1 Noise Figure

Noise figure is defined as SNR (Signal to Noise Ratio) at the input divided by SNR at the output, when environment temperature is 290K. Y-method is used for LMX8410L noise figure measurement. The LMX8410L typical performance plot of NF is shown in Figure 11. At 6 GHz, the noise figure is below 16 dB.

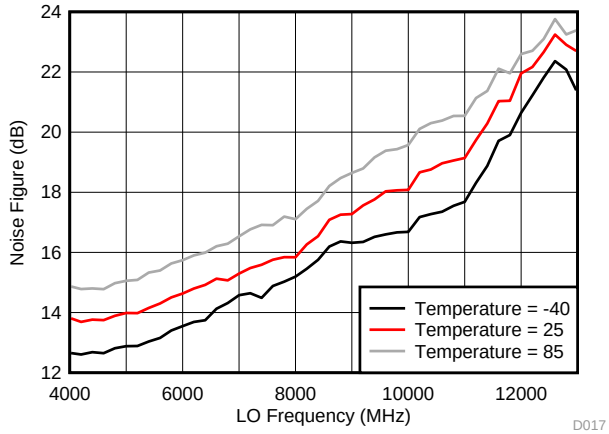

Figure 11. Noise Figure Across LO Frequency for Internal LO Mode

4.2 Conversion Gain

Voltage gain is used for characterization of LMX8410L to avoid confusion, because the input and output impedances are not the same, and because in practice, the following IQ demodulator stage may have capacitive input impedance if the LMX8410L directly drives the ADCs. The voltage gain of LMX8410 versus LO frequency is shown in Figure 12.

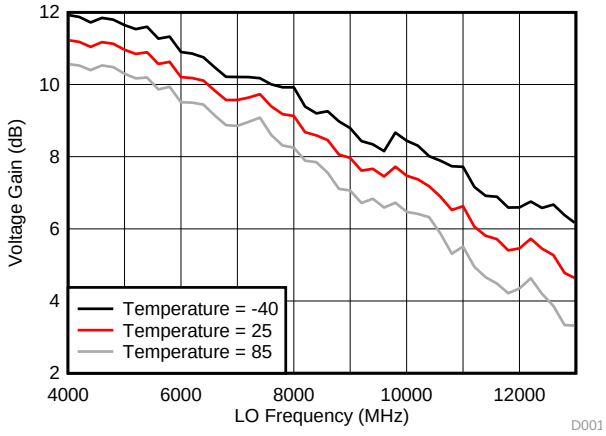

Figure 12. Voltage Gain Across LO Frequency for Internal LO Mode

4.3 IIP3 and OIP3

IIP3 is a measure of linearity with respect to input power. It is defined as the input power level when the power of IM3 (third order intermodulation product) equals the power of the fundamental tones. Use Equation 3 to calculate the IIP3.

$$P_{IIP3} = P_{in} + \frac{P_{out} - P_{IM3,out}}{2} \tag{3}$$

where

- P_{in} is the input tone power
- P_{out} is the power of fundamental tone at the output
- $P_{IM3,out}$ is the power of IM3 at the output

The IIP3 of LMX8410L across LO frequency is shown in Figure 13.

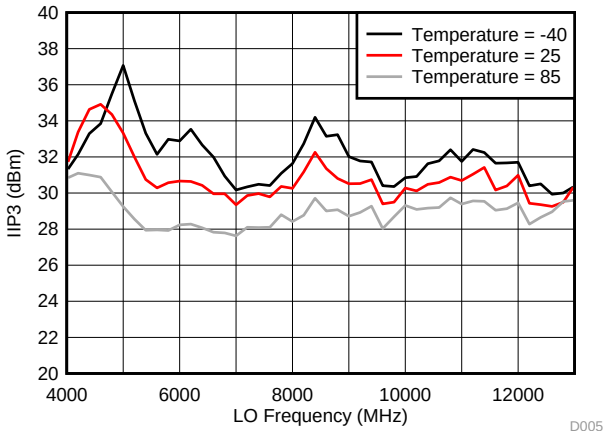

Figure 13. IIP3 Across LO Frequency for Internal LO Mode

OIP3 (Output-referred IIP3) is also commonly used, and it is defined with respect to output power level. Equation 4 shows the relationship between OIP3 and IIP3.

$$\mathrm{OIP_3} = \mathrm{IIP_3} + \text{Conversion Gain} \tag{4}$$

4.4 Figure of Merit

Usually there is a tradeoff between IIP3 and NF in the design process. At a system level, these two can 'compensate' for each other. Consider the diagram shown in Figure 14, where G, F, and I are gain, noise figure, and IIP3 in linear scale, respectively.

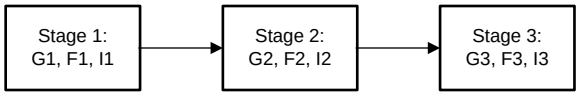

Figure 14. Block Diagram for Cascaded NF and IIP3 Calculation

The designer can use Equation 5 to calculate the cascaded noise figure in linear scale:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{5}$$

Equation 6 shows the cascaded IIP3 in linear scale:

$$\frac{1}{IIP_3} = \frac{1}{I_1} + \frac{G_1}{I_2} + \frac{G_1 G_2}{I_3} + \cdots \tag{6}$$

In a direct conversion receiver, there is an LNA preceding the mixer, which is then followed by other stages. Therefore it is reasonable to assume that Stage 2 is the mixer.

According to Equation 5, if F2 is too high, then the designer can reduce the overall F by raising G1. The designer can either choose an LNA with higher gain or simply add another LNA. According to Equation 6, however, if G1 is increased, total IIP3 will be decreased. In that sense, the designer trades the IIP3 for better NF. The opposite can be observed in a similar manner, however, because the designer can trade NF for better IIP3. To characterize this property, 'IIP3 - NF' is often used to assess NF and IIP3 together.

The effect of G2 is not very obvious, but it does impact system performance. If the mixer gain is too low, then an additional amplifying stage is required either before or after stage 2 to suppress the effect of F3.

For example, if the additional gain stage is implemented before Stage 2, then the overall noise figure may be reduced along with the IIP3. In the case where the gain of Stage 1 is already sufficient to suppress the F2, a decrease in noise figure by adding another LNA may be negligible, whereas the decrease in IIP3 can be significant. Therefore, besides NF and IIP3, the gain of Stage 2 is also important to mixer's in-system performance, and many applications require the gain of the IQ demodulator to be at least 0 dB.

Based on above discussions, the Figure of Merit defined in Equation 7 is commonly used to evaluate the in-system performance of mixer.

$$\text{FOM} = \text{OIP}_3 - \text{NF} = \text{IIP}_3 + \text{Gain} - \text{NF} \tag{7}$$

Figure 15 shows the FOM of the LMX8410L versus other IQ demodulators that have an overlapping frequency range with LMX8410L. Figure 15 shows that LMX8410L significantly outperforms its competitors in the 4-GHz to 12-GHz frequency range.

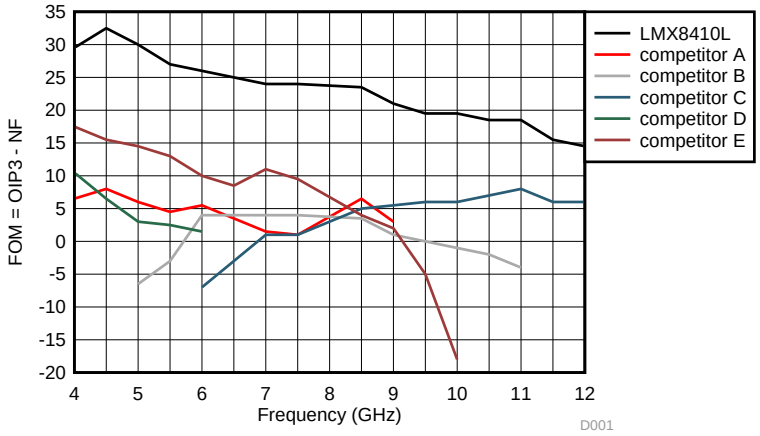

Figure 15. FOM of LMX8410L vs. Competitors Across LO Frequency

Note that:

- The performance data of competitor A, B, C, D, and E are obtained from the typical performance plots in their data sheets.
- Room temperature data is used for all devices.

5 In-System Evaluation of LMX8410L

The section describes the in-system performance evaluation of the LMX8410L in a RF front end example. This section describes the two parameters that are used to characterize receiver RF front end, namely sensitivity and dynamic range, and explains how to calculate these parameters in the presence of the LMX8410L and its competitors.

5.1 Receiver Sensitivity

The sensitivity of a receiver is the minimum signal power level that a receiver can detect (see Equation 8):

$$Sensitivity = -174\text{dBm} + NF + 10\log_{10}(B) + SNR_{min} \tag{8}$$

where

- –174dBm is the absolute noise floor kTB when T = 290K and B = 1Hz
- NF is the cascaded system noise figure
- B is signal bandwidth in Hz
- SNR_{min} is the minimum acceptable SNR at the output of ADC

When signal bandwidth and minimum SNR are fixed, the system noise figure is the determining factor of receiver sensitivity.

5.2 Spurious Free Dynamic Range (SFDR)

The maximum input power allowed for a spurious free system is the level when IM3 equals noise floor. The minimum input power is the receiver sensitivity. Equation 9 shows that the difference between cascaded IIP3 and cascaded NF reflects the system SFDR.

$$\text{SFDR} = \frac{2}{3}(174\text{dBm} + IIP_3 - NF - 10\log B) - SNR_{min} \tag{9}$$

5.3 LMX8410 In-System Performance

Consider the block diagram shown in Figure 16, where only one of the I/Q paths is shown and the other one is the same. For this example, the user can assume that RF frequency = 6 GHz, the complex signal bandwidth = 200 MHz (that is, IF band is from DC to 100 MHz), and SNR_{min} = 20 dB.

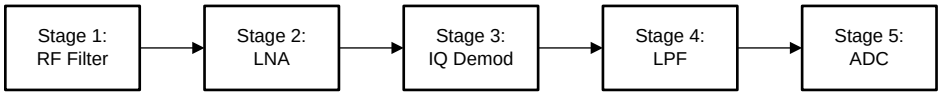

Figure 16. Example Direct Conversion Receiver Block Diagram for Spec Calculation

The specs required for each stage are shown in Table 2. Note that ADS54J60 is a dual-channel ADC that can sample both I and Q channels at the same time. The NF and IIP3 for ADC are calculated based on the *Direct RF Conversion: From Vision to Reality* [3] and *Calculating noise figure and third-order intercept in ADCs*[9]. Room temperature data is used for LMX8410L.

Table 2. Specifications of Receiver Components and Calculation of Cascaded NF and IIP3

COMPONENT	RF FILTER	LNA	IQ DEMODULATOR	LPF	ADC	UNIT
Part number	-	-	LMX8410L	-	ADS54J60	-
Frequency Range / Sampling rate	5.9 - 6.1 GHz	2 - 12 GHz	4 - 10 GHz	DC to 100 MHz	1GSPS	-
Gain(1)	-2	18	10.5	-3	-	dB
NF(1)	2	3	14.5	3	23.5	dB
IIP3(1)	1000(2)	10	30	1000(2)	40	dBm
Cacaded Gain	-2	16	26.5	23.5	-	dB
Cascaded NF	2	5	5.8	5.9	6.9	dB
Cascaded IIP3	1000	12	9.9	9.9	9.0	dBm

(1) Room temperature data is used for LMX8410L.
(2) A passive filter does not degrade system linearity. A large number is used such that the IIP3 of the filter does not influence the cascaded IIP3.

The cascaded NF and IIP3 of competitor D and E are calculated in a similar manner, where the IQ demodulator is the only variable and every other component remains the same. Competitor A, B, and C are left out of the comparison because they have a negative conversion gain that would require extra stages to optimize the system performance. In Table 3, the receiver sensitivity and SFDR are compared with the demodulator as LMX8410L, Competitor D, and Competitor E, respectively.

Table 3. Receiver Sensitivity and SFDR With LMX8410L vs Competitors

DEMODULATOR(1)(2)	LMX8410L	COMPETITOR D	COMPETITOR E	UNIT
NF	14.5	31	22	dB
IIP3	30	31	23	dBm
Gain	10.5	2	9	dB
Receiver cascaded NF	6.9	16.2	9.3	dB
Receiver cascaded IIP3	9.0	10.1	5.6	dBm
Receiver sensitivity	–67.1	–57.8	–64.7	dBm
Receiver SFDR	44.1	38.6	40.2	dB

(1) The data of Competitors D and E are obtained from the typical performance plots in the data sheet.
(2) Room temperature data is used for all devices.

When RF = 6 GHz, IF bandwidth = 100 MHz, and SNR_{min} = 20 dB, Table 3 shows that the LMX8410L yields a sensitivity that is 9.4 dB better than Competitor D and 2.5 dB better than Competitor E. The LMX8410L also yields an SFDR that is 5.5 dB better than Competitor D and 4.0 dB better than Competitor E.

To justify the FOM defined in Section 4.4, the receiver sensitivity and SFDR are plotted across the RF frequency in Figure 17 and Figure 18, respectively. The plot of dynamic range aligns with Figure 15 that shows the LMX8410L outperforming its competitors across the 4-GHz to 12-GHz frequency range.

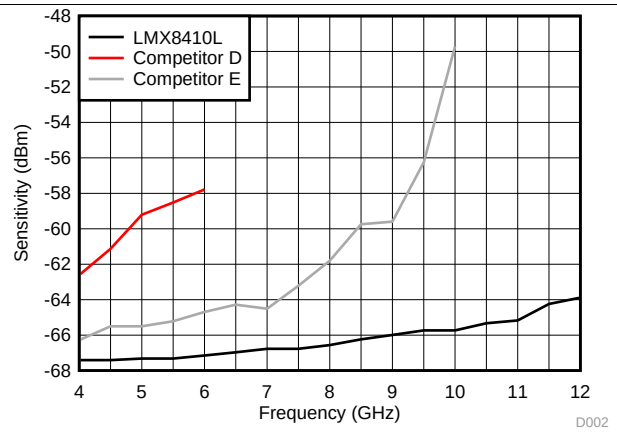

Figure 17. Receiver Sensitivity Across RF Frequency: LMX8410L vs Competitors

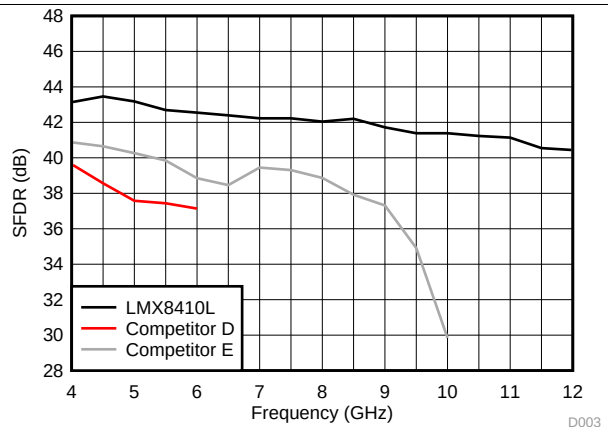

Figure 18. Receiver SFDR Across RF Frequency: LMX8410L vs Competitors

6 Additional Features of LMX8410L

Besides having excellent performance as an IQ demodulator, the LMX8410L offers additional features including integrated synthesizer, phase sync feature of the internal LO, single-ended RF input and internal 50-Ω matching, and adjustable common-mode level for driving ADCs.

6.1 Internal LO Mode and External LO Mode

One key feature of LMX8410L is that the device can integrate a low-noise RF synthesizer like the LMX2594. As a result, the LO can be injected internally. There are several advantages of having an internal LO:

1. One does not need to worry about the interfacing between the LO and mixer, and no amplifying or attenuation is needed for LO output, because the interfacing is optimized internally.
2. Compared to a discrete LO and mixer, the mixer with an integrated LO saves the evaluation time and simplifies design process for a project because only one device needs to be tested and configured.
3. In special cases where external LO injection is preferred, the internal synthesizer can be powered down and bypassed easily.

6.2 Sync Feature of Internal LO

The sync feature of the integrated synthesizer allows the user to synchronize the internal LO phase across multiple LMX8410L devices. The sync feature can be useful in applications such as a communications base station.

6.3 RF Input Matching

The LMX8410L offers single-ended, wide-band, 50-Ω matching for RF port. The single-ended RF port eliminates the need for external balun, and the internal, wide-band, 50-Ω matching makes it much easier to interface with the LNA. At high frequencies, external baluns can introduce extra distortion, mismatch, and loss. The RF S11 across frequency is shown in Figure 19.

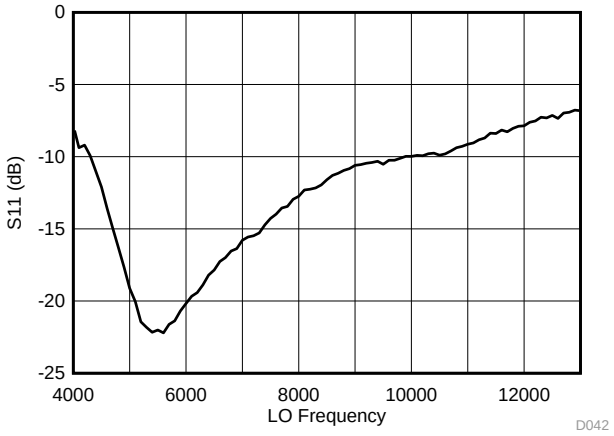

Figure 19. RF Port S11

6.4 Internal and External Common mode

The ADCs usually have common-mode voltage requirements for the ADC drivers. Usually, The ADC provides a voltage reference to define the common mode of the ADC driver output. The LMX8410L has a VCM_IN pin that can take the ADC voltage reference and set the common mode for the paired IF amplifier. This feature makes it easy for the LMX8410L to drive ADC directly.

Some ADCs may not provide this voltage reference. In that case, the voltage can be set internally. In other words, the VCM_IN pin is unused and common mode is defined in software. There are three options for IF common mode level: 1.2 V, 1.7 V, and 2 V.

7 Conclusion

The designer must consider two things when choosing IQ demodulators for the direct conversion receivers: the implementation challenges and the performance of the mixer. The designer should always look for devices that have low DC offset, low 1/f noise corner frequency, high IRR (absolute value), high IIP2, low LO to RF leakage, and low mixing spurs. For the mixer, a low NF, high IIP3, and high gain are required for better system sensitivity and spurious free dynamic range. The LMX8410L has excellent performance in both. The device also has an integrated internal LO, a single-ended 50-Ω RF input, and the device can support a VCM input for setting ADC common mode to help system design.

8 References

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265