Application Report
SNLA065A–May 2004–Revised April 2013

AN-1329 DP83865 and DP83864 Gigabit Physical Layer Device Trouble Shooting Guide

ABSTRACT

This application report focuses on debugging the GPHY circuitry in a systematic way and hopefully, will shorten the debugging time.

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1 Introduction

One of the biggest problems engineers encounter during the prototype stage is when the gigabit physical layer device (GPHY) fails to perform up to the expectations. There are many things that can easily go wrong when "attention to details" is neglected. "If anything can go wrong, it will." Sadly, the only thing seems to "work" reliably is the Murphy's Law.

Depending on the level of the experience of the designer and the familiarity with the GPHY device, the trouble shooting time could vary between a few hours to several days. This application report focuses on debugging the GPHY circuitry in a systematic way and hopefully, will shorten the debugging time.

2 Knowing the GPHY

To trouble shoot effectively, knowing the overall picture of the GPHY is helpful for understanding the logical steps taken to uncover the problem. Externally, the GPHY has three ports, two ports are for passing data between the host and the communications media, and one port is for accessing the GPHY internal registers (Figure 1).

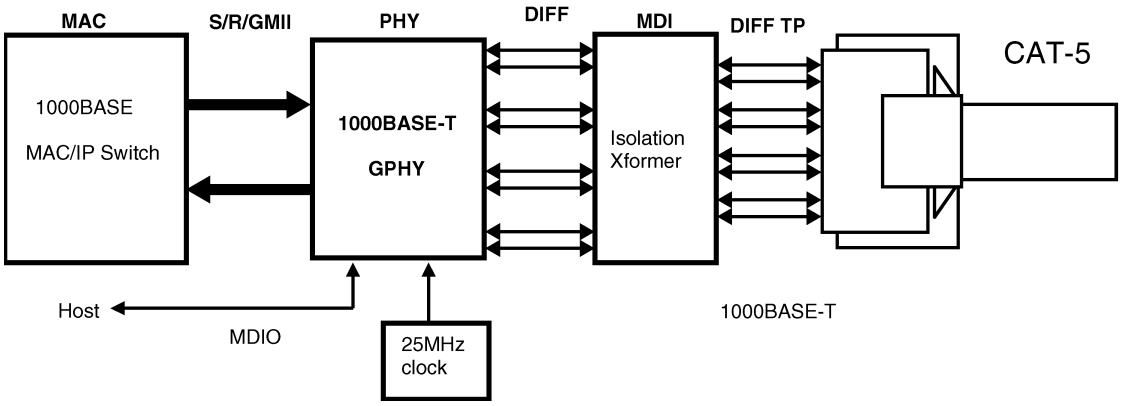

Figure 1. GPHY Block Diagram

The three external ports:

1. MAC interface is for the host to pass transmit and receive data to and from the physical layer device. Note that the clock signals on the MAC interface is only used for synchronizing data transfers between the MAC and the GPHY devices.
2. Media Dependent Interface (MDI) in the copper PHY is also referred to as the twisted pair (TP) interface. The TP interface places the encoded transmit data on to the copper cable and retrieves the receive data from the copper cable. In the 10BASE-T and 100BASE-TX modes, there is a dedicated transmit (Tx) pair and a receive (Rx) pair. In the Gigabit mode, all four pairs of the twisted pairs are used and the data transfer is bi-directional.
3. The management interface is also referred to as the MDIO port. Through this port, the host can access the GPHY registers, to alter operating mode or, to read the internal status of the GPHY.

The GPHY requires two power supplies, 1.8V for the core and analog receiver, and 2.5 V for the analog driver and the digital I/O interface. A third power supply 3.3V may be needed for interfacing with the 3.3V I/O logic.

Internally, the GPHY contains three major blocks:

1. Analog signal processing block contains multiple sub-blocks on transmit and receive path. The main function of this block is to condition the signal for transmit and receive, and to convert the signal between analog and digital domain.
2. The digital signal processing (DSP) block processes the data signals in the digital domain.
3. A microcontroller (µC) is the "brain" of the GPHY. The µC manages the communication between the host and the GPHY, the register status, the auto-negotiation, and many other features and functions.

There are other auxiliary functional blocks, such as clock generation and recovery blocks that provides clock to each of the digital blocks.

3 GPHY Trouble Shooting

There are various steps in debugging the GPHY. The process of GPHY trouble shooting is very similar to an emergency room (ER) service, while the GPHY is like a patient. This may not be an appropriate comparison, but hopefully, it will help user to remember the steps.

3.1 The "Heartbeat" of GPHY - Clock Source

Heartbeat is the absolute essential function for life. The heartbeat is also the vital sign. The similar essential element for the GPHY to function normally is the reference clock source to the GPHY. The following is a checklist of the clock signal.

1. Clock frequency: It should be 25 MHz at the reference input. For DP83864, it could be 125 MHz if the 125 MHz option is selected. The reference clock drift should be less then 50 parts-per-million (ppm).
2. Clock signal amplitude: When clock oscillator or clock distribution circuit is used, the signal amplitude is 3.3V or 2.5V. Do not over drive the reference input with a 3.3V clock driver if 2.5V I/O Vdd is selected. In the case of DP83865, when crystal is used, the clock oscillator amplitude should to be at least 200 mVpp (peak-to-peak) centered at the mid point of the supply voltage.
3. Clock signal integrity: Use scope probe on the reference clock input to check if (a) the edge of the clock is clean; (b) there is excessive ringing. If there is clock signal integrity problem, follow the Design Guide in the datasheet to terminate the clock signal correctly.
4. Strapping pins: Verify the strapping level with the datasheet to make sure (a) the correct reference clock input frequency is selected for DP83864; (b) the I/O Vdd selection matches the oscillator output level for both DP83865 and DP83864.

3.2 The "Defibrillation" - Reset

If for some reason the GPHY may enter into an unknown state and appears to be none functional. The only way to restart the GPHY is by external hardware reset. The following is a checklist for the reset signal.

1. Reset signal level: Hardware reset is an active low signal. Make sure the reset reaches the active low logic level during the active state. If reset is distributed to multiple GPHY on a board, probe each reset pin on the GPHY to make sure the signal reaches each device. Check to make sure the inactive level meets the logic high requirement (Figure 2) so that the GPHY internal logic starts normal operation.

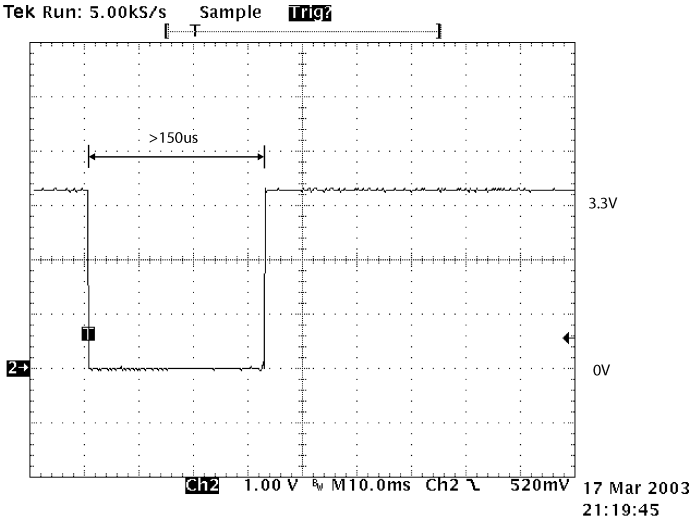

Figure 2. Reset Signal

2. Internal initialization time: After the GPHY coming out of the reset, it takes at least 20 ms to complete the internal initialization. No MDIO management access should be performed immediately after reset (Figure 3). Any attempt to access the internal register through management MIO port immediately after reset may cause the GPHY to malfunction.

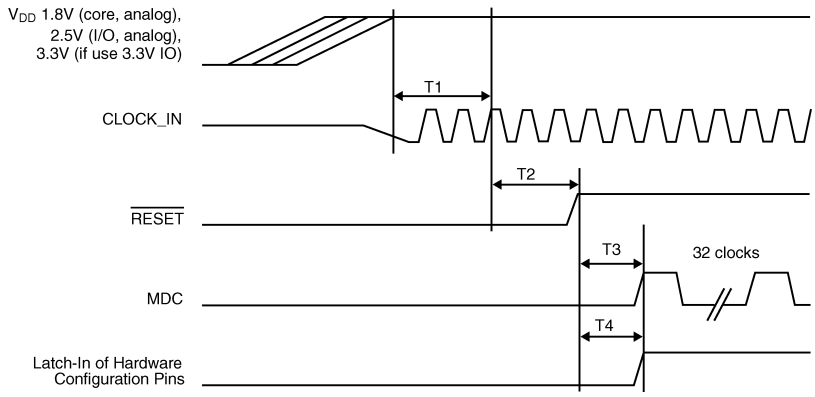

Figure 3. Reset Timing. T1 = 0+µs; T2 = 150 µs; T3 = T4 = 20 ms

3.3 Is There "Sign of Life"? - µC Operation

The GPHY will not function if the µC is not operating. The easiest way to verify the µC operation is to observe the presence of auto-negotiation link pulses.

1. When auto-negotiation (AN) is enabled (that is, AN_EN is strapped high), after reset, the GPHY transmits link pulses. By default, the auto-MDIX is also enabled. The link pulse will alternate between channels A and B (Figure 4).
2. Differential probe with 100-Ω termination can be placed on the RJ-45 connectors. The link pulse has (a) 2V pulse amplitude with pre-emphasis; (b) pulse width of 100 ns; (c) pulse period of 150 µs (Figure 5).
3. What if link pulse is not found? (a) The most common cause is that the transformer center tap is connected to the GND instead of 2.5V; (b) The designer may have mislabeled the transformer pins so that GPHY A, B, C, and D channels are not connected to the appropriate transformer windings; (c) Check to ensure the AN_EN pin is strapped high; (d) There should be 50 (termination resistors to 2.5V on each member of the MDI pair (Figure 4).

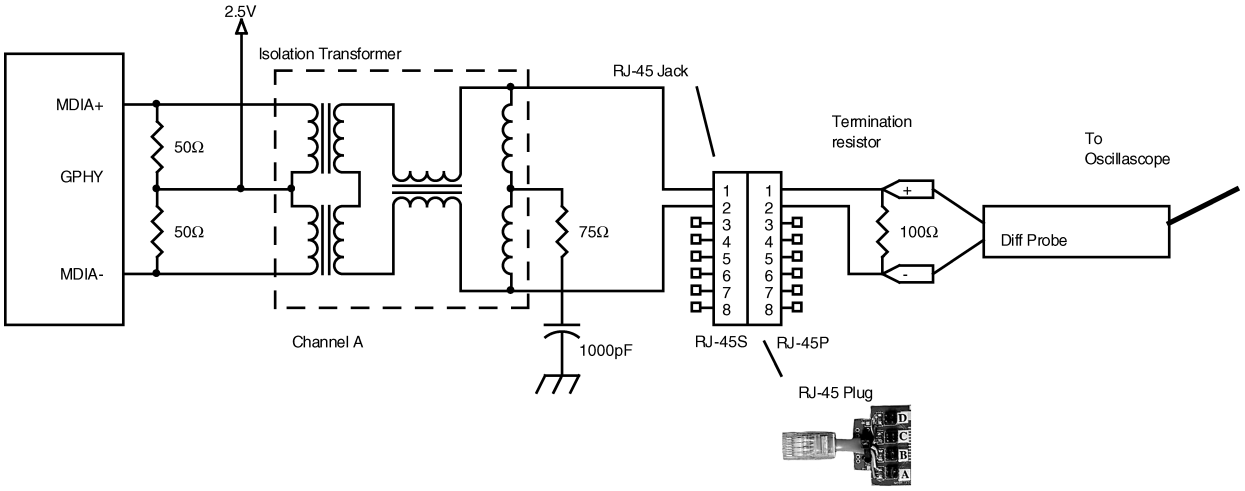

Figure 4. Link Pulse Test On Channel A

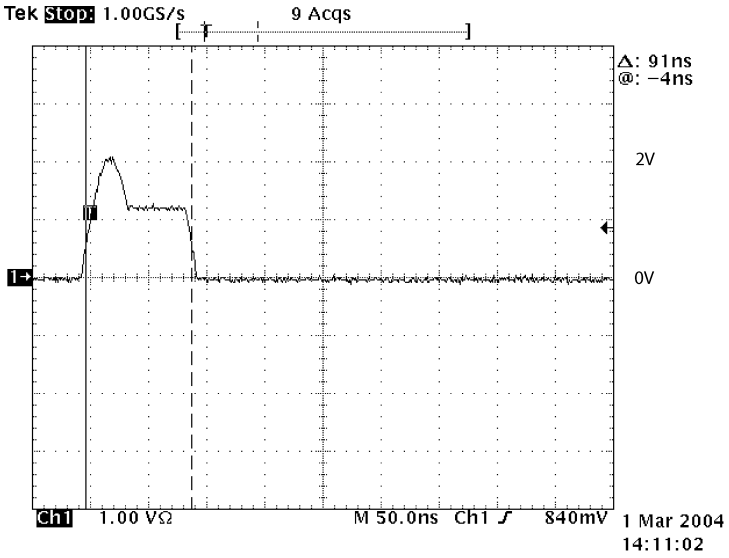

Figure 5. Auto-Negotiation Link Pulse

3.4 Checking the "Tubes" - Power Supply

3.4.1 Power Supply

The "feeding tubes" for the GPHY are the power sources. Check to make sure:

1. The power supply voltages (1.8, 2.5, and 3.3V) are at the level within tolerance of ±5%.
2. Verify with the datasheet that the power supply pins are connected with the appropriate supply source. Also, verify that the ground pins are connected correctly.
3. The I/O Vdd selection is strapped to the correct level; High for 3.3V and low for 2.5V I/O interface.

3.4.2 Bandgap Reference Voltage

Bandgap Reference (BG_REF) sets the internal reference voltage for many analog and digital functional blocks. Measure the voltage on the BG_REF to GND is around 1.20V. In order to achieve the correct BG voltage, the BG resistor value should be 9.76 KΩ (Figure 6).

3.4.3 PGM Supply

The PGM_VDD is the voltage to the internal clock phase generation module. A RC low pass filter attenuates the high frequency ripple on the PGM_VDD. Verify that the component values are 18 Ωs, 22 µF, and 0.1µF (Figure 6). The PGM_VDD should be about 1.8V.

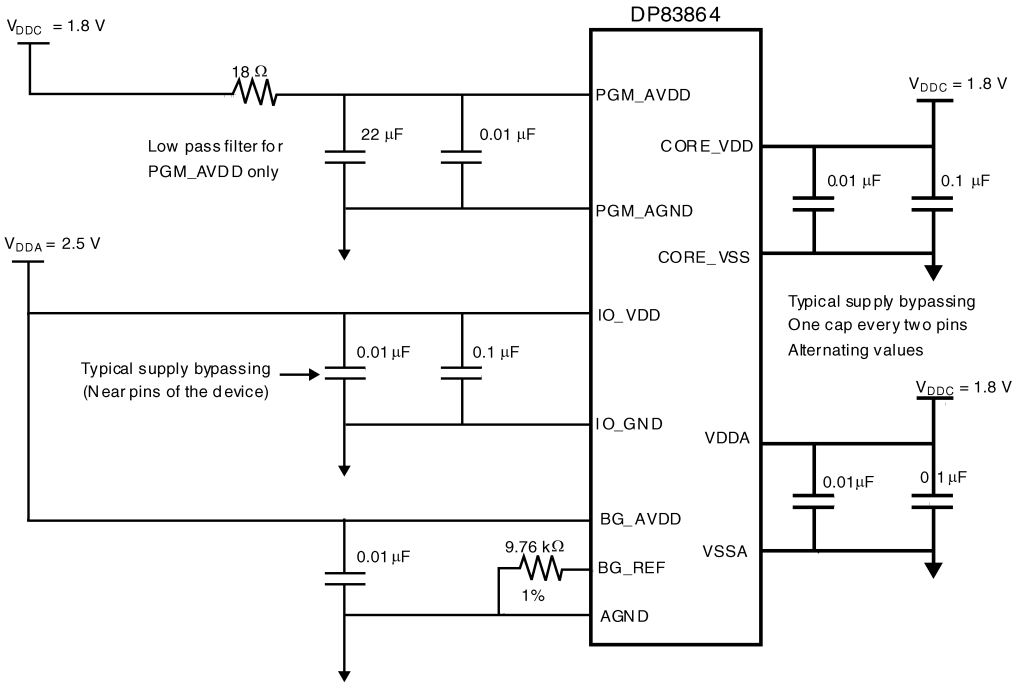

Figure 6. GPHY Power Supplies and Bandgap Voltage

3.5 It Is Time for Lab Tests - GPHY Internal Registers

3.5.1 Reading GPHY Registers Through MDIO

A critical diagnostic tool to have is the capability to access the GPHY internal registers through management MDIO port. The typical register values for the GPHY are listed in Table 1 and Table 2.

1. The value in register 0x00 is 0x1140. This means the AN_EN function is enabled.
2. If the value in register 0x04 is 0x01E1, the auto-negotiation will advertise 10/100 FDX and HDX.
3. If the value in register 0x09 is 0x0700, gigabit is advertised.
4. Register 0x10 displays the strapping pin status.
5. Register 0x12 displays 0x8000 so that Auto-MDIX is enabled. Auto-MDIX allows GPHY to detect any combinations of pair swap among the four pairs. Auto-MDIX can also correct the "+" and "-" polarity swaps within a pair. Note that Auto-MDIX works as long as each member of a channel pair stays within the pair.

Table 1. Register value, typical, while link is not established.

Addr.	Value	Addr.	Value	Addr.	Value	Addr.	Value
00	1140	08	0000	10	C061	18	0000
01	7479	09	0700	11	0018	19	0000
02	XXXX	0A	0000	12	8000	1A	0000
03	XXXX	0B	0000	13	0000	1B	0000
04	01E1	0C	0000	14	0000	1C	0000
05	C1E1	0D	0000	15	0000	1D	0000
06	0004	0E	0000	16	0000	1E	0036
07	0001	0F	3000	17	0000	1F	0001

Table 2. Register value, typical, while gigabit link is established (in master mode).

Addr.	Value	Addr.	Value	Addr.	Value	Addr.	Value
00	1140	08	4801	10	C061	18	0000
01	747D	09	0700	11	0017	19	0000
02	XXXX	0A	7C00	12	8000	1A	0000
03	XXXX	0B	0000	13	0000	1B	0000
04	01E1	0C	0000	14	0000	1C	0000
05	C1E1	0D	0000	15	0000	1D	0000
06	000D	0E	0000	16	0000	1E	0036
07	0001	0F	3000	17	0000	1F	0001

NOTE: DP83865 is typically used in the node applications. During the auto-negotiation, it advertises slave mode priority by default. DP83864 is a multiport device and typically used in the switches and hubs. It advertises master mode priority.

3.5.2 MDIO Management Port Trouble Shoot

What if MDIO does not read the correct value, for example, all 0xFFFF or all 0x0000?

1. Check MDC clock frequency; it should be no more than 2.5 MHz.
2. The MDIO signal is bi-directional and requires a 2 K pull up resistor.
3. Verify the MDIO data sequence with the datasheet to make sure the MDIO read access timing is correct. Pay special attention to the "turn around (TA)" time. The TA time should be at least 1-bit long.
4. Expand the scope scale to look at the MDC clock rising edge. Although the clock frequency is 2.5 MHz, the MDC input is sensitive to ringing. Ringing on clock edge can cause double clocking and produce erroneous reading.

3.5.3 Link with a Known Good Link Partner

By following the above steps, the fast link pulse should be seen on channel A and B. Try linking the GPHY with a known good link partner using a known good category 5 (CAT5) cable. After a valid link is established with a link partner, register 1 should read value 0x747D and the link LED should be lit.

3.5.4 IEEE Test Mode 2

If for any reason the GPHY still does not establish a valid link with a link partner, the gigabit test mode can help identify if there is any issue with the transmit and receive pairs. In the gigabit test mode 2, all four channels transmit a 62.5 MHz sinusoidal signal at 1 V (peak-to-peak) amplitude. To turn on the test mode 2:

1. Write register 0x00 with 0x1940 to power down the device.
2. Write register 0x09 with 0x4700 to enable the test mode 2.
3. Write register 0x00 with 0x1140 to power up the device. Test waveform should appear on all four channels of the GPHY.
4. Check RJ-45 pairs 1-2, 3-6, 4-5, and 7-8 to see the test waveform. Note that 100-Ω differential termination resistor is required.

Make sure sinusoidal signal presents on all four channels (Figure 7).

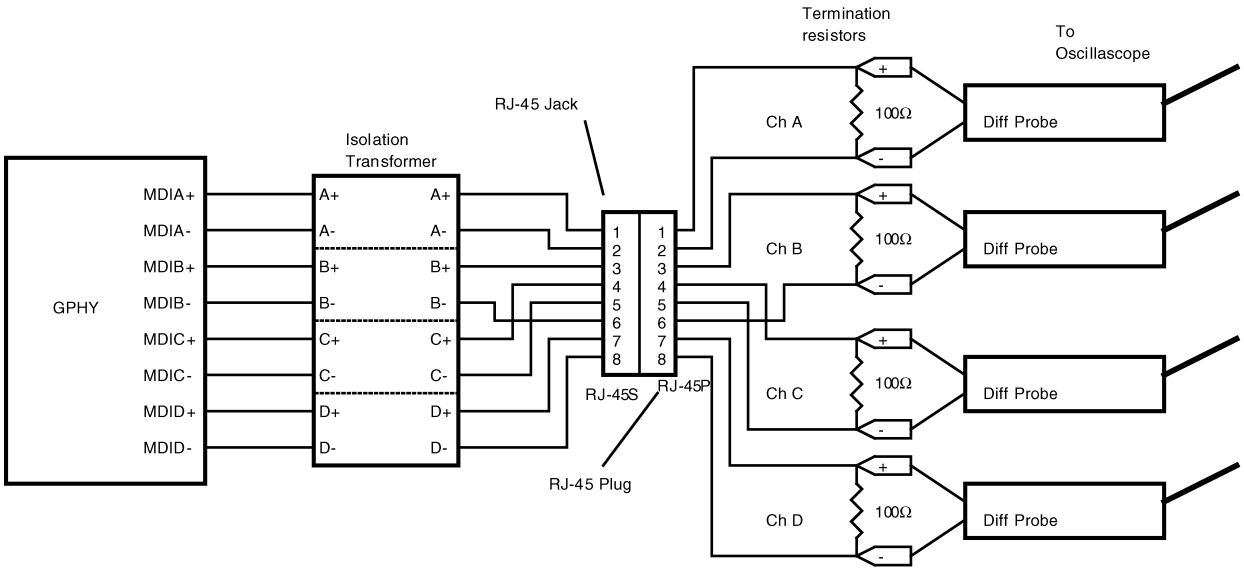

Figure 7. IEEE Gigabit Test Mode 2. (Simplified Diagram)

If the waveform is not found, check the MDI connections between the GPHY and the isolation transformer and, between the transformer and RJ-45 jack. Note that the transformer center tap should be connected to 2.5V. In addition, make sure that the 50-Ω termination resistors on each of the MDI pairs are connected correctly (Figure 4).

The waveform amplitude should be 1 Vp-p with ±5% tolerance. If the output amplitude is in correct, check the GPHY MDI to transformer connection. Make sure the transformer is made for gigabit Ethernet operation. The transformer specification may be compared with the table provided in the "Design Guide" section of the datasheet.

3.6 Can't Transmit and Receive Data from MAC?

If the GPHY has established a stable link with a link partner, but it is not able to transmit and receive data with a link partner, there are two steps that can be taken to determine if the problem is with GPHY or the MAC interface.

3.6.1 Built-in Self-test

GPHY has a built-in self-test (BIST) module. BIST can be configured to transmit and receive packets. The following is an example of transmitting continuous packet to a link partner:

1. Write to BIST_CFG2 0x1A with 0x8000 - Enable receive BIST counter.
2. Write to BIST_CFG1 0x19 with 0x4800 - Select BIST receive packet counter, clear any fragmented packet, and enable transmit.
3. Read register BIST_CNT 0x18 to check for received packet.

The BIST works under all three media speeds. The media speed can be established through auto-negotiation or manual forced mode. The manual speed mode can be setup by clearing register 0x00.12 (that is, register 0x00 bit 12), and using the Speed[1:0] to select the desired test speed. Note that 1000BASE-T link is through auto-negotiation per IEEE 802.3. Forced gigabit mode may cause link issues and it is not recommended. In addition, the 1000BASE-T mode BIST test requires GTX_CLK to be active in order for BIST to transmit packets.

The BIST also works in the loopback mode. To enable loopback mode, register 0x00.14 should be set, and use manual speed selection to enable the speed mode for the loopback tests.

By using the BIST, the ability to transmit and receive on MDI can be determined. For further detail, please refer to datasheet "BIST Operation" under "Configuration" section.

3.6.2 Transmit Loopback to Receive

To further confirm if the problem exists on the MAC interface, loopback mode can be setup to loop the transmit packet back on to the receive side of the MAC interface.

1. Write BMCR 0x00 with 0x4940 - Power down device and enable 1000BASE-T loopback.
2. Write BMCR 0x00 with 0x4140 - Power up and start loopback test.
3. Transmit data from MAC and observe received data.

If no data is received on the in the loopback mode, check the timing of GMII or MII interface against the datasheet.

3.7 What if the GPHY Can Not Achieve a Stable Link?

10BASE-T and 100BASE-TX are more tolerant to noise than 1000BASE-T. The signal-to-noise ratio requirement for the Gigabit mode is more stringent. The failure to achieve a stable link is commonly seen in the Gigabit mode.

There are many reasons for not achieving a stable link. User may examine the idle error count in the register 0x0A LSB byte. When idle error counter is none zero, there is CRC error and consequently, there will be packet drop during the transmission. When idle error count is high, approaching 0xFF, the link may drop and the GPHY will try to re-adapt with the link partner. Idle errors may come from the following sources.

3.7.1 Link Partner Transmit Problem

The commonly seen link partner transmit problem could be due to transmit waveform not meeting IEEE requirement and excessive clock jitter. Verify the link partner with another GPHY.

3.7.2 Cable Length and Quality

IEEE 802.3 specified cable reach is 100 meters CAT5 cable. The Texas Instruments GPHY has enough built-in headroom to operate with cables with lower quality, such as excessive attenuation and crosstalk. To eliminate the possibility of a bad cable, always try a shorter cable first, for example, CAT5 cables less than 50 meters in length.

It should also be noted that there are two types of CAT5 cable, solid conductor for longer reach and stranded conductor for short distance patching. The CAT5 patch cable is softer and has higher attenuation at high frequencies. Patch cables are typically up to five (5) meters long. Do not use the patch cable for long reach usage and use the solid conductor CAT5 for long reach applications.

Do not use lower than CAT5 grade cable for Gigabit transmission.

3.7.3 Clock Jitter

When two GPHY's are linked in gigabit mode, one is operating in Master mode and the other is operating in Slave mode. The Slave GPHY recovers the clock from Master's transmitted data. The Slave GPHY uses recovered clock for transmitting its data.

Master's clock. The Master's reference clock source jitter is mostly the cause for the transmitted data jitter.

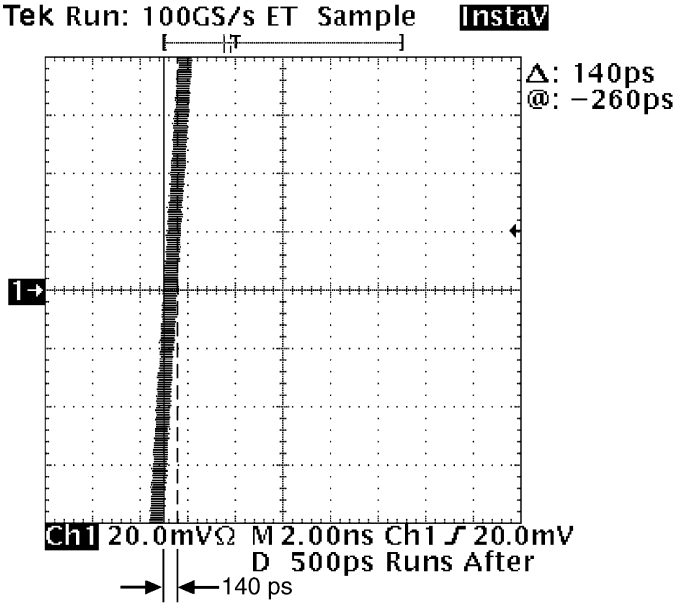

Figure 8. Typical Jitter Measured at the Jtxout in Ieee 802.3 Gigabit Test Mode 2 on a Compliant GPHY Device. The Captured is the Rising Edge of the Test Mode 2 Waveform.

The 1000BASE-T Test Mode 2 is designed to test the Master mode clock jitter. The IEEE 802.3 Clause 40.6.1.2.5 specifies that the filtered timing jitter on TX_TCLK plus the MDI Jtxout jitter shall be less than 300 ps (Figure 8). However, filtering the TX_TCLK timing jitter and making an accurate measurement may be subjected to different interpretation. To make rough jitter measurement, the easiest way is to place a differential probe on the MDI output (Figure 7). If a digital oscilloscope is used, set the scope in the "Infinite persistence" mode, adjust the "Display delay" to 10 us, the cumulative timing jitter is measured.

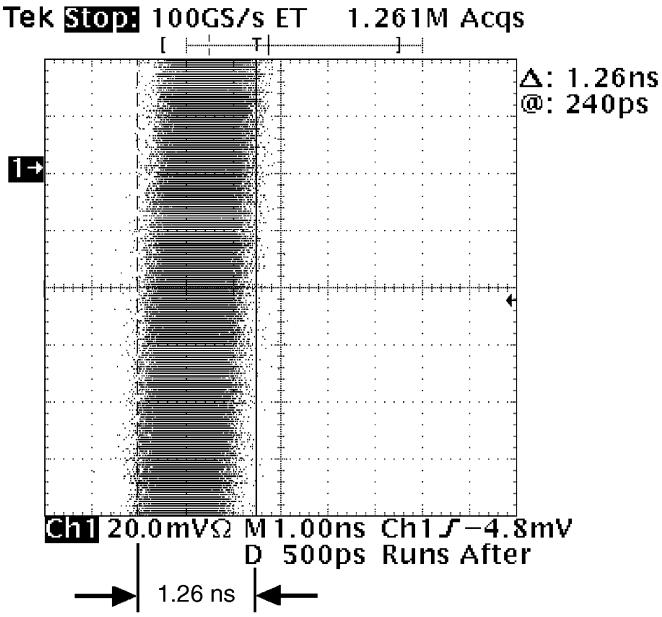

Figure 9. Excessive Jitter Measured at the Jtxout in IEEE 802.3 Gigabit Test Mode 2 on a Compliant GPHY Device

If excessive timing jitter is found on the transmit pairs (Figure 9), the user may choose to probe the GPHY reference clock input to provide some hint the source of the timing jitter. In many cases, the excessive jitter comes from clock distribution buffer, oscillator, or crystal. Check with the manufacturer on the component specification. The clock source component requirements can be found in the "Design Guide" section of the datasheet.

3.7.4 Voltage Supplies and Decoupling

The Texas Instruments GPHY uses 1.8V for both digital core and for sensitive analog receivers. Decoupling the 1.8V supply for the analog section will improve the GPHY performance. Check out the Design Guide in the datasheet for details of power supply decoupling and bypassing.

The PGM_VDD and Bandgap voltages mentioned in the previous sections are also important to the GPHY gigabit performance. Please follow the Design Guide in the datasheet.

3.7.5 GPHY Component Placement

The GPHY contains sensitive analog circuitries. Component placement planning is critical to minimize the potential noise coupling between digital and analog sections. If GPHY is placed between a noisy digital component and the power supply, the digital component's return current may cause ground bounce and couples the noise into the GPHY. Please refer to the "Design Guide" in the datasheet for further information.

4 Summary and Check List

- Make sure GPHY reference clock has the correct frequency and amplitude.
- Check out the reset signal active level and inactive level.
- Is the µC functional? Verify the auto-negotiation link pulse.
- Verify power supply connections, voltages, and I/O VDD selection.
- Bandgap reference voltage (1.2V) and bandgap resistor value (9.76 KΩ).
- PGM_VDD supply RC low pass filtering.
- Check out the GPHY internal registers. The main status registers are 0, 4, 9, and 0x10.
- Debug the MDIO management interface. Check the pull up resistor on MDIO and the TA time.

- Try to link with a known good link partner.
- Turning on the IEEE 1000BASE-T Test Mode 2 to check all four channels.
- Use the BIST module to verify the GPHY transmit and receive functions.
- Use Loopback mode to check the MAC interface data integrity.
- Hints on why GPHY is not able to achieve stable link with a link partner.
  - Link partner transmission
  - Cable length and quality
  - Clock jitter
  - Power supply and decoupling

5 References

DP83865 Gig PHYTER V 10/100/1000 Ethernet Physical Layer (SNLS165)

DP83864 Quad GigPHYTER 10/100/1000 Ethernet Physical Layer (SNLS172)

AN-1263 DP83865 Gig PHYTER V 10/100/1000 Ethernet Physical Layer Design Guide (SNLA056)

IEEE 802.3 ETHERNET WORKING GROUP: http://grouper.ieee.org/groups/802/3/

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