

AN-1340 Simplified Programming of Xilinx Devices Using a SCANSTA111/112 JTAG Scan Chain Mux

ABSTRACT

The SCANSTA111/112 provides a straightforward and flexible method of isolating scan chains for simplified programming.

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1 Introduction

Many modern communication and networking systems incorporate a system-wide IEEE 1149.1 (JTAG) test bus. The test bus not only enables a comprehensive, life-cycle approach to system test, but it also offers a number of additional benefits to the system designer.

The utility of the JTAG bus continues to expand beyond the boundaries of just test. JTAG is now used for emulation, memory programming, and configuration of CPLDs or FPGAs. These applications of the JTAG bus are well supported by the industry.

JTAG bus infrastructures continue to become more extensive, expanding to many devices on a circuit board and to multiple boards within a system. The need to manage the JTAG bus becomes apparent as the bus infrastructure expands. Grouping devices with similar technologies into smaller, local scan chains can reduce complexity and improve debug and fault isolation. Partitioning sets of components into local scan chains maximizes access for speed-critical applications, such as configuring large CPLDs or FPGAs or sets of such devices.

Systems with multiple cards and complex backplanes are designed to extend the JTAG infrastructure on each circuit card by extending the JTAG test bus across the backplane. Multiple cards can share the test bus when each card utilizes a JTAG interface device that enables multidrop addressing using the JTAG TAP.

Texas Instruments SCANSTA111 and SCANSTA112 (STA11x) devices enable partitioning of complex scan chains. The SCANSTA111 and SCANSTA112 support multidrop addressing, and manage up to three or seven local scan chains, respectively. The STA11x devices are commonly used for isolating components on a circuit board. This is particularly useful for configuring CPLDs or FPGAs.

When developing configuration vectors for Xilinx CPLDs, FPGAs and PROMs, adding the STA11x into the scan path introduces a new device that the Xilinx iMPACT programming tool is not expecting. For some STA11x operating modes, the Xilinx iMPACT tool can provide a serial vector format (SVF) file that may be modified in order to access the target device through the STA11x. This SVF may then be played through various means (for example, standalone Xilinx XSVF player from XAPP058, System ACE CF, or third-party JTAG tools).

In order to configure a Xilinx ISP device, a few simple additional steps are needed. [Figure 1](#) provides a basic description of how to accomplish this.

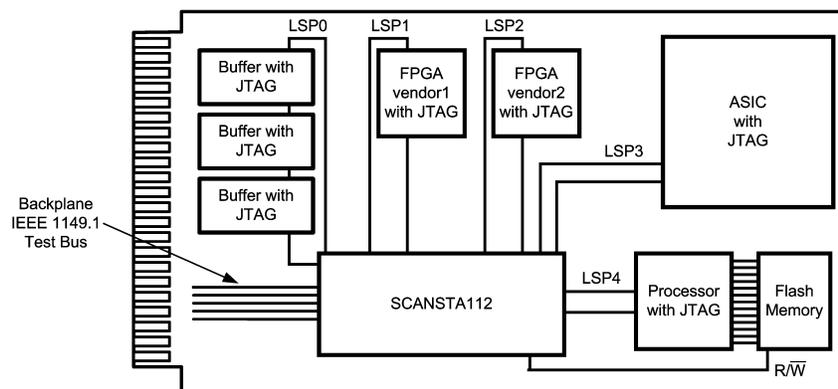


Figure 1. Typical Use of SCANSTA112 to Manage Multiple JTAG Chains on a Single Board

2 SCANSTA111/112 Operating Modes

There are three basic ways to get "through" the STA11x devices: transparent stitcher mode, transparent Scan Bridge mode, and normal Scan Bridge mode.

Transparent stitcher mode (STA112 feature only) is activated by way of external pins, and does not require changes to the SVF. This mode does require external hardware control. Setting the SB/S pin to 0 selects the stitcher mode; setting the TRANS pin to 1 puts the device into transparent mode; and the LSP select pins select the appropriate LSPs.

The transparent stitcher mode is specifically recommended when configuring Xilinx FPGAs due to bitstream alignment requirements of the Xilinx FPGA.

Transparent Scan Bridge mode requires a preamble in the vectors that are used to configure the Xilinx ISP devices. The iMPACT tool can write out an SVF file that can be "played" later by third-party SVF delivery tools. Note that when the STA11x is in transparent mode it is simply buffering the 1149.1 signals. Therefore, it is adding delay, and this may require that the clock speed be lowered.

[Example 2](#) and [Example 3](#) demonstrate preambles to configure the STA11x device into transparent Scan Bridge mode. Once this is executed, the STA11x device acts as a set of buffers between the backplane side and the LSP side of the device (Tester TDO → STA11x TDI → STA11x LSP TDO → local chain → STA11x LSP TDI → STA11x TDO → Tester TDI).

Normal Scan Bridge mode also requires a preamble in the vectors used to configure a Xilinx ISP device. Note, however, that when the STA11x is not in transparent mode, it adds a re-synchronization bit (pad bit) to the end of the chain. This re-times the signals and allows for operation at full clock speed, but requires the addition of the pad bit into the scan path for each LSP inserted in the path. [Example 4](#) and [Example 5](#) demonstrate preambles to configure the STA11x device into normal Scan Bridge mode. Once this is executed, the STA11x acts as a set of buffers between the backplane side and the LSP side of the device, with the addition of the pad bits (Tester TDO → STA11x TDI → STA11x register → STA11x LSP TDO → local chain → STA11x LSP TDI → PAD-bit → STA11x TDO → Tester TDI). Note that this requires additional bits in the scan process for the STA11x register and the pad bits.

In complex Scan Bridge architectures, pad bits that are put inline prior to the FPGA might misalign critical bitstream data arriving at the FPGA. This method is not recommended for configuring Xilinx FPGA devices.

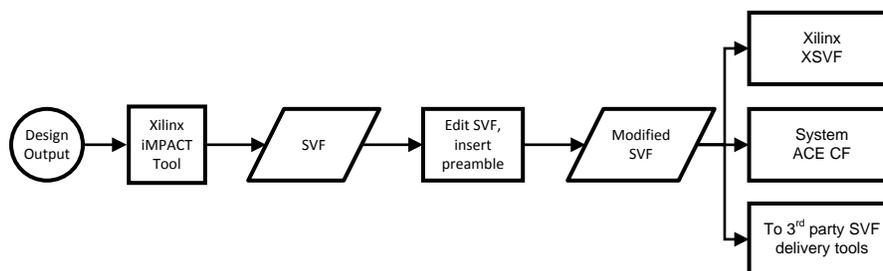


Figure 2. Tool Chain and Process for Modifying SVF

3 Example Code From Xilinx Modified SVF

[Example 1](#) is modified SVF from the iMPACT tool output. In this example, the STA11x device is at hex address 0x1B; the target device is located on LSP1. In the example, two lines of code (the highlighted lines) have been added that address the correct device and select the correct local port.

Example 1. Modified SVF From the iMPACT Tool Output

```

// Created using Xilinx iMPACT Software [ISE Foundation - 6.3.01i]
TRST OFF;
ENDIR IDLE;
ENDDR IDLE;
STATE RESET IDLE;
SIR 8 TDI(1B); ! <<<-- level one protocol, STA11x at address 1B hex
SIR 8 TDI(A1); ! <<<-- level two protocol, target device on LSP 1
TIR 0; !
HIR 0; ! Describes additional devices in the chain besides the target device
TDR 0; !
HDR 0; !
// Validating chain...
HIR 0;
TIR 0;
TDR 0;
  
```

Example 1. Modified SVF From the iMPACT Tool Output (continued)

```
HDR 0 ;
SIR 8 TDI (ff) SMASK (ff) TDO (01) MASK (e7) ;
//....rest of SVF file
```

4 Example Code for Simulations and Verification

4.1 Transparent Scan Bridge Mode

In [Example 2](#), the STA11x device is at address 0x11; the target device is located on LSP0. In [Example 3](#), the STA11x device is at the same address, but the target device is on LSP1.

Example 2. Configuring an LSP of the STA11x in Transparent Scan Bridge Mode

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Address ScanBridge
SIR 8 TDI (A0); ! Load instruction to enable transparent mode for LSP0
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (C3); ! Try to load GOTOWAIT in ScanBridge
SDR 8 TDI (5a); ! Verify that ScanBridge did not recognize GOTOWAIT
! Now TDIB → lsp0 → TDOB
```

Example 3. Configuring an LSP of the STA11x in Transparent Scan Bridge Mode

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Address ScanBridge
SIR 8 TDI (A1); ! Load instruction to enable transparent mode for LSP1
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (C3); ! Try to load GOTOWAIT in ScanBridge
SDR 8 TDI (5a); ! Verify that ScanBridge did not recognize GOTOWAIT
! Now TDIB → lsp1 → TDOB
```

4.2 Normal Scan Bridge Mode

In [Example 4](#), the STA11x device is at address 0x01. LSPs 0, 1, and 2 are connected to the backplane port. In [Example 5](#), the STA11x device is at the same address (0x01) but only LSP0 is connected to the backplane port.

Example 4. Configuring LSP's of the STA11x in "Normal" Scan Bridge Mode

```
TRST ON;
TRST OFF;
SIR 8 TDI(01); ! scan in address
SIR 8 TDI(8E); ! modesel-0 Setup mode register to select LSP
SDR 8 TDI(07); ! LSP0-2 STA11x
SIR 8 TDI(E7); ! UNPARK Sync LSPs to backplane port.
! MR0: X000X111
! TDIB → register → lsp0 → pad → lsp1 → pad → lsp2 → pad → TDOB
```

Example 5. Configuring LSP's of the STA11x in "Normal" Scan Bridge Mode

```
TRST ON;
TRST OFF;
SIR 8 TDI(01); ! scan in address
SIR 8 TDI(8E); ! modesel-0 Setup mode register to select LSP
SDR 8 TDI(01); ! LSP0 STA11x
SIR 8 TDI(E7); ! UNPARK Sync LSPs to backplane port.
! MR0: X000X001
! TDIB → register → lsp0 → pad → TDOB
```

Revision History

Dec 2009 – Clarification changes only.

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