

AN-1511 Cable Discharge Event

ABSTRACT

This application report discusses exposing semiconductor devices to potentially destructive Electro Static Discharge (ESD).

Contents

1	Introduction	2
2	What is Cable Discharge Event?	2
	2.1 The Charging Process	2
	2.2 The Discharge Process	3
3	Design for CDE	6
4	Validating the CDE Protection Circuitry	7
5	Factors That Can Alter the Measurement Results	8
6	Conclusion	8

List of Figures

1	Charge Build Up On A Cat5 Cable	3
2	CDE Discharge Path During UTP Cable Installation	4
3	CDE Discharge Using Simulated Test Setup	4
4	Cable Discharge Measured MDI+ to Ground and MDI- to Ground. MDI offset is at 2.5V. The peak-to-peak amplitude can be 20V.	5
5	IEEE Test Mode 2. Top trace channel A is showing the normal amplitude. Bottom trace channel B shows reduced amplitude due to ESD damage.	6
6	CDE Test Jig Block Diagram	7

1 Introduction

The widespread use of electronic equipment in various environments exposes semiconductor devices to potentially destructive Electro Static Discharge (ESD). Semiconductor devices internal to a piece of equipment are typically immune to ESD events. However, the semiconductor devices that interface to the outside world are exposed to and are at a much higher risk to an ESD event.

ESD events can occur from many sources and each has its own set of characteristics. Human Body Model (HBM), Charged Device Model (CDM) and Machine Model (MM), named by their sources, are the most common ESD events. With the preponderance of Ethernet network 'connected' equipment, the equipment's network or Ethernet interface is becoming increasingly critical. Since the Ethernet network connection is often very long, and typically made of Unshielded Twisted Pair (UTP) cable, the Ethernet interface is also prone to an additional ESD event called Cable Discharge Event (CDE).

The ESD event occurring during the UTP network cable installation is very different from the standardized HBM, CDM and MM. Unlike the HBM, CDM and MM, that consist of a very high impedance and low capacitance model, the UTP CDE discharges a very large amount of charge with low source impedance. The UTP cable discharge event can be as high as a few thousand volts and can be very destructive. The following sections describe the CDE event that occurs during the cable installation, that is, the charge build-up and dissipation process. Also discussed is the destruction prevention during the ESD event and the test for validating the ESD protection methodology.

2 What is Cable Discharge Event?

As with any ESD event, a build-up or accumulation of electrostatic charge, and a subsequent release or dissipation of the charge to some conductive path causes the CDE.

2.1 The Charging Process

The charge accumulation can come from two main sources, triboelectric (friction) effect and electromagnetic induction effect. Pulling a PVC-covered CAT5 UTP cable on a nylon carpet can cause charge build up on the cable by triboelectric effect. In a similar way, charge can also build up on a cable when the cable is pulled through a conduit or dragged through other network cables. This charge build up is similar to that from scuffing your feet as you walk across a carpet.

Other events adjacent to the cable such as electronic light ballasts that generate electromagnetic fields can induce charge build up on the cable, too.

In the above cases, the subject cable resembles one plate on a capacitor and the carpet floor or the conduit resembles another plate ([Figure 1](#)). The quantity of the charge accumulated is directly proportional to the cable length and inversely proportional to the distance between the two plates.

Note that the charge build up only occurs when cable is un-terminated and the charge is not dissipated immediately. In other words, both ends of the cable are not plugged into a system. Also, the accumulated charge has to be retained in order to cause substantial damage. The newer CAT5 and CAT6 cables have very low dielectric leakage and tend to retain charge for a long period. Charge retention time is increased in an environment where there is low relative humidity. All these factors are causing more frequent incidents of ESD events.

All these charge accumulation and retention processes set up for a potentially destructive dissipation, the CDE event.

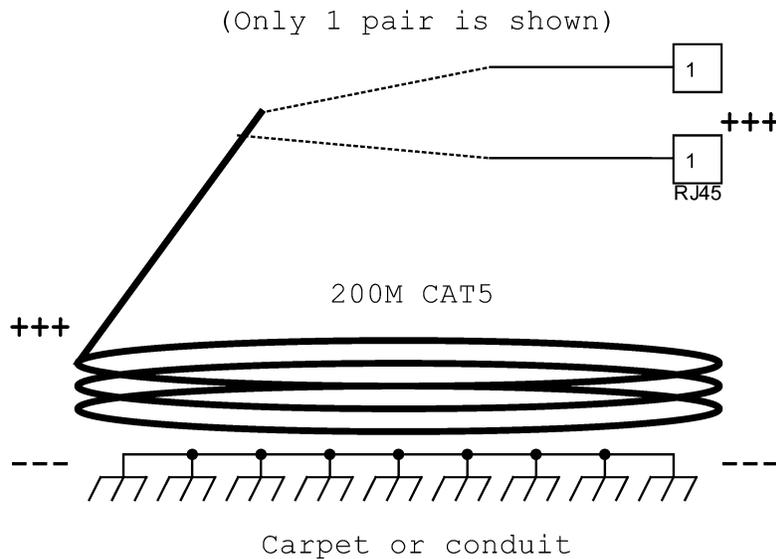


Figure 1. Charge Build Up On A Cat5 Cable

2.2 The Discharge Process

When a charged UTP cable is plugged into a RJ-45 network port, there are many paths of discharge. Following the rules of the AC current flow, the transient current takes the lowest inductance path. This path could be at the RJ-45 connector, between two traces of a printed circuit board (PCB), in the transformer, through the Bob Smith AC termination, or on the silicon device (Figure 2). This current is large enough to cause dielectric breakdown. When high voltage appears at the device's Media Dependent Interface (MDI) transceiver input, the high voltage could cause damage to the ESD protection diode, the line driver, and dielectric break down between the MDI signal path and the adjacent circuitry, and so on.

To simulate the CDE event, a test jig is built with relays to charge the UTP cable using Hi-Pot voltage generator and then discharge UTP cable through the RJ-45 network port (Figure 3). The signal swing measured at the MDI pins reference to ground is in the range +10V and -10V (Figure 4). Although the signal amplitude is not very high, the current is large since the UTP cable only has a small source impedance to limit the current flow during the transient state. This high discharge current is enough to cause irreversible damage to the transceiver semiconductor device. A post CDE discharge transceiver functional test reveals that the MDI output driver is damaged. Figure 5 shows the signal swing of the output driver is greatly reduced after the CDE event.

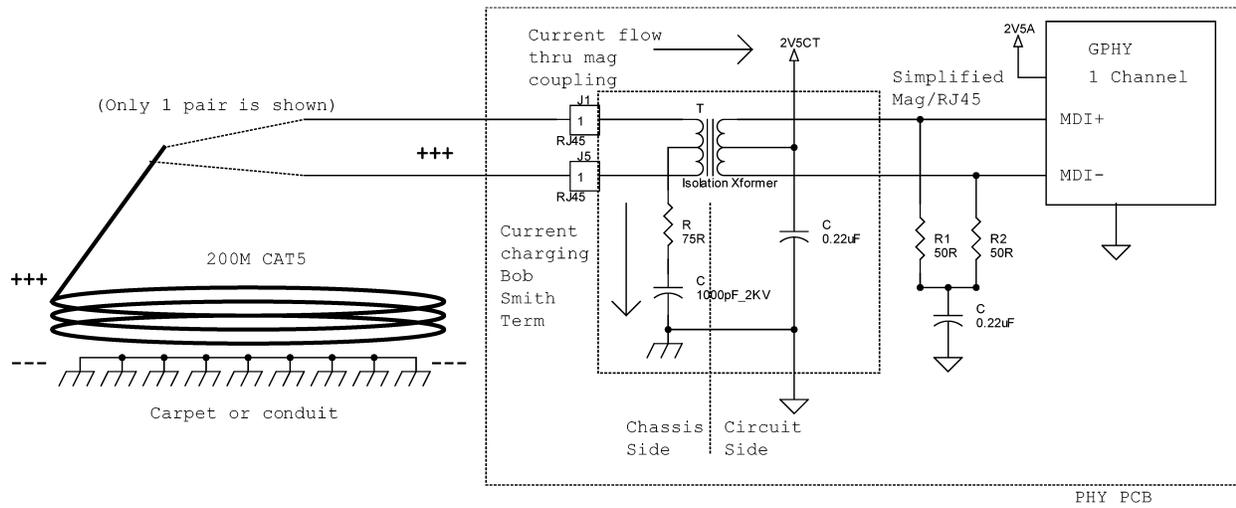


Figure 2. CDE Discharge Path During UTP Cable Installation

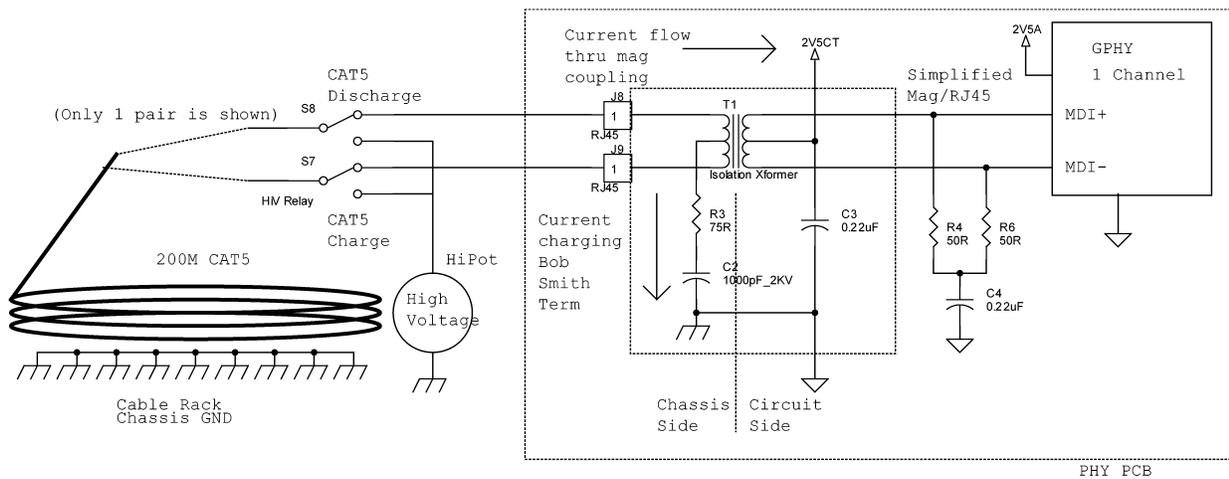


Figure 3. CDE Discharge Using Simulated Test Setup

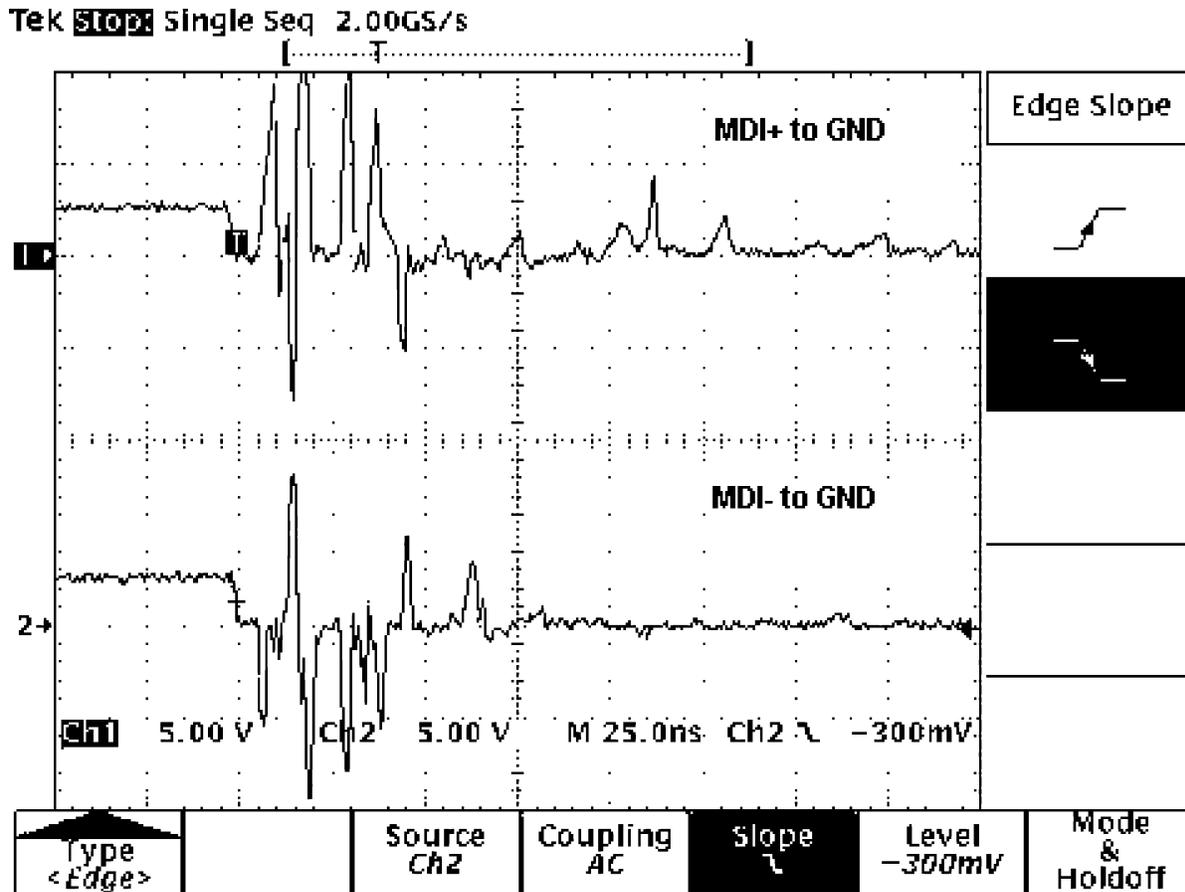


Figure 4. Cable Discharge Measured MDI+ to Ground and MDI- to Ground. MDI offset is at 2.5V. The peak-to-peak amplitude can be 20V.

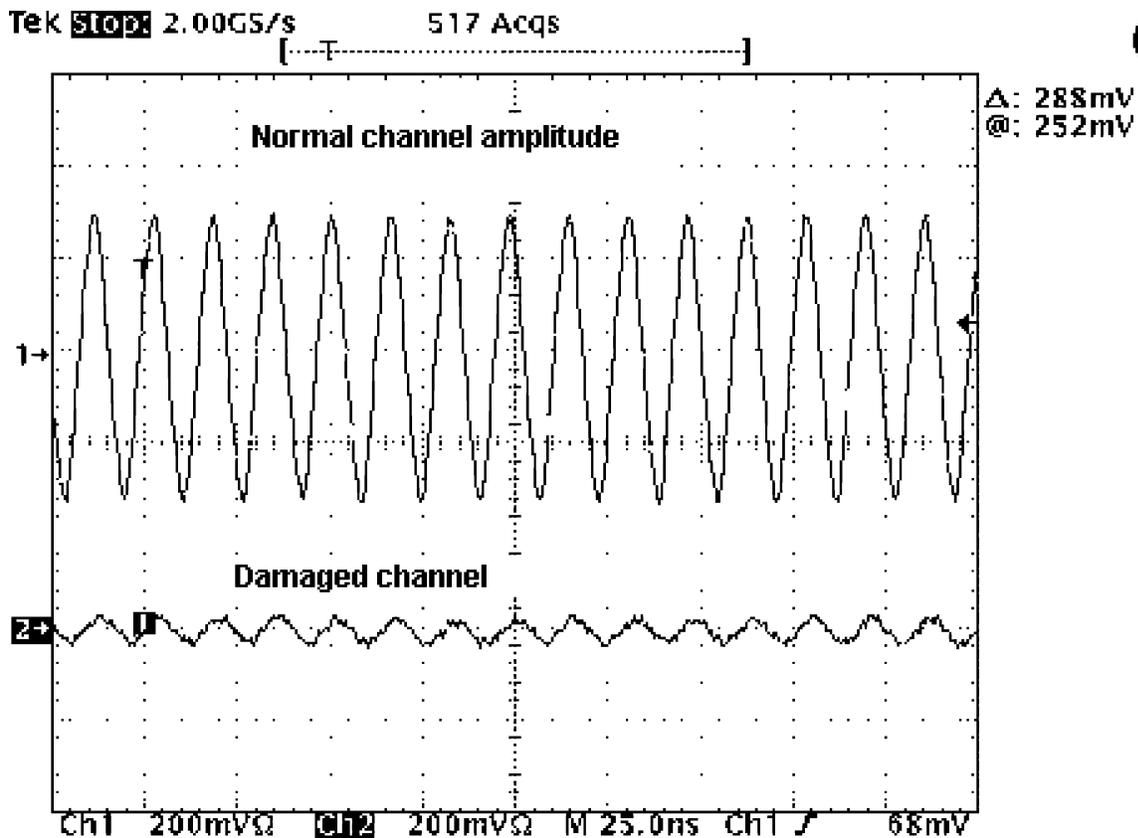


Figure 5. IEEE Test Mode 2. Top trace channel A is showing the normal amplitude. Bottom trace channel B shows reduced amplitude due to ESD damage.

3 Design for CDE

To prevent arcing on the RJ-45 connector, circuit designers should use RJ-45 connectors that can withstand high transient voltage. The IEEE 802.3 standard calls out isolation voltages of 2250V DC and 1500V AC to prevent connector failures. These isolation voltages also apply to the transformers. The designer should verify with the component vendor to make sure that the selected RJ-45 connector meets these specifications.

To prevent dielectric break down and sparking on the circuit board, the line side (that is, the UTP side) printed circuit board and the ground should have ample spacing. Lab tests have shown that to withstand 2000V of transient voltage, the FR4 circuit board trace spacing should have a separation of at least 250 mils.

When high voltage appears at the MDI transceiver pins, there has to be an intended current route designed for the charge to dissipate. Placing ESD diodes at the I/O pad ring periphery of the transceiver provides the first line of defense before the high voltage entering the input/output (I/O block) circuitry. During the CDE event, these ESD diodes conduct and the large transient current routes to the power supply or ground bypassing the device circuit. The CDE energy is dissipated by the ESD protection circuitry.

The cable discharge event causes much higher current flow than the ESD Human Body Model, Machine Model, and Charged Device Model since there is no current limiting resistance at the ESD source. Depending on the length of the cable, the charge accumulated can be hundred times larger than the charge built up on other ESD model. This large accumulated charge makes dissipation design more challenging. Instead of using ESD diodes, designers often use silicon controlled rectifier (SCR) to provide lower "ON" impedance so that less heat builds up and to reduce the possibility of silicon break-down.

4 Validating the CDE Protection Circuitry

A test jig along with a CDE CAT5 cable plant test and validate the CDE design (Figure 6). The test jig contains relays and switching circuitry. By using a high voltage generator (Hi-Pot tester), CAT5 cable is charged up with high voltage reference to the chassis ground. The relay switches the charged cable to the device under test (DUT) RJ-45 port. This is a charge transferring process. The charge transfers from UTP cable to the DUT. Some charge dissipates at the DUT and there is residual charge built up on the DUT (see Section 5). After the cable discharge event, the charge built up on the DUT should bleed off, allowing for safe human handling of the circuit board before the next test and for ensuring test consistency.

Figure 6 shows two sets of relays. One set (S3 and S4) handles the cable charge and discharge, and the other set of relays (S5) handles the DUT residual charge bleeding.

Figure 6 also shows a delay circuit between S3 relay to S4 relay in the discharge switching process. This circuit is to simulate the connector insertion process and show that there are timing differences between the contacts making process. The contact delay is adjustable between 0.5 ms to 5 ms. This difference in timing creates an additional differential voltage between the MDI+ and MDI- pair. Within a UTP pair, the first wire makes the contact with the RJ-45 will have the charge dissipated or partially dissipated. When the second wire makes the contact with the RJ-45 after the first wire, the second wire will have the full voltage while the first wire has lower voltage potential. This potential difference creates a differential voltage difference across the MDI+ and MDI- pair. This differential voltage creates an additional challenge to the circuit designer to tolerate the differential in addition to the common mode CDE voltage.

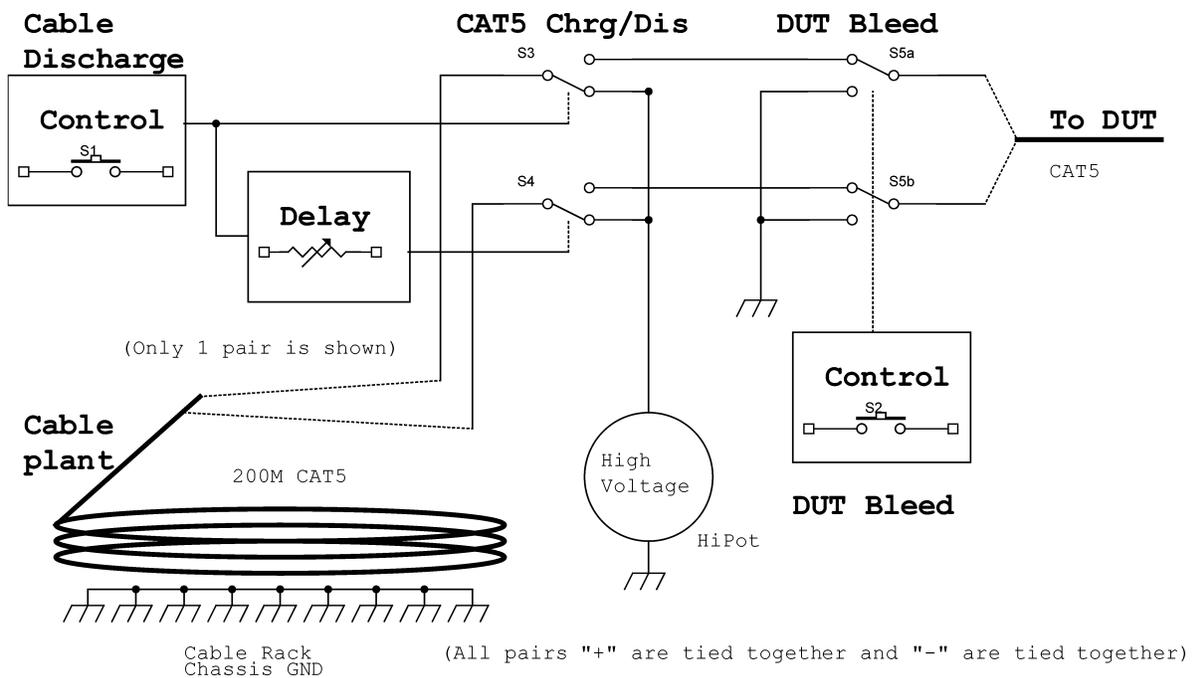


Figure 6. CDE Test Jig Block Diagram

5 Factors That Can Alter the Measurement Results

- **Residual Charge Bleeding:** While there is residual charge built up on the DUT port, the next CDE discharge will not achieve the expected voltage potential difference between the charged cable and the DUT port. The discharge current is directly proportional to the voltage difference between the UTP cable and the DUT. The higher the potential difference is, the higher will be the transient current during the CDE ESD event.
- **The Interval Between Each Test:** To test a DUT port multiple times in one test session, lab test results show that there should be a minimum of 2 minutes between each CDE ESD event. Because of the the dissipation of large current, the ESD protection circuitry generates heat. Heating can further reduce the circuit ESD tolerance, causing circuit damage and failure. In reality, having CDE event frequency less than 2 minutes, during a cable installation, rarely happens and creates unnecessary stress to the silicon device.
- **Humidity:** Humidity affects the charge build-up between the cable spool and the ground. Increasing the humidity, changes the air dielectric property between the wire and the ground so that the capacitance is reduced. With reduced capacitance, the charge stored on the cable will be reduced, so that the transient current during the CDE discharge will be reduced causing inconsistent test results. The CDE cable should be placed in a humidity controlled environment to minimize test inconsistencies.

6 Conclusion

All semiconductor devices are susceptible to Electrostatic Discharge (ESD) events. Devices interface to the outside world are more at risk than devices that interface internal within a piece of equipment. The Ethernet network interface is exposed to an additional, and even more hazardous ESD event called Cable Discharge Event (CDE). A CDE during the UTP cable installation can be destructive to the Ethernet PHY device. Texas Instruments has created a process and a set-up to test the CDE ESD tolerance. This test process can serve as a quality measure of the robustness of the Ethernet network connected equipment to CDE.

Texas Instruments devices that pass the CDE tests:

- DP83848 - 2000V CDE
- DP83865 – 1500V CDE

For more product details, go to [Ethernet Solutions](#).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com