Application Report
SNLA120A–July 2009–Revised April 2013

AN-1979 LVDS Timing DS32ELX0421 and DS32ELX0124 Serializers and Deserializers

ABSTRACT

The highly integrated FPGA-Link SerDes chipset (DS32ELX0421 and DS32ELX0124) enables low-cost FPGAs in a variety of high performance, high-speed applications. They feature advanced on-chip signal and clock conditioning circuitry that extends the data transmission reach of CAT-6 (shielded 24 AWG) cable beyond 20 meters without additional external components.

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1 Introduction

The serializer and deserializer unique architecture is designed specifically to address the interface requirements of low cost FPGA devices. The 5-bit LVDS parallel data interface simplifies board layout by reducing the number of input/output (I/O) pins and traces between the serializer, deserializer and the FPGA. This application report explains the serializer and deserializer LVDS timing requirements for the DS32EL0421, DS32EL0124, DS32ELX0421 and the DS32ELX0124 products.

This application report refers to DS32EL0421, DS32EL0124, DS32ELX0421, DS32ELX0124.

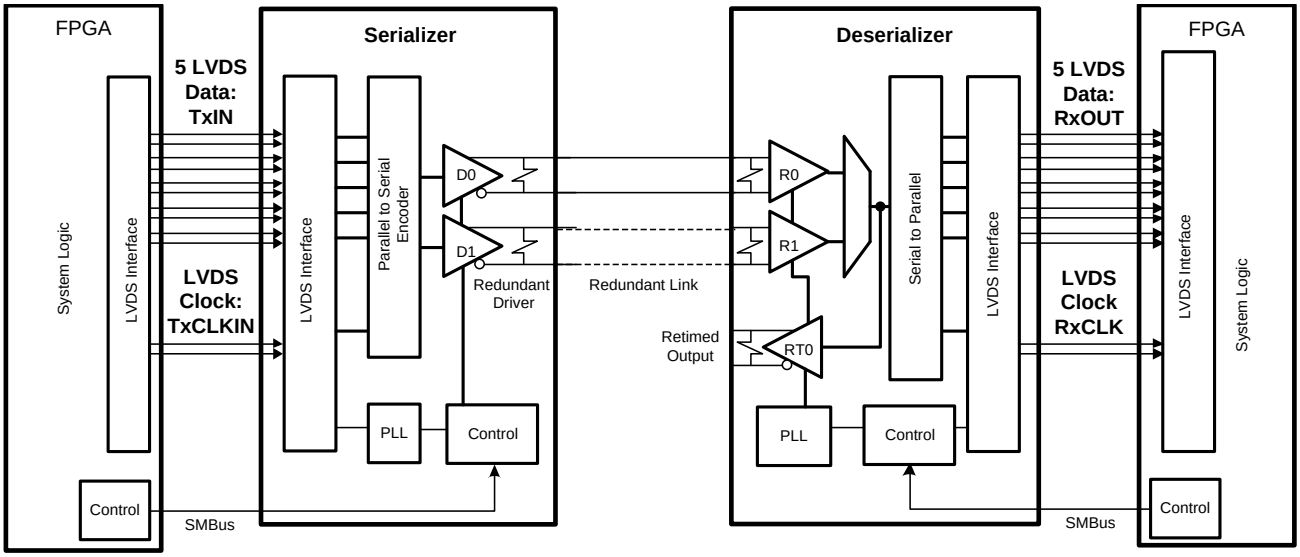

Figure 1. FPGA-Link System Diagram

2 Serializer Device Timing Requirements

If you think back to how the channel link serializers (DS90CR483A) are specified, there is a single clock edge sampling a single data edge on the LVCMOS parallel interface. The clock samples the data on a single edge. The setup time of 2.5 nanoseconds and hold times are 0 seconds. The optimal clock position for the channel link serializer is in the middle of the bit period of the data, as seen in Figure 2.

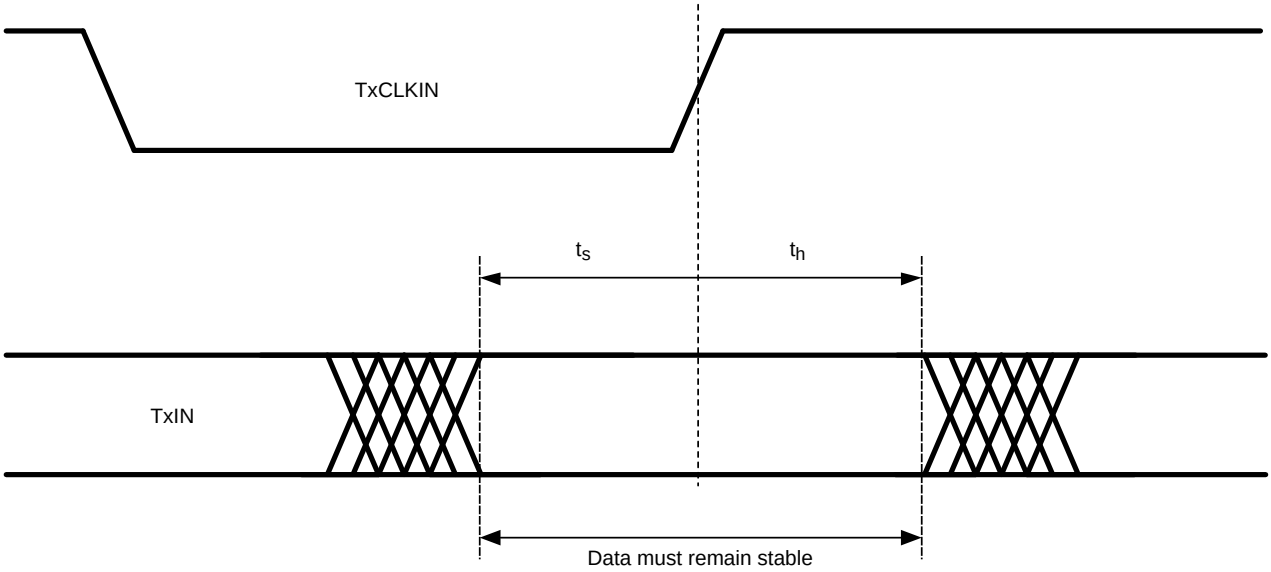

Figure 2. Single Clock Sampling Data Setup and Hold Time

For dual data rate (DDR) interfaces, the clock samples the data on both edges of the clock. CMOS, LVPECL or LVDS interfaces can utilize a DDR interface. The main advantage of DDR interfaces is that the clock and data frequency are identical, which maximizes data throughput for the protocol. The duty cycle distortion of the clock plays a critical part in the setup and hold time as both edges must meet the setup and hold time requirements to sample the data in the mid-bit transition.

Note that if there is skew between the various data lines, or if there is duty cycle distortion of the clock, all of these non-idealities work to reduce the amount of timing margin in the system, so all effort should be taken to reduce inter-pair data skew and clock distortion.

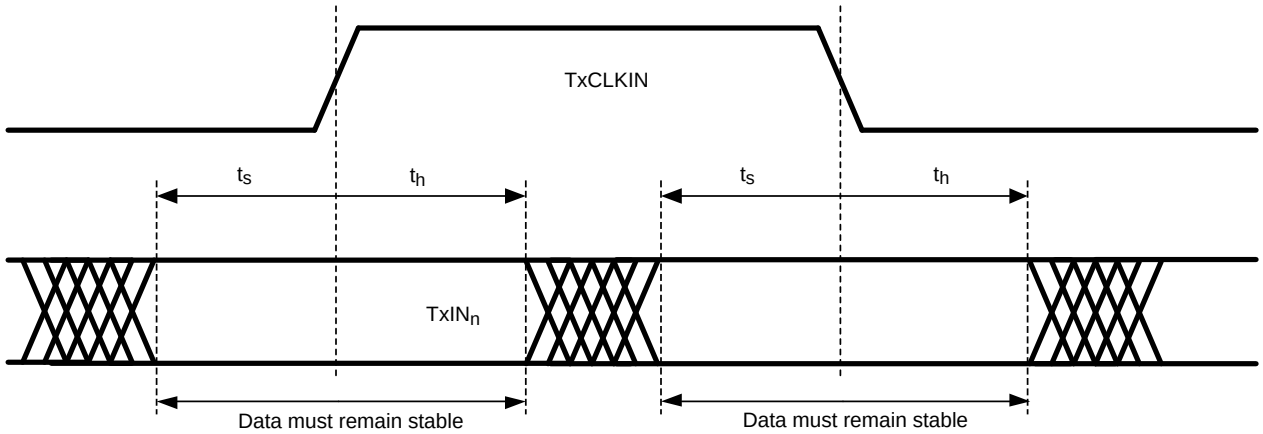

Figure 3. DDR Interface Setup and Hold Time

The LVDS DDR input implementation in the serializer reduces the number of clock/PLL resources required in the host FPGA. The setup and hold time requirements for the LVDS Interface input latch expects the alignment of the clock and data transitions. An additional clock resource is not needed to offset the clock edges in the middle of the data bits.

The numbers that are specified in the data sheet (minimum setup time is -550 ps and the maximum hold time is 900 ps) are worst case numbers and by assuring that each of your data lines meets these timing requirements, you are assuring that the device will properly latch its input data. A negative setup time comes about because within the device there is a delay on the clock line that allows the FPGA to shift out the clock and data on the same clock edge. Internal to the serializer, the clock is shifted to sample the data. When the clock transitions, the actual data that is sampled is the data that was on the input pins a few hundred ps earlier. A graphical explanation of these timings is shown in the Figure 4 and shows a sampling window of 350 ps.

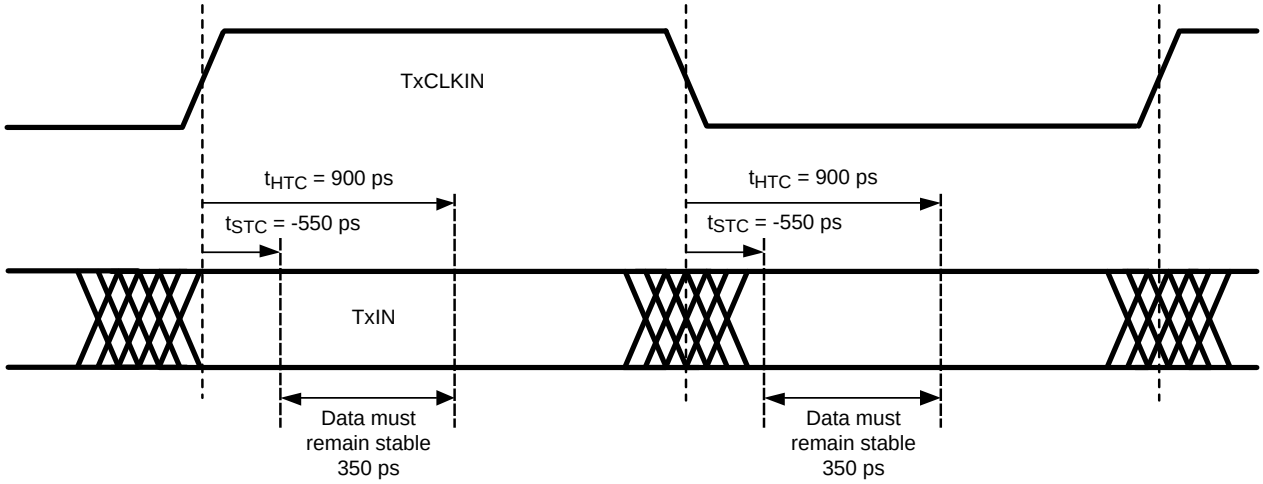

Figure 4. Serializer Setup and Hold Time

3 Serializer Register Programmability

The clock-to-data delay can be optimized by programming register bits in the serializer. This feature allows adjustment of the serializer setup and hold time locations to be optimized to the data valid time provided by the FPGA host device.

Use register 0x30 bits [7:5] to adjust the serializer clock and data delay. The default delay between the clock and data is 725 ps (value 011'b). Each LSB changes the delay by 125 ps that gives a range in delay from 350 ps to 1225 ps.

See Table 1 and Figure 5.

Table 1. Register 0x30 bits 7:5 Setup/Hold Delay Settings (* = default)

Register Setting Reg 0x30 bits [7:5]	Sample Time Instant (ps)	Setup Time (ps)	Hold Time (ps)	Data Valid (ps)
000'b	350	– 175	525	350
001'b	475	– 300	650	350
010'b	600	– 425	775	350
011'b *	**725**	**- 550**	**900**	**350**
100'b	850	– 675	1025	350
101'b	975	– 800	1150	350
110'b	1100	– 925	1275	350
111'b	1225	– 1050	1400	350

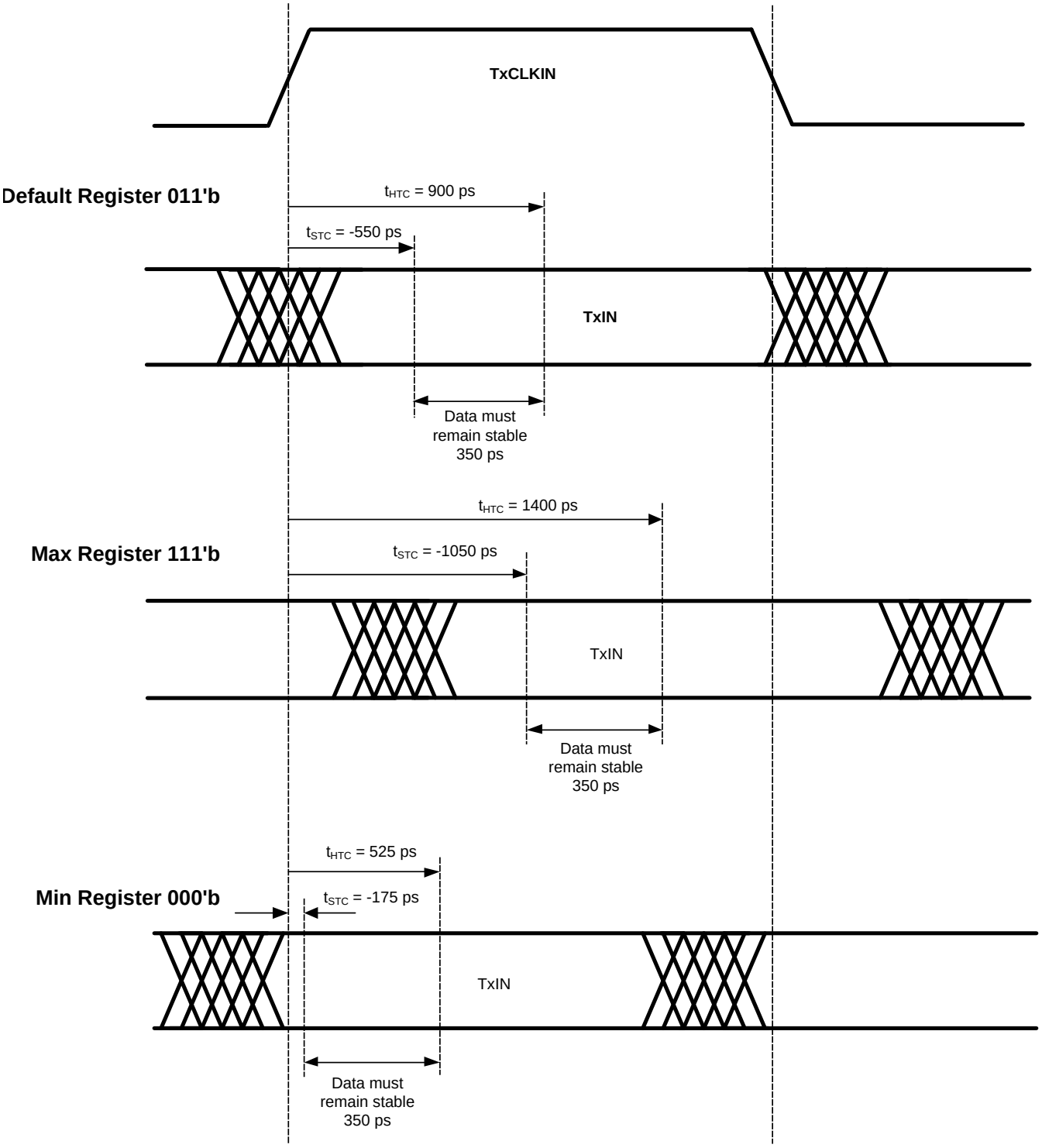

Figure 5. Clock and Data Phase Adjustment

4 Deserializer Device Timing Requirements

For the deserializers (DS32EL0124 and DS32ELX0124), the LVDS clock and data outputs are skewed to provide maximum setup and hold durations for the target FPGA. Further examination of the data sheet reveals the setup and hold times are 800 ps, centering the clock and data at a maximum line rate.

For example, at a maximum line rate of 3.125 Gbps, the LVDS clock rate is 312.5 MHz or 3.2 ns. Divide this by 2 due to the DDR clocking and the data period is 1.6 ns. A setup and hold time at 800 ps puts the clock transition in the mid-bit transition of the data as shown in Figure 6.

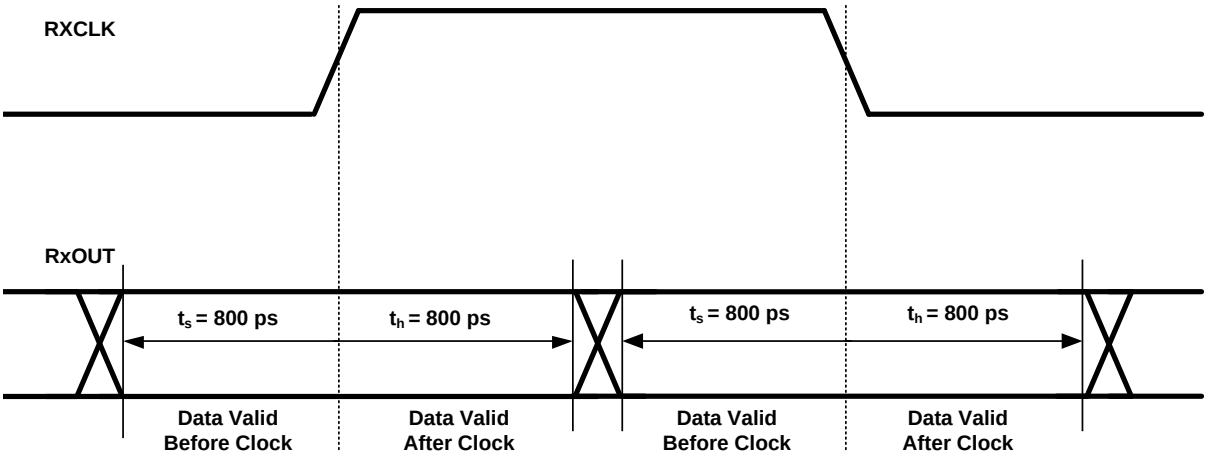

Figure 6. Deserializer (Setup and Hold Time) Data Valid Times

5 Deserializer Register Programmability

Like the serializer, the deserialize can also be optimized to adjust the clock edge location to be compatible with the downstream device's input timing requirement. To adjust the deserializer, use register 0x28. Bits 2 and 3 of register 0x28 adjust the phase in 80 ps steps, which gives 240 ps adjustment. The default value of register 0x28 is 10'b for an 800 ps setup and hold time. The time can be adjusted to a minimum of 640 ps and a maximum of 880 ps. The data valid after clock (Hold) can be set from 960 ps to 720 ps.

The clock phase can also be inverted by bit 4 of register 0x28.

See Table 2 and Figure 7.

Table 2. Deserializer Clock and Data Phase Offset Settings Register 0x28 bits [3:2] (* = Default)

Register Setting Reg 0x28 bits [3:2]	Offset (ps)	Data Valid Before Clock (ps)	Data Valid After Clock (ps)
00'b	160	640	960
01'b	80	720	880
10'b *	**0**	**800**	**800**
11'b	– 80	880	720

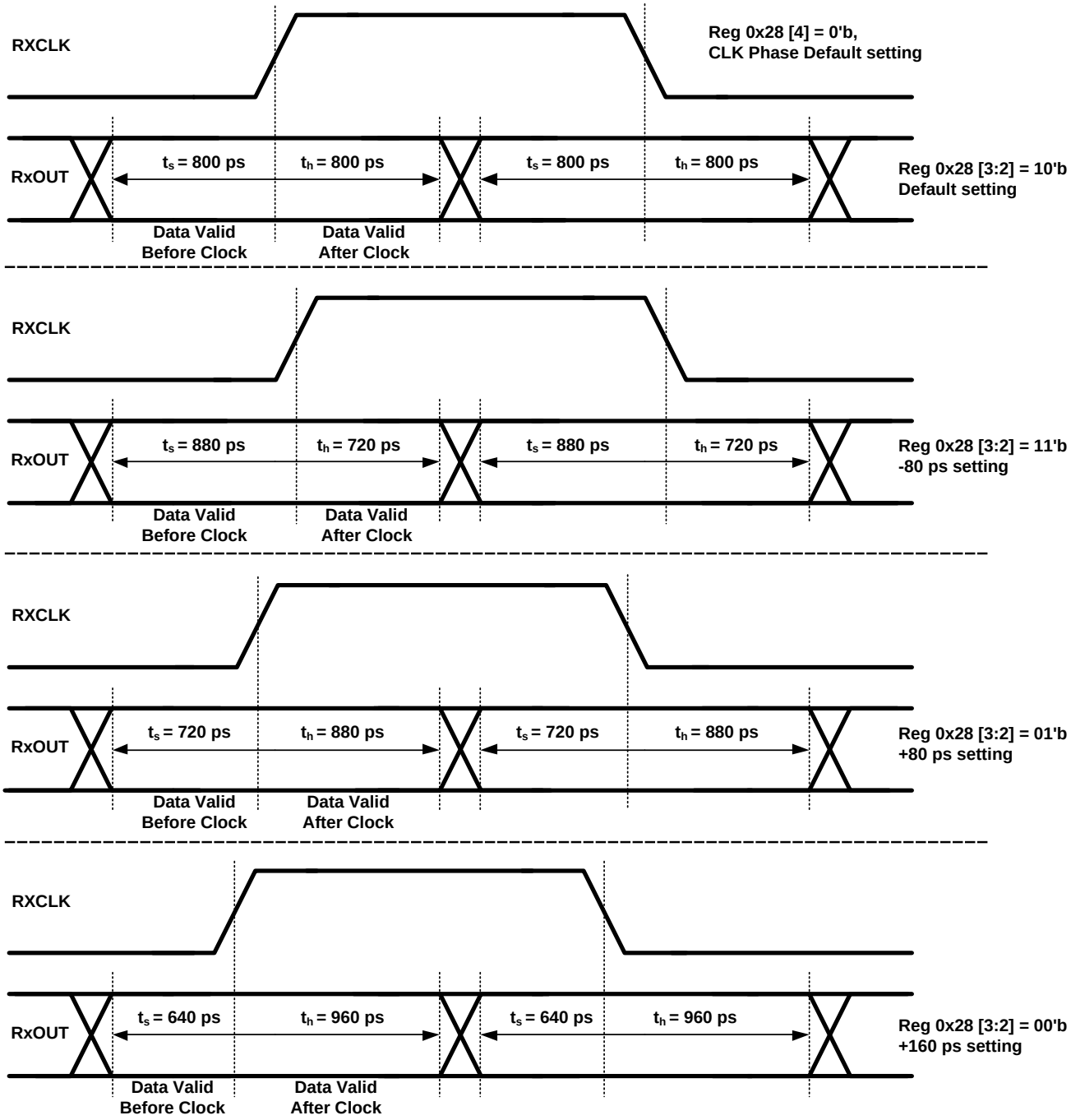

Figure 7. Deserializer (Setup and Hold Time) Data Valid Times Programability

6 Conclusion

In summary, the DDR timing of the FPGA-Link serializers and deserializers have been optimized for use with FPGAs. Further, adjustability of the delay between the clock and data allows you to configure the sampling window or the clock edge to optimize it for specific FPGA requirements.

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