ABSTRACT

The object of this application note is to describe the design requirement of the RS-422 standard and to show that Texas Instruments DS8921, DS8922 and DS8923 Differential Driver and Receiver pair meet all of those requirements.

Contents

1 Introduction .................................................................................................................. 2
2 Balanced Voltage Digital Interface Circuits (RS-422) Requirement .................................................. 2
3 Cable Length ................................................................................................................ 2
4 Modulation Rate ........................................................................................................ 3
5 RS-422 Characteristics ................................................................................................. 3
5.1 The Driver ............................................................................................................... 3
5.2 The Receiver .......................................................................................................... 3
6 DS8921, DS8922 and DS8923 .................................................................................. 4
7 ESDI Enhanced Small Device Interface ........................................................................... 5

List of Figures

1 Data Modulation Rate vs Cable Length .............................................................................. 2
2 RS-422 Balanced Digital Interface Circuit .......................................................................... 3
3 DS8921A Connection Diagram ...................................................................................... 4
4 DS8922A Connection Diagram ...................................................................................... 4
5 DS8923A Connection Diagram ...................................................................................... 4
6 ESDI Timing Diagrams ................................................................................................ 5

List of Tables

1 DM74AS74 Switching Characteristics - 1 ns Clock Skew .................................................. 5
1 Introduction

In system design, due to the distributed intelligence ability of the microprocessor, it is a common practice to have the peripheral circuits physically separated from the host processor with data communications being handled over cables. Usually, these cables are measured in hundreds or thousands of feet. Signals transmitted on these lines (or cables) are exposed to electrical noise sources which may require large noise immunity. The requirements for transmission lines and noise immunity are covered in E.I.A. standard RS-422.

Special circuit design techniques are used to achieve small skew on complementary signals of the driver outputs. In fact, these devices are designed specifically for applications which must meet stringent timing constraints including the ESDI Disk Drive standard. Additionally, the DS8921 series meet the requirement of ST506 and ST412HP standards.

2 Balanced Voltage Digital Interface Circuits (RS-422) Requirement

Balanced circuits are normally used in data, timing, or control applications where the data signaling rate approaches speeds of 10 Mbit/s. In addition, balanced data transmission techniques should be used whenever the following conditions exist:

1. The interconnecting cable is too long for effective unbalanced operation.
2. The interconnecting cable is exposed to a noise source which may cause a voltage sufficient to indicate a change of binary state at the load.
3. It is necessary to minimize interference with other signals.

Figure 2 shows a balanced circuit connection.

There are three major controlling factors in balanced voltage digital interface:

1. The cable length
2. The modulation rate
3. The characteristics of the Driver and Receiver

3 Cable Length

There is no maximum cable length specified in the RS-422 standard. Guidelines are given with respect to conservative operating distances as a function of modulation rate. Figure 1 below is the guideline provided by RS-422 for data modulation rate versus cable length.

![Figure 1. Data Modulation Rate vs Cable Length](image)

The curve is based on empirical data using a 24 AWG, copper conductor, twisted pair cable terminated for worst case in a 100Ω load, with rise and fall time equal or less than one half unit interval at the applied modulation rate.

Even though the maximum cable length between driver and load is a function of data signaling rate, it is also influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds.
Modulation Rate

The balanced (or differential) voltage mode interface will normally be utilized on data, timing or control circuits operating at up to 10 Mbps. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates. The DS8921 family of devices meets or exceeds all of the recommended RS-422 performance specifications.

RS-422 Characteristics

5.1 The Driver

The balanced driver characteristics are specified in RS-422 as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage to the interconnecting cable in the range of 2V to 6V.

2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the two output terminals shall be equal to or greater than 2V, or 50% of the magnitude of VO, whichever is greater. For the opposite binary state the polarity of VT is reversed (VT).

3. During transitions of the driver output between alternating binary states, the differential voltage measured across 100Ω load shall monotonically change between 0.1 and 0.9 of VSS within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall not change more than 10% of VSS from the steady state value until the binary state occurs.

5.2 The Receiver

The electrical characteristics of the receiver are specified in RS-422 as follows:

1. The receiver shall not require a differential input voltage more than 200 mV to correctly assume the intended binary state, over an entire common-mode voltage range of −7 to +7V. The common-mode voltage (VCM) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.

2. The receiver shall maintain correct operation for a differential input signal ranging between 200 mV and 6V in magnitude.

3. The maximum voltage between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal +7V common-mode) in magnitude. Also, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load (up to 10 receivers) shall not have a resistance more than 90Ω at its input points.

6 **DS8921, DS8922 and DS8923**

The DS8921 is a single differential line driver and receiver pair, whereas, the DS8922 and DS8923 are dual differential line driver and receiver pairs. The difference between the DS8922 and DS8923 is in the TRI-STATE® control (Figure 5).

These devices are designed to meet the full specifications of RS-422. The driver features high source and sink current capability.

The receiver will discriminate a ±200 mV input signal over a full common-mode range of ±7V. Switching noise which may occur on input signal can be eliminated by the built-in hysteresis (50 mV typical, and 15 mV min.). An input fail-safe circuit is provided so that if the receiver inputs are open, the output will assume the logical one state.

These devices have power up/down circuitry that will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or down operation.

The most attractive feature of these devices is the small skew between the complementary outputs of the driver, typically about 0.5 ns. This small skew specification is often necessary to meet tight system timing requirements.

---

![Figure 3. DS8921A Connection Diagram](image)
![Figure 4. DS8922A Connection Diagram](image)
![Figure 5. DS8923A Connection Diagram](image)
(1) All times in ns measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the reference or read clock frequency.

(2) Similar period symmetry shall be in ±4 ns between any two adjacent cycles during reading and writing.

(3) Except during a head change or PLO synchronization the clock variances for spindle speed and circuit tolerances shall not vary more than −5.5% to +5.0%. Phase relationship between reference clock and NRZ write data or write clock is not defined.

(4) The write clock must be the same frequency as the drive supplied reference clock (i.e., the write clock is the controller received and retransmitted drive reference clock).

(5) Reference clock is valid when read gate is inactive. Read clock is valid when read gate is active and PLO synchronization has been established.

Figure 6. ESDI Timing Diagrams

Table 1. DM74AS74 Switching Characteristics - 1 ns Clock Skew

<table>
<thead>
<tr>
<th>Parameter</th>
<th>From</th>
<th>To</th>
<th>Conditions</th>
<th>DM74AS74</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>F_{MAX}</td>
<td></td>
<td></td>
<td>V_{CC} = 4.5V to 5.5V</td>
<td>105</td>
<td></td>
</tr>
<tr>
<td>T_{PHL}</td>
<td>Preset</td>
<td>Q or R_{L} = 500Ω</td>
<td>3.3</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>T_{PHL}</td>
<td>or clear</td>
<td>Q or C_{L} = 50 pF</td>
<td>3.5</td>
<td>10.5</td>
<td></td>
</tr>
<tr>
<td>T_{PHL}</td>
<td>clock</td>
<td>Q</td>
<td>3.5</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>T_{PHL}</td>
<td>Q</td>
<td>4.5</td>
<td>9</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

(1) Over recommended operating free air temperature range. All times in ns measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the reference or read clock frequency. All typical values are measured at V_{CC}= 5V, T_{A}= 25°C.

7 ESDI Enhanced Small Device Interface

The ESDI specification requires that the read and Reference Clock must meet the symmetry shown in Figure 6. This necessitates the use of TI's DS8921A/22A/23A series of transceivers.

All specifications are in % T, where

\[ T = \frac{1}{F}, \]

the ESDI specification is assumed to be a 10 Mbits/second standard, \( T = 100 \text{ ns} \).
Given this, the negative pulse width measured at the drive connector must equal $0.5T \pm 0.05T$ (50 ns ± 5 ns). The best available RS-422 driver, other than the DS8921A Family, is specified at ±4 ns differential skew. If the clock is from a high speed 74AS74 device, shown in Table 1, it will have a typical skew of 1 ns.

This combination of 4 ns ±1 ns uses all of the ESDI specified 5 ns and leaves no margin for noise. Use of the DS8921A, 22A, or 23A, specified at ±2.75 ns max. differential skew would allow up to ±2.25 ns for clock skew and noise. This is as close to meeting the ±5 ns spec. of ESDI as is possible with today’s advanced testing systems.

One other consideration is the relationship between Read Clock and Read Data. Figure 6 shows that the positive edge of Read Clock must be 0.31T (31 ns) after the leading edge of Read Data, and 0.31T (31 ns) before the trailing edge of Read Data.

The Read Clock positive edges will be used to strobe Read Data into the controller after both signals go through their respective cable lines and receivers. Use of the DS8922A/23A assures minimum skew between these two signals. Because both drivers, or both receivers, are on the same piece of silicon an optimum match is achieved.

The above is applicable to an ESDI controller as well as the Drive itself. The controller receives the Reference Clock and uses both positive and negative edges to generate WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe out WRITE DATA and the positive edge will strobe WRITE DATA into the Drive.

The WRITE CLOCK positive edge has to be centered within WRITE DATA after it is received by the Drive. The transmitted WRITE CLOCK and WRITE DATA must be as closely matched as possible.

The DS8921A, 22A, and DS8923A devices offer the combination of tightly specified parameters and drivers and receivers on one chip to meet various system timing constraints.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products
- Audio: www.ti.com/audio
- Amplifiers: amplifier.ti.com
- Data Converters: dataconverter.ti.com
- DLP® Products: www.dlp.com
- DSP: dsp.ti.com
- Clocks and Timers: www.ti.com/clocks
- Interface: interface.ti.com
- Logic: logic.ti.com
- Power Mgmt: power.ti.com
- Microcontrollers: microcontroller.ti.com
- RFID: www.ti-rfid.com
- OMAP Applications Processors: www.ti.com/omap
- Wireless Connectivity: www.ti.com/wirelessconnectivity

### Applications
- Automotive and Transportation: www.ti.com/automotive
- Communications and Telecom: www.ti.com/communications
- Computers and Peripherals: www.ti.com/computers
- Consumer Electronics: www.ti.com/consumer-apps
- Energy and Lighting: www.ti.com/energy
- Industrial: www.ti.com/industrial
- Medical: www.ti.com/medical
- Security: www.ti.com/security
- Space, Avionics and Defense: www.ti.com/space-avionics-defense
- Video and Imaging: www.ti.com/video
- TI E2E Community: e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated