SCAN25100

Delay Calibration of Signal Path Interconnect In Remote Radio Head (RRH) Basestations and Other Applications

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Tips, tricks, and techniques from the analog signal-path experts

No. 107

Delay Calibration of Signal Path Interconnect

In Remote Radio Head (RRH) Basestations and Other Applications

— By Dave Lewis, Interface Applications Manager

Calibrating delays through a signal path is growing in importance as systems become faster and more parallel. Often, the system needs to know the delay from the central processing unit to remote A/D and D/A modules and then be able to compensate for any delay variations between one signal path and the others. Example applications where delay calibration may be useful include wireless basestations, radar, satellite, test equipment, medical imaging, particle accelerator equipment, and other high-performance applications. This issue of the *Signal Path Designer* will focus on basestations as an example, to see how National's SCAN25100 serializer/deserializer (SerDes) performs precision delay calibration measurement.

Basestations

There is a growing trend in wireless basestations to move the radio electronics from the basestation to the antennas, increasing radio efficiency, deployment flexibility, and coverage while consolidating DSP and backhaul resources for lower CAPEX and OPEX. These Remote Radio Heads (RRHs), however, can be a challenge to synchronize back to the central basestation "hotel." A second challenge is calibrating every delay path from each antenna to the basestation. This article will examine these two timing challenges in more detail.

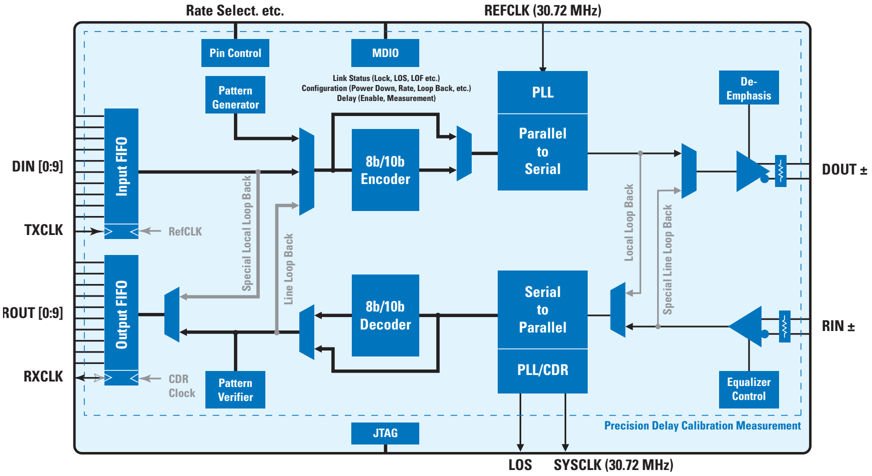

Figure 1. SCAN25100 Next-Generation CPRI SerDes Block Diagram

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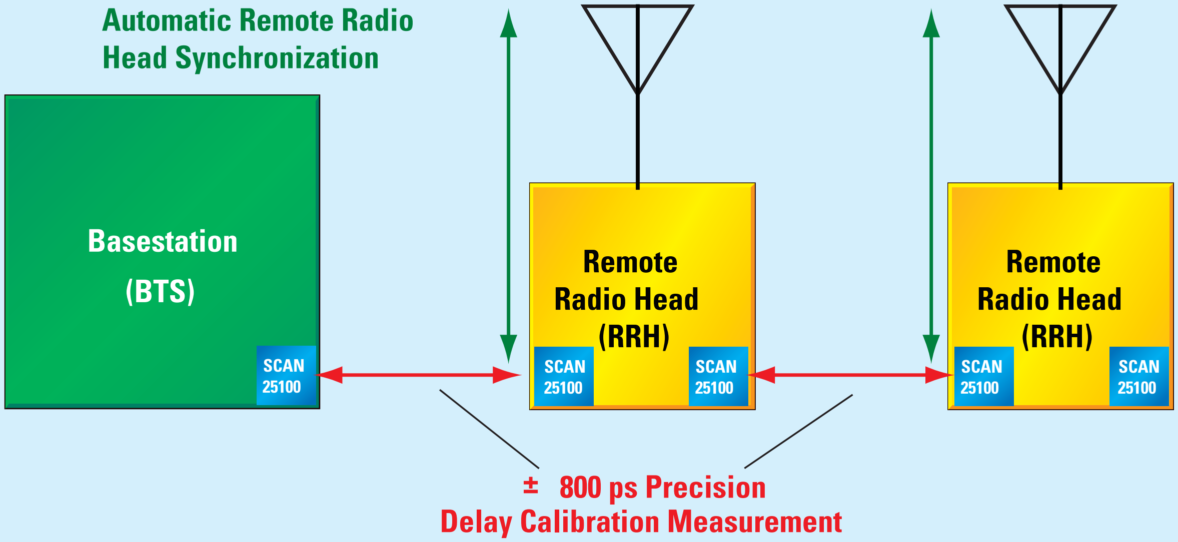
SerDes with Integrated 30.72 MHz Clocking and Precision Delay Calibration Measurement



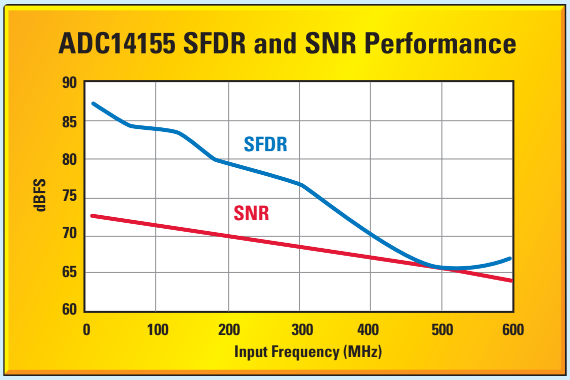
SCAN25100 Features

- 2457.6, 1228.8, and 614.4 Mbps operation
- Exceeds both LV and HV CPRI v2.0 physical interface requirements
- Superior jitter tolerance and link performance
- Precision delay calibration circuitry measures delay with ± 800 ps accuracy
- Deterministic chip latency
- Automatic remote radio head synchronization
- Receiver locks without a reference clock
- Low phase noise 30.72 MHz recovered clock output
- Serializer output jitter independent of Ref$_{CLK}$
- Industrial –40 to +85°C temperature range
- Available in TQFP-100 packaging

1.1 GHz Bandwidth 14-bit, 155 MSPS ADC Enables High IF Sampling

ADC14155 Features

- 1.1 GHz full power bandwidth
- Digitize IFs as high as 450 MHz
- Dual 3.3V and 1.8V supplies for low power consumption
- Duty cycle stabilizer
- Power down mode
- Straight binary or 2's compliment data format
- Internal precision 1.0V reference
- Data ready output clock
- Single or differential clock modes
- Available in LLP-48 packaging



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Delay Calibration of Signal Path Interconnect

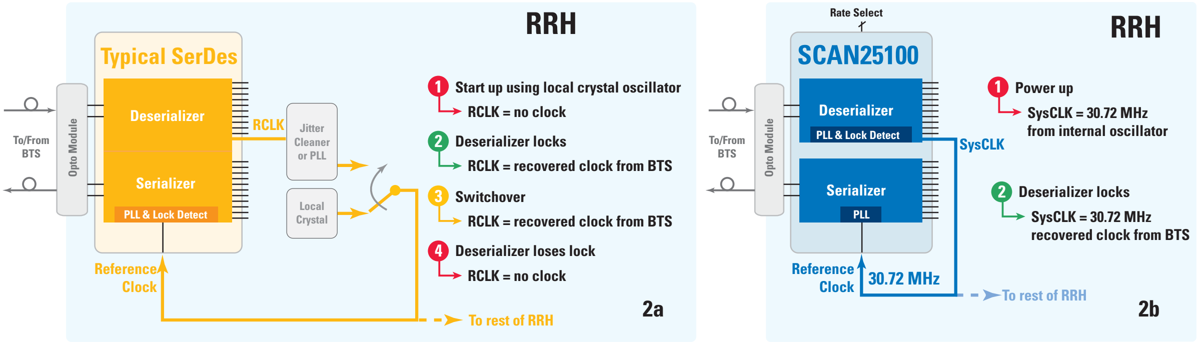

Figure 2a and 2b. RRH Synchronization with Typical SerDes (a), with National's SCAN25100 (b)

RRH Synchronization

During initialization, the system must synchronize the entire network of remote radio heads to the basestation hotel even though the basestation (BTS) and RRHs are often separated by large distances over a serial fiber links. All data, control, and timing is carried by these serial streams—there is no high frequency clock sent in parallel—so each RRH must extract all timing information from the serial link. The RRH first starts up based on a local, on-board clock source. In this mode, it is free running and is not synchronized to the BTS. To synchronize to the BTS, the RRH must transition to its SerDes recovered clock once the SerDes is locked to incoming stream from the BTS. This clock switchover can cause many SerDes devices to lose lock because they use the reference clock to determine if the deserializer still locked. During the clock switch, the deserializer sees a phase and frequency change on reference clock and may decide it is no longer locked *(Figure 2a)*, reverting back to lock acquisition mode. This issue may not occur under all conditions, so it raises reliability concerns in the field.

National's SCAN25100 *(Figure 1)* incorporates separate, independent transmit and receive Phase Lock Loops (PLLs) and on-chip oscillator, enabling the deserializer to acquire lock without a reference clock. It seamlessly automates RRH synchronization through a special clock output called SysCLK. SysCLK reflects the SCAN25100 on-chip oscillator during start up to get the RRH logic up and running, but then transitions to the recovered clock once the deserializer locks to the incoming serial stream *(Figure 2b)*. SysCLK gracefully transitions from on-chip oscillator to recovered clock in order to allow downstream components to track this slight change in frequency. Since SysCLK is a low-noise output, it can be fed directly back to RefCLK in single-hop RRH applications, saving jitter-cleaning cost and complexity.

Figure 1 shows the SCAN25100 has four clocks. The TxCLK and RxCLK are FIFO logic strobes for the parallel bus data timing and don't play a role in serializing or deserializing data. RefCLK, on the other hand, is used by the serializer to serialize data and should be a low jitter clock to minimize jitter on the serialized data stream. Finally, SysCLK reflects the internal on-chip oscillator before deserializer lock and then mirrors the recovered clock from the BTS data stream after deserializer lock. During this frequency transition, TxCLK should be held static high or low to prevent over- or under- flow of the parallel bus FIFO as shown in the typical start-up flow diagram in *Figure 3.*

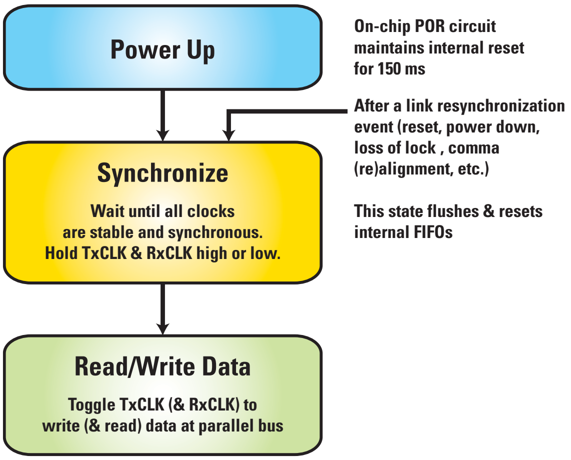

Figure 3. SCAN25100 RRH Synchronization Start-Up Flow

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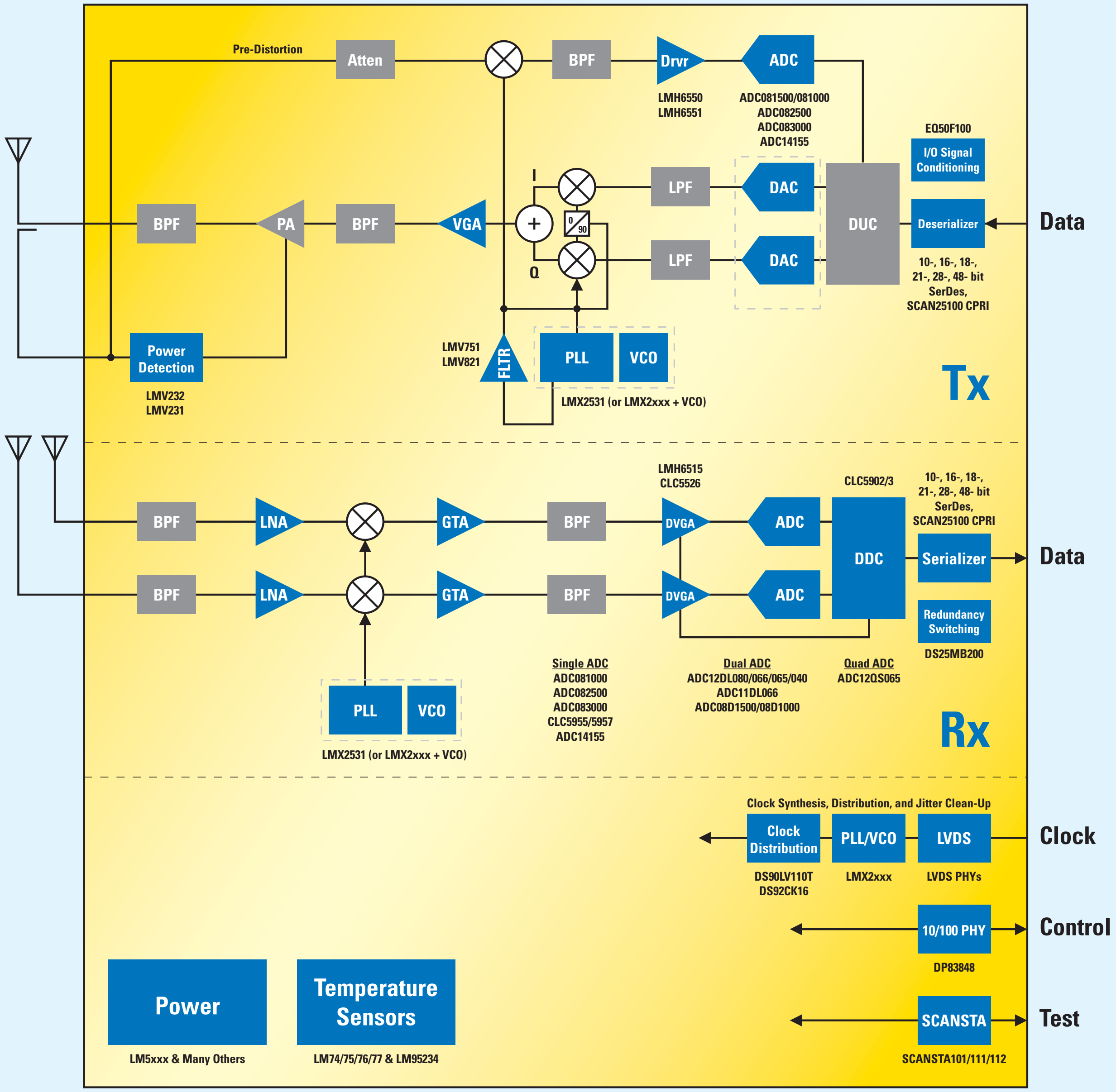
Typical Radio Diagram



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Select Products

High-Speed A/D Converters

Product ID	Resolution	Max Speed (MSPS)	Supply Voltage	Power (mW)	SFDR (dB)	THD (dB)	ENOB (bit)	SNR (dB)	Packaging
14-bit ADCs									
ADC14L040	14-bit	40	3.3	236	90	87	11.9	73	LQFP-32
ADC14155	14 bit	155	3.3	980	84	-81	11.5	71	LLP-48
8-bit ADCs									
ADC081000	8-bit	1000	1.9	1450	59	-57	7.5	48	LQFP-128 exp pad
ADC081500	8-bit	1500	1.9	1200	56	-54.5	7.4	47	LQFP-128 exp pad
ADC082500*	8-bit	2500	1.9	1750	57.5	-55	7.25	45.6	LQFP-128 exp pad
ADC083000*	8-bit	3000	1.9	1800	57.5	-55	7.25	45.6	LQFP-128 exp pad
ADC08D1000	8-bit dual	2000	1.9	1600	55	-55	7.4	47	LQFP-128 exp pad
ADC08D1500	8-bit dual	3000	1.9	1800	56	-54.5	7.4	47	LQFP-128 exp pad
ADC14C105*	14-bit	105	3.3	400	86	82	11.7	72.5	LLP-32

2/2.5G Digital Down Converter (DDC)

Product ID	Description
CLC5903	14-bit input resolution, 78 MSPS DDC with AGC control and 1.8V core supply voltage. Very low 290 mW power consumption. SFDR is 100 dB, SNR is 127 dB, and tuning resolution is 0.02 Hz.

Precision Amplifiers

Product ID	Description	I_{CC}/Ch (mA)	V_{OS} (mV)	GBW (MHz)	Noise (nV/√Hz)	Packaging
LMP7701/2/4	Precision single/dual/quad	0.7	0.2	2.5	9	SOT23-5, MSOP-14, TSSOP-14
LMP7711/12	Precision single/dual	1.15	0.15	17	5.8	SOT23-6, MSOP-10
LM6211	Low noise 5 to 24V single with CMOS input	1.05	2.5	20	5.5	SOT23-5

High-Speed Amplifiers

Product ID	Type	Slew Rate (V/μs, A_V=1)	Small Signal Bandwidth (MHz, A_V=1)	I_{CC} (mA/ch)	2nd/3rd HD (R_L = 100Ω)	Voltage Noise (nV/√Hz)	Packaging
LMH6550	Single differential I/O amplifier	3000	400	20	-78/-88 at 20 MHz	6	SOIC-8, MSOP-8
LMH6551	Single differential I/O amplifier	2400	370	12.5	-94/-96 at 5 MHz	6	SOIC-8, MSOP-8
LMH6702	Single, op amp	3100	1.76 GHz	12.5	-63/-72 at 60 MHz	1.8	SOT23-5, SOIC-8
LMH6703	Single, op amp	4500	1.26 GHz	11	-69/-90 at 20 MHz	2.3	SOT23-5, SOIC-8
CLC5526	Digitally controlled variable gain amplifier	—	350	48.0	-67/-71 at 150 MHz	2.2	SSOP-20

RF Detectors

Product ID	Application	Detector	Channel	Range	Packaging
LMV221*	3G, WCDMA, CDMA, UMTS, TD-SCDMA	Log amp	1	40 dB, 3.5 GHz	LLP-6
LMV232	3G, WCDMA, UMTS, TD-SCDMA	Mean square	2	20 dB, 2.2 GHz	Micro SMD

Interface

Product ID	Mux Ratio	Function	#Ser	#Des	Clock Speed (MHz)	Max Rate/Ch (Mbps)	Max Throughput (Mbps)	Temperature	Packaging	Eval Kit
8b/10b CPRI Basestation SerDes										
SCAN12100	8:1	SerDes	1	1	30.72	614.4, 1228.8		-40 to +85°C	TQFP-100	SCAN25100EVK
SCAN25100	8:1	SerDes	1	1	30.72	614.4, 1228.8, 2457.6		-40 to +85°C	TQFP-100	SCAN25100EVK

Product ID	Function	In-puts	Out-puts	Muxing Options	Input Compatibility	Output	Pre-emphasis (dB)[1]	Receive Equalization (dB)	Max Speed/Ch (Mbps)	Packaging
Buffers										
DS25BR400	Quad CML buffer	8	8	Loopback	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	2500	LLP-60
DS42BR400	Quad CML buffer	8	8	Loopback	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	4250	LLP-60
Multiplexers and Mux-Buffers										
DS25MB200	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2, LB	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	2500	LLP-48
DS40MB200	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2, LB	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	4000	LLP-48

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* Preliminary product information

[1] CML devices in this column that feature de-emphasis show a negative dB

Delay Calibration of Signal Path Interconnect

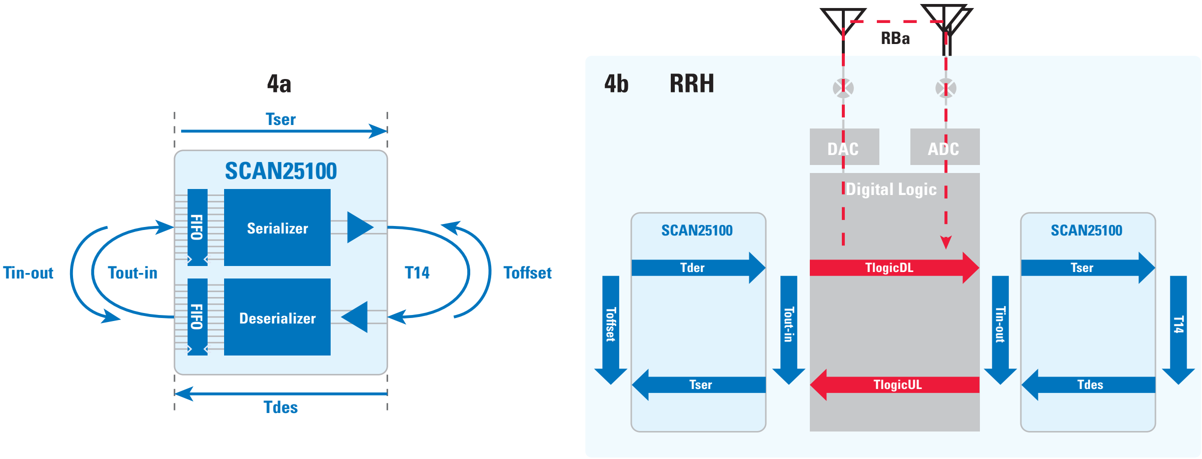

Figure 4a and 4b. SCAN25100 Delay Calibration Measurement Operation (a), Results (b), Intra-RRH Delay Measurement Example

Delay Calibration

After the system powers up and the RRHs are frequency-locked to the BTS, the system must calibrate all delays between RRHs and the BTS to meet air-interface timing requirements. Delay measurement in basestations is usually accomplished using frame timing. For example, the CPRI basestation standard specifies that the delay between an RRH and a BTS is (T14 – T_{OFFSET})/2, where T14 is the delay between transmitting and receiving a hyperframe at the BTS and T_{OFFSET} is the delay between receiving and transmitting a hyperframe at the RRH. Assuming the system is synchronous, hyperframes have fixed length and the RRH-BTS interconnect delay is equal in both directions (e.g. both optical fibers are in one bundle), the interconnect delay is just the difference in hyperframe arrival and departure times measured at each side of the link.

The SCAN25100 simplifies delay calibration by directly reporting T14 and T_{OFFSET} delays as well as its own chip delay *(Figure 4a)*. In addition, the SCAN25100 also measures something National calls $T_{IN\text{-}OUT}$ and $T_{OUT\text{-}IN}$. These delays are just like T14 and T_{OFFSET} but where T14 and T_{OFFSET} are measured at the serial bus, $T_{IN\text{-}OUT}$ and $T_{OUT\text{-}IN}$ are measured at the parallel bus. That means the system can use $T_{IN\text{-}OUT}$ and $T_{OUT\text{-}IN}$ to measure digital logic delays, and with loop back, even delays in the analog RF signal path *(Figure 4b)*.

Delay measurement accuracy requirements for RRH systems are typically on the order of 10 ns, however in multi-hop RRH networks where RRHs are cascaded, delay measurement errors from each hop are additive and higher precision may be required. National's SCAN25100 guarantees T14 and T_{OFFSET} accuracy to better than ± 800 ps while Tser, Tdes, $T_{IN\text{-}OUT}$, and $T_{OUT\text{-}IN}$ are accurate to better than ± 1.2 ns, allowing reliable and precise control over basestation system timing. All delay measurements are performed transparently (the data stream is not interrupted) on request as often as every 5 ms, letting the system track delay changes over the life of the system.

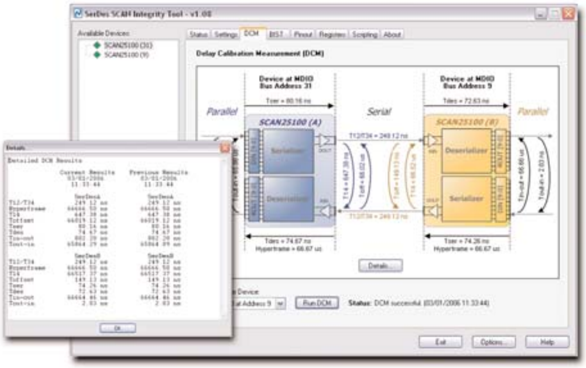

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Figure 5. SCAN25100 Evaluation Software Showing Delay Calibration Measurement Results

Measuring Light

Traditional basestation delays were typically calibrated using special test equipment and were not expected to change significantly over time. Distributed RRH networks, however, cover a wide area and BTS-RRH fiber interconnect delays may change significantly over temperature. For example, a temperature swing from -40° to +40°C on 15 km single mode fiber can result in a ≈37 ns delay shift *(Figure 6)*. This is probably enough to violate basestation timing requirements after just one hop.

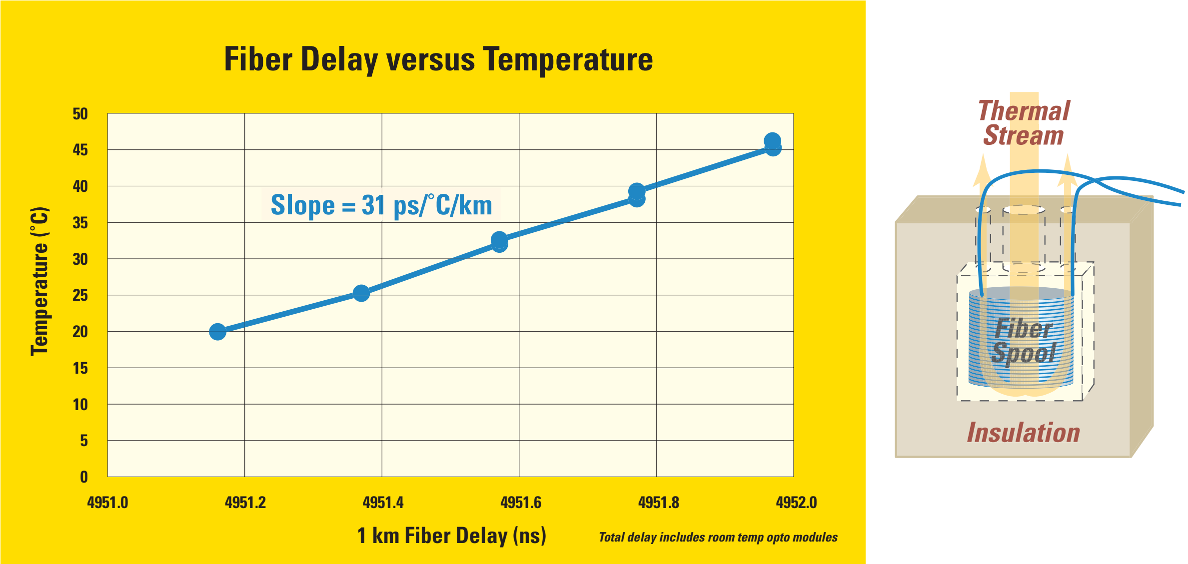
Fiber Delay Variation		31 ps/°C/km
Temperature Range	x	80°C (-40 to +40°C)
Fiber Length	x	15 km
Total Delay Change		**37.2 ns**

Figure 6. Single Mode Fiber Propagation Delay Change Due to 80°C Temperature Shift

The delay measurement resolution or granularity of the SCAN25100 is ≈200 ps delay, enabling it to track small delay variations in RRH fiber links over temperature. To prove this, National conducted an experiment by placing a one kilometer spool of single mode fiber into a well-insulated box while slowly increasing the temperature from about 20°C to 45°C using a SCAN25100 to monitor fiber delay. Experiment results consistently demonstrated a 31 ps/°C/km coefficient *(Figure 7)* which closely agrees with investigations published by particle accelerator physicists.

Conclusion

SCAN25100 automatic synchronization and precision delay calibration ease the design of distributed remote radio basestation systems. Having high delay calibration accuracy also opens the door to new parallel approaches to signal acquisition and processing. For example, in basestations SCAN25100 precision delay calibration measurement can enable wider remote antenna placement via independent RRH links, thereby increasing diversity. In the future, system designers may even coordinate clusters of multi-element antennas to reduce interference while increasing coverage and capacity. The SCAN25100 couldalso be employed similarly in non-basestation applications to match phase and frequency across multiple parallel signal acquisition or signal processing paths. ■



Fiber Delay versus Temperature

Total delay includes room temp opto modules

Figure 7. Experiment results: Using the SCAN25100 to track fiber delay changes over temperature.

Design Tools

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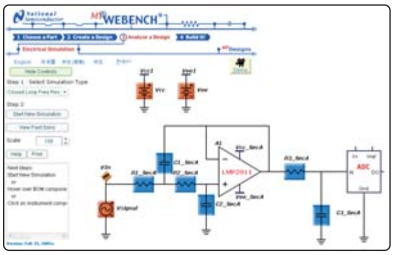

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