Application Report
SNLA261–August 2016

DP83822 Wake-On-LAN

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ABSTRACT

The DP83822 was designed to meet the needs of rugged and high performance applications while still offering a wide range of options for minimizing power consumption. This application note will discuss how the DP83822 Wake-on-LAN works and how to implement each Wake-on-LAN mode.

Contents

1 Introduction

The DP83822 10/100Mbps Industrial Ethernet PHY offers a wide range of power saving modes that can be applied individually or in combination with each other depending on the desired operation. Supported low power modes include:

- Energy Efficient Ethernet – IEEE802.3az
- Wake-on-LAN
  - Magic Packet Detection
  - Magic Packet Detection with Secure-ON
  - Custom Packet Detection
- Low Power Sleep Modes
  - Passive Sleep
  - Active Sleep
- IEEE Power Down
- Deep Power Down

This application note will discuss Wake-on-LAN.

Table 1. Terminology

Acronym	Definition
DUT	Device Under Test
LP	Link Partner
EEE	Energy Efficient Ethernet
WoL	Wake-on-LAN
Opcode	Operation Code
PHY	Physical Layer Transceiver
SMI	Serial Management Interface
IPG	Inter-Packet Gap
LPI	Low-Power Idle
NLP	Normal Link Pulse
TX	Transmit – Digital Pins
RX	Receive – Digital Pins
TD	Transmit – Analog Pins
RD	Receive – Analog Pins

2 Wake-on-LAN

This section discusses the principles behind WoL and implementation of WoL.

2.1 WoL – Principles of Operation

Wake-on-LAN (WoL) is a mechanism that maintains full function of the PHY, but allows for specific frame detection based on the mode of operation desired. By using WoL, backend equipment (i.e. FPGAs, Processors, ASICs, MCUs) can be powered-down until the PHY receives information that passes the specific frame detection criteria. An active link with a LP is maintained in WoL mode. When a qualifying frame is received, the DP83822 can be configured to either send a level change or pulse indication on any of the three GPIO pins. Additionally, the DP83822 allows for interrupt configuration on INT/PWDN_N pin with polarity specification as active HIGH or active LOW.

There are three main WoL functions supported by the DP83822 to allow for user flexibility and security:

- Magic Packet Detection
- Magic Packet Detection with Secure-ON
- Custom Pattern Detection

The DP83822 offers features that allow for a range of security options. The Magic Packet structure is vulnerable to hacks because it only requires one to know the MAC address of the node connected. Magic Packet Detection with Secure-ON adds an additional 6-byte user defined password to allow for extra protection from such attacks. Secure-ON has a Secure-ON Hack Flag that is triggered if a Magic Packet arrives with an invalid Secure-ON password. Additionally, the DP83822 goes even a step further by providing user definable 64-byte sequence frame detection.

2.1.1 Magic Packet Detection

When configured for Magic Packet Detection, the DP83822 scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6-bytes of 0xFF.

2.1.2 Magic Packet Detection with Secure-ON

The DP83822 also offers Magic Packet Detection with Secure-ON for increased security. Secure-ON is a 6-byte user configurable password through register access.

A Magic Packet frame with Secure-ON must also meet the basic requirements outlined in Section 2.1.1.

The specific Magic Packet sequence with Secure-ON consists of 16 duplications of the MAC address of this node, with no breaks or interruptions, followed by Secure-ON 6-byte password. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6-bytes of 0xFF.

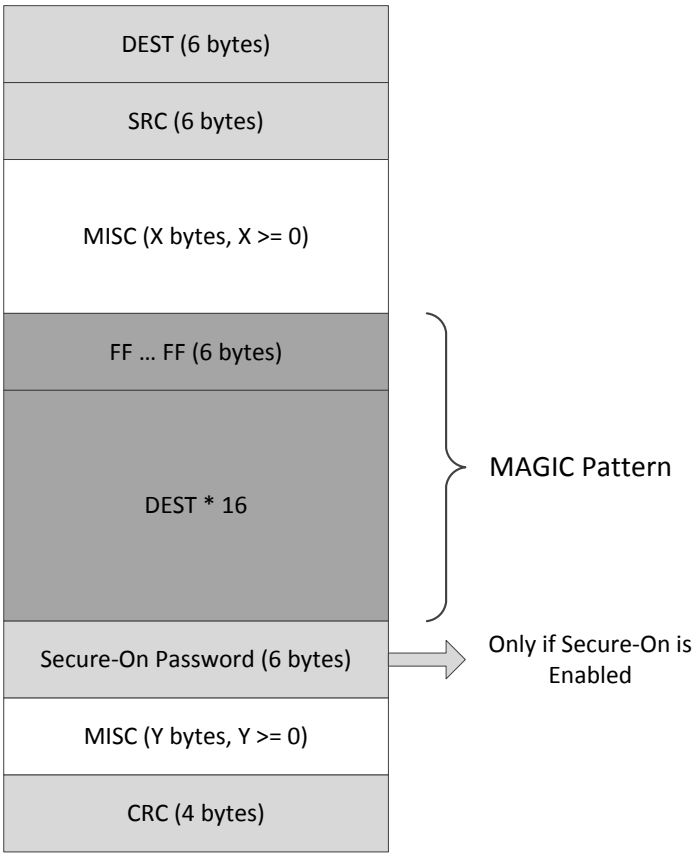

Figure 1. WoL Magic Packet Structure

2.1.3 Custom Pattern Detection

When configured for Custom Pattern Detection, the DP83822 scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Custom Pattern frame.

A Custom Pattern frame does not need to adhere to the basic requirements for LAN technology.

The Custom Pattern frame can be up to a 64-byte sequence that is defined by the user in registers. An optional Byte Mask register within the DP83822 provides more customization by allowing the user to selectively mask the incoming sequence to specify a smaller sequence in the range of 1-byte to 64-byte.

2.2 WoL - Implementation

WoL must be enabled through register configuration using the SMI. All WoL registers are located in the vendor specific register map, which requires the vendor specific DEVAD [4:0] = '11111'.

2.2.1 Magic Packet Detection - Implementation

WoL Magic Packet detection requires use of the following registers:

- Receive Configuration Register (RXFCFG) – address 0x04A0
- Receive Status Register (RXFS) – address 0x04A1
- MAC Destination Address Registers #1-3 (MACDA) – address 0x04A2 to 0x04A4

Two examples Table 2 and Table 3 are intended to display various configuration options for the DP83822 WoL Magic Packet detection feature.

2.2.1.1 Example 1 – Pulse Mode Indication on LED_1

MAC ADDRESS = 00:17:83:E2:FC:73

To enable Magic Packet detection with pulse (32 clock cycles) indication on LED_1 use the following register writes:

Table 2. WoL Magic Packet Configuration Steps; Pulse Mode

Step	Register	Value	Description
1	04A2	1700	MAC Address Bytes 5 and 4
2	04A3	E283	MAC Address Bytes 3 and 2
3	04A4	73FC	MAC Address Bytes 1 and 0
4	0462	0002	Configures LED_1 pin for WoL Indication
5	04A0	0481	WoL Enabled, Pulse Indication, 32 clock cycles

2.2.1.2 Example 2 – Level Change Mode Indication on COL

MAC ADDRESS = 00:17:83:B2:F7:45

To enable Magic Packet detection with level change indication on COL use the following register writes:

Table 3. WoL Magic Packet Configuration Steps; Level Change Mode

Step	Register	Value	Description
1	04A2	1700	MAC Address Bytes 5 and 4
2	04A3	B283	MAC Address Bytes 3 and 2
3	04A4	45F7	MAC Address Bytes 1 and 0
4	0463	0002	Configures COL pin for WoL Indication
5	04A0	0181	WoL Enabled, Level Change
6	04A0	0981	WoL Enabled, Level Change, Clear Level Change

Note: For level change mode, bit [11] in register 0x04A0 will need to be set to '1' to clear the level change indication.

2.2.2 Magic Packet Detection with Secure-ON - Implementation

WoL Magic Packet detection with Secure-ON requires use of the following registers:

- Receive Configuration Register (RXFCFG) – address 0x04A0
- Receive Status Register (RXFS) – address 0x04A1
- Receive Secure-ON Password Registers #1-3 (RXFSOP) – address 0x04A5 to 0x04A7

Table 4 and Table 5 are intended to display various configuration options for the DP83822 WoL Magic Packet detection with Secure-ON feature.

2.2.2.1 Example 1 – Pulse Mode Indication on COL with Secure-ON

MAC ADDRESS = 00:17:83:F3:A1:38
Secure-ON Password = 3C-41-9D-44-BB-5E

To enable Magic Packet detection with Secure-ON using pulse (64 clock cycles) indication on COL use the following register writes:

Table 4. WoL Magic Packet with Secure-ON Configuration Steps; Pulse Mode

Step	Register	Value	Description
1	04A2	1700	MAC Address Bytes 5 and 4
2	04A3	F383	MAC Address Bytes 3 and 2
3	04A4	38A1	MAC Address Bytes 1 and 0
4	04A5	413C	Secure-ON Bytes 0 and 1
5	04A6	449D	Secure-ON Bytes 2 and 3
6	04A7	5EBB	Secure-ON Bytes 4 and 5
7	0463	0002	Configures COL pin for WoL Indication
8	04A0	06A1	WoL Enabled, Pulse Indication, 64 clock cycles

2.2.2.2 Example 2 – Level Change Mode Indication on RX_D3 with Secure-ON

MAC ADDRESS = 00:17:83:DD:23:79
Secure-ON Password = DF-CB-85-68-17-05

To enable Magic Packet detection with Secure-ON using level change indication on RX_D3 use the following register writes:

Note: MAC IF must be in RMII operation since RX_D3 is used in MII and RGMII operation.

Table 5. WoL Magic Packet with Secure-ON Configuration Steps; Level Change Mode

Step	Register	Value	Description
1	04A2	1700	MAC Address Bytes 5 and 4
2	04A3	DD83	MAC Address Bytes 3 and 2
3	04A4	7923	MAC Address Bytes 1 and 0
4	04A5	CBDF	Secure-ON Bytes 0 and 1
5	04A6	6885	Secure-ON Bytes 2 and 3
6	04A7	0517	Secure-ON Bytes 4 and 5
7	0462	0200	Configures RX_D3 pin for WoL Indication
8	04A0	01A1	WoL Enabled, Level Change
9	04A0	09A1	WoL Enabled, Level Change, Clear Level Change

Note: For level change mode, bit [11] in register 0x04A0 will need to be set to ‘1’ to clear the level change indication.

2.2.3 Custom Pattern Detection - Implementation

WoL Custom Pattern detection requires use of the following registers:

- Receive Configuration Register (RXFCFG) – address 0x04A0
- Receive Pattern Registers #1-32 (RXFPAT) – address 0x04A8 to 0x04C7
- Receive Pattern Byte Mask Registers #1-4 (RXFPBM) – address 0x04C8 to 0x04CB

Table 6 is intended to display configuration options for the DP83822 WoL Custom Pattern detection with byte masking.

2.2.3.1 Example – Pulse Mode Indication on COL with Byte Mask

Byte Mask = 00-FF-FF-FF-FF-FF-FF-FF (Masking Byte 8 to Byte 63)
Pattern = 01-23-45-67-89-AB-CD-EF (First eight Bytes programmed, Byte 8 to Byte 63 left to default '0' since they are don't cares)

To enable Custom Pattern detection with pulse (8 clock cycles) indication on COL use the following register writes:

Table 6. WoL Magic Packet Configuration Steps; Pulse Mode

Step	Register	Value	Description
1	04A8	2301	Pattern Bytes 0 and 1
2	04A9	6745	Pattern Bytes 2 and 3
3	04AA	AB89	Pattern Bytes 4 and 5
4	04AB	EFCD	Pattern Bytes 6 and 7
5	04C8	FF00	Byte Mask 0 to 15
6	04C9	FFFF	Byte Mask 16 to 31
7	04CA	FFFF	Byte Mask 32 to 47
8	04CB	FFFF	Byte Mask 48 to 63
9	0463	0002	Configures COL pin for WoL Indication
10	04A0	0082	WoL Enabled, Pulse Indication, 8 clock cycles

3 Conclusion

This application note provided details on the principles behind each WoL mode and the mechanisms to enable each mode in the DP83822.

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