Application Report
SNLA262–August 2016

DP83822 Hardware Rollover

Ross Pimentel

ABSTRACT

The DP83822 was designed to meet the needs of rugged and high performance applications while still offering a back-compatible pin-to-pin replacement for the TLK105, TLK106, TLK105L and TLK106L PHYs. This application note will discuss how to upgrade an existing TLK design to the DP83822 and briefly describe the added features within the DP83822.

Contents

1 Introduction

The DP83822 10/100 Mbps Industrial Ethernet PHY is pin-to-pin compatible with the TLK105, TLK106, TLK105L and TLK106L PHYs. Upgraded features within the DP83822 include:

- 100BASE-FX Support
- 4-Level Bootstraps for Additional Hardware Settings
- MAC Interface Support:
  - MII
  - RMII Slave
  - RMII Master
  - RGMII
- Energy Efficient Ethernet – IEEE802.3az
- Wake-on-LAN
- Short Inter-Packet Gap Support – 120 ns
- Three GPIOs supporting:
  - Multi-purpose LEDs
  - WoL Status Indication
  - Clock Daisy Chain Support
  - IEEE 1588 SFD Indication

Note: In this application note the use of 'TLK' is in reference to the following devices: TLK105, TLK106, TLK105L and TLK106L

Table 1. Terminology

Acronym	Definition
EEE	Energy Efficient Ethernet
WoL	Wake-on-LAN
PHY	Physical Layer Transceiver
SMI	Serial Management Interface
IPG	Inter-Packet Gap
MII	Media Independent Interface
RMII	Reduced-Media Independent Interface
RGMII	Reduced-Gigabit Media Independent Interface
SFD	Start-of-Frame Detection
PU	Pull-Up
PD	Pull-Down

2 DP83822 Replacement of TLK105, TLK106, TLK105L and TLK106L

This section discusses how to upgrade a TLK design with the DP83822.

2.1 Pinout Comparison

The DP83822 is pin-to-pin compatible to the TLK devices. Figure 1 and Figure 2 show Pinouts of both DP83822 and TLK PHYs

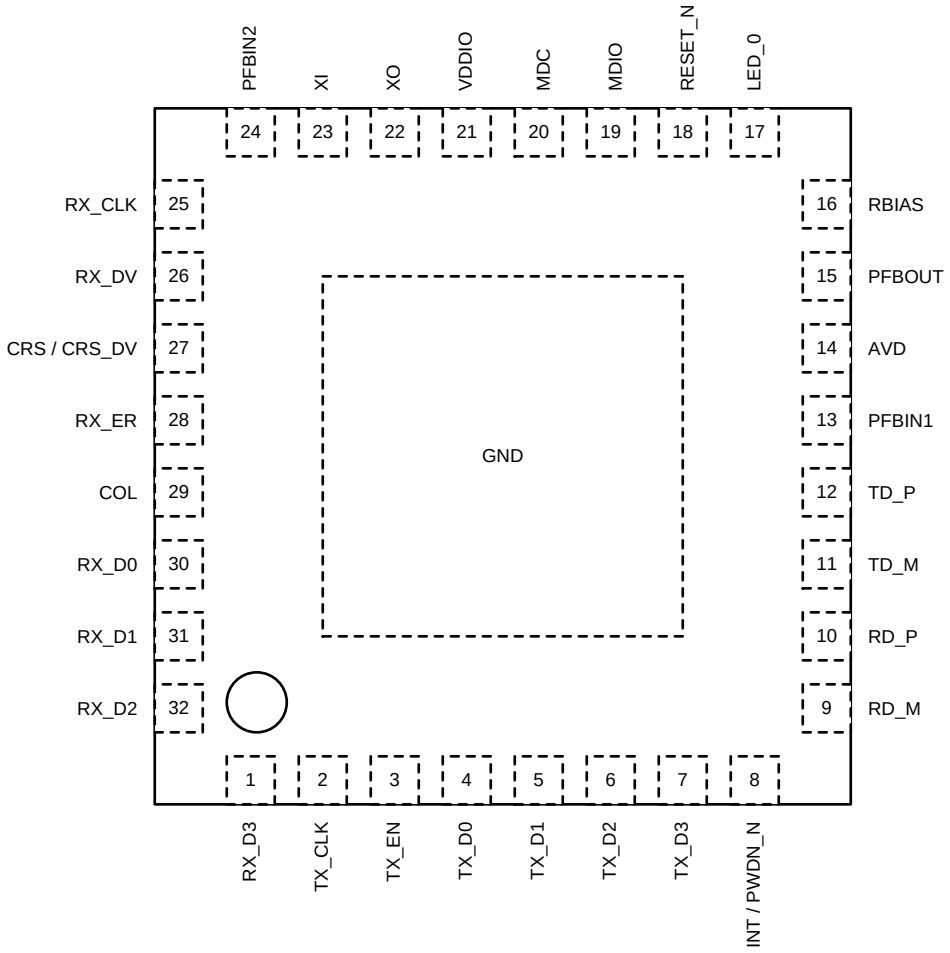

Figure 1. TLK105, TLK106, TLK105L and TLK106L Pinout

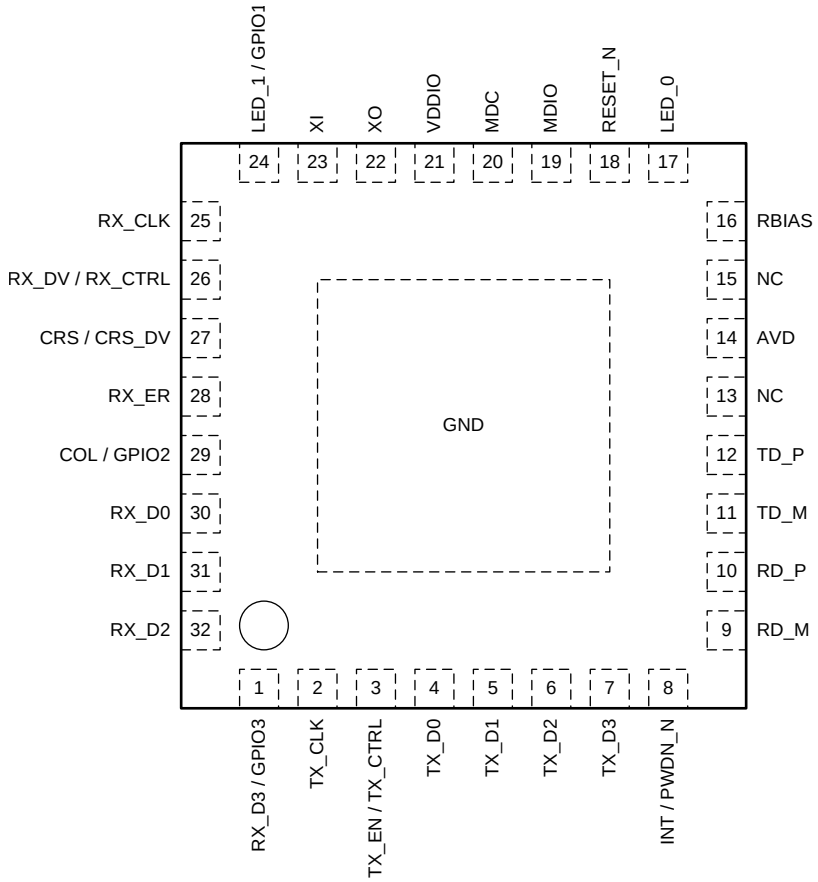

Figure 2. DP83822 Pinout

There are three pins used by the TLK devices that are not used by the DP83822: PFBIN1, PFBIN2 and PFBOUT. The TLK devices use these pins for the 1.55-V supply by either connecting an external supply or using the internal regulator and connecting decoupling capacitors. The DP83822 has an improved internal regulator design, which no longer requires these pins for functional use. By default, pin #24, #15 and #13 are tri-state.

When using an existing TLK footprint, the DP83822 does not require any board modification because the pins are tri-stated; decoupling capacitors can remain as well as an external supply. However, it is recommended to remove such connections to lower BOM cost and footprint size. Additionally, the DP83822 can operate with pin #24, #15 and #13 floating.

2.2 Hardware Bootstrap Configurations

The DP83822 uses 4-level bootstraps for hardware configuration while the TLK devices use 2-level bootstraps. All existing bootstrap modes in the TLKs are the same in the DP83822.

Figure 3 and Figure 4 explain the differences between the DP83822 4-level bootstrap configuration circuits and the TLK 2-level bootstrap configuration circuits.

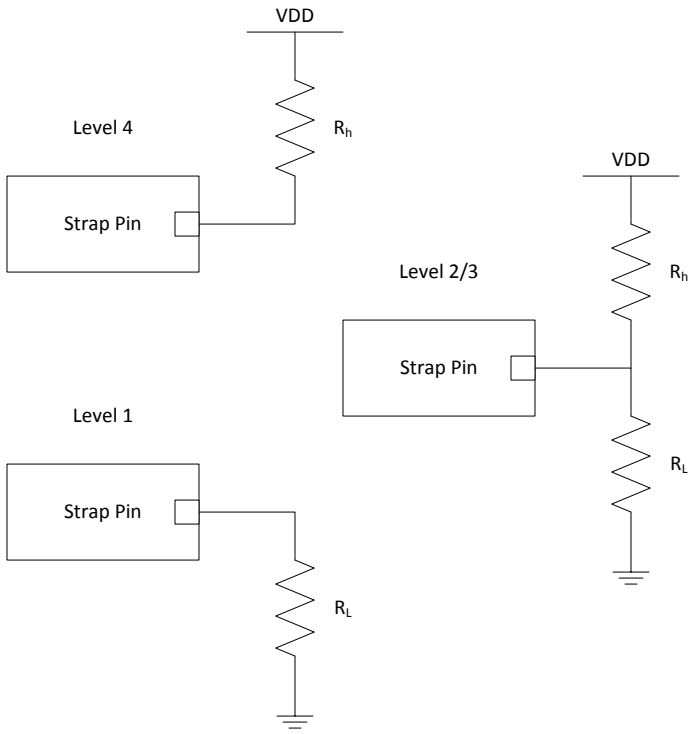

Figure 3. 4-Level Bootstrap Configuration Options (DP83822)

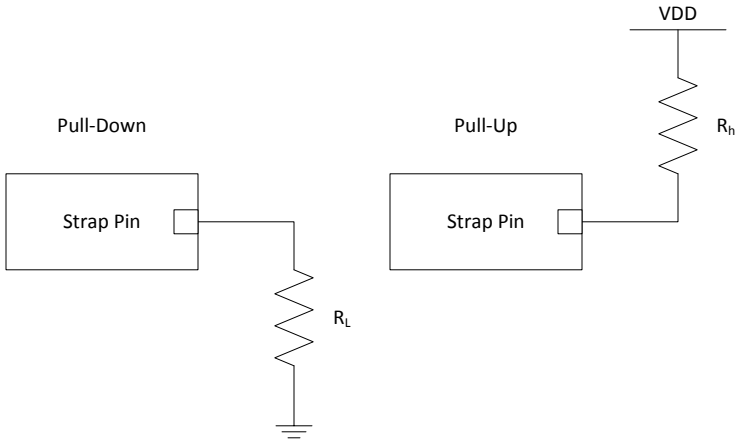

Figure 4. 2-Level Bootstrap Configuration Options (TLK105/TLK106/TLK105L/TLK106L)

Table 2 outlines the additional bootstrap options within the DP83822 and how the options correlate back to the TLK devices.

Table 2. Bootstrap Comparison

Pin Name	Pin Number	Default Level	DP83822 Strap Functions			TLK Strap Functions	
COL	29	4 PU	**Level**	**FX_EN**	**PHYAD_0**	**Level**	**PHYAD_0**
			1	0	0	PD	0
			2	1	0		
			3	1	1		
			4	0	1	PU	1
RX_D0	30	1 PD	**Level**	**AN_1**	**PHYAD_1**	**Level**	**PHYAD_1**
			1	1	0	PD	0
			2	0	0		
			3	0	1		
			4	1	1	PU	1
RX_D1	31	1 PD	**Level**	**EEE_EN**	**PHYAD_2**	**Level**	**PHYAD_2**
			1	0	0	PD	0
			2	1	0		
			3	1	1		
			4	0	1	PU	1
RX_D2	32	1 PD	**Level**	**FLD_EN**	**PHYAD_3**	**Level**	**PHYAD_3**
			1	0	0	PD	0
			2	1	0		
			3	1	1		
			4	0	1	PU	1
RD_D3	1	1 PD	**Level**	**AN_EN**	**PHYAD_4**	**Level**	**PHYAD_4**
			1	1	0	PD	0
			2	0	0		
			3	0	1		
			4	1	1	PU	1
LED_0	17	4 PU	**Level**	**RESERVED**	**AN_0**	**Level**	**AN_0**
			1	X	0	PD	0
			2	X	0		
			3	X	1		
			4	X	1	PU	1
CRS	27	4 PU	**Level**	**LED_SPEED**	**LED_CFG**	**Level**	**LED_CFG**
			1	0	0	PD	0
			2	1	0		
			3	1	1		
			4	0	1	PU	1
RX_ER	28	4 PU	**Level**	**RGMII_EN**	**AMDIX_EN *(SD_DIS)***	**Level**	**AMDIX_EN**
			1	0	0	PD	0
			2	1	0		
			3	1	1		
			4	0	1	PU	1

Table 2. Bootstrap Comparison (continued)

Pin Name	Pin Number	Default Level	DP83822 Strap Functions			TLK Strap Functions	
RX_DV	26	1 PD	**Level**	**XI_50**	**RMII_EN**	**Level**	**RMII_EN**
			1	0	0	PD	0
			2	1	0		
			3	0	1		
			4	1	1	PU	1

Additional DP83822 bootstraps include:

1. FX_EN – 100BASE-FX Enable
2. SD_DIS – Signal Detect input when operating in 100BASE-FX mode
3. AN_1 & AN_EN – Enabling of various Auto-Negotiation Advertise Modes and Forced Modes
4. EEE_EN – Energy Efficient Ethernet (IEEE 802.3az) Enable
5. FLD_EN – Fast Link Drop Enable
6. LED_SPEED – SPEED LED Enable on pin #24
7. RGMII_EN – RGMII Enable
8. XI_50 – PHY Reference Clock Selection (25 MHz when set to ‘0’ or 50 MHz when set to ‘1’)

Please reference the DP83822 Datasheet for more information regarding bootstrap functionality and configuration.

Note: The DP83822 allows for only 5% supply variation on AVD supply and VDDIO supply. TLK PHYs allow up to 10% supply variation. Please ensure that the selected supply is within the DP83822 Recommended Operating Conditions.

Note: The DP83822 uses a reduced power 10BASE-Te line driver design. The TLK PHYs use a 10BASE-T line driver design and will have a higher peak swing. The DP83822 is fully interoperable with 10BASE-T PHY, but when conducting compliance testing 10BASE-Te standards should be used.

3 Upgraded Feature Set

The DP83822 offers added features listed below in a pin-2-pin compatible upgrade to the TLK devices.

3.1 MAC Interface Upgrades

3.1.1 Reduced-Media Independent Interface

The DP83822 supports both RMII Slave and RMII Master modes. In RMII Slave mode, the DP83822 operates off a 50-MHz CMOS-Level oscillator connected to XI pin. In RMII Master mode, the DP83822 can operate off either a 25-MHz crystal resonator connected across XI and XO pins or off a 25-MHz CMOS-Level oscillator connected to XI pin.

The DP83822 RMII modes support all three VDDIO supply rail options (3.3 V, 2.5 V and 1.8 V) while the TLK devices only support 3.3 V and 2.5 V operation.

When the DP83822 is bootstrapped to RMII Master mode (i.e. RMII_EN = ‘1’ and XI_50 = ‘0’), a 50-MHz reference clock will be outputted on RX_D3. This reference output clock should be routed to the connected MAC for error free transmission of data.

3.1.2 Reduced-Gigabit Media Independent Interface

The DP83822 supports RGMII operation, which is not included in the TLK devices. For information regarding the implementation and configuration of RGMII mode, please reference the DP83822 Datasheet.

3.1.3 Integrated Series Termination

The DP83822 has a built-in adjustable series termination network to eliminate the need for external series termination resistors. The series termination can be adjusted by accessing the IO MUX GPIO Control Register (IOCTRL Register, 0x0461). MAC Impedance Control bits[4:1] allow for a range of termination adjustments: 42.5 Ω to 99.25 Ω.

3.2 GPIOs

There are three GPIOs available when using the DP83822. LED_1, RX_D3 and COL pins can all be configured as GPIOs when not used for their default functions. Table 3 outlines various PHY GPIO support based on MAC interface and duplex selection.

Table 3. GPIO Availability Options

MAC Interface	Duplex	Pin Name	Supported Functions
MII	HD	COL	Collision Detection
MII	HD	RX_D3	Receive Data bit[3]
MII	HD	LED_1	GPIO
MII	FD	COL	GPIO
MII	FD	RX_D3	Receive Data bit[3]
MII	FD	LED_1	GPIO
RMII Slave	HD	COL	GPIO
RMII Slave	HD	RX_D3	GPIO
RMII Slave	HD	LED_1	GPIO
RMII Slave	FD	COL	GPIO
RMII Slave	FD	RX_D3	GPIO
RMII Slave	FD	LED_1	GPIO
RMII Master	HD	COL	GPIO
RMII Master	HD	RX_D3	GPIO
RMII Master	HD	LED_1	GPIO
RMII Master	FD	COL	GPIO
RMII Master	FD	RX_D3	GPIO
RMII Master	FD	LED_1	GPIO
RGMII	HD	COL	GPIO
RGMII	HD	RX_D3	Receive Data bit[3]
RGMII	HD	LED_1	GPIO
RGMII	FD	COL	GPIO
RGMII	FD	RX_D3	Receive Data bit[3]
RGMII	FD	LED_1	GPIO

The DP83822 GPIO pins are capable of outputting any of the following configurations:

1. LED Indication
2. Clock Reference
3. IEEE 1588 SFD Pulse or Level Change
4. WoL Status Indication
5. Constant ‘1’ or ‘0’

GPIO configuration is accessible through register access using the LEDs Configuration Register (LEDCFG Register, 0x0460), IO MUX GPIO Control Register #1 (IOCTRL1 Register, 0x0462) and the IO MUX GPIO Control Register #2 (IOCTRL2 Register, 0x0463).

3.3 Low Power Modes

The DP83822 includes the existing Active Sleep, Passive Sleep, and IEEE Power Down low power modes included in the TLK devices. Additionally, the DP83822 offers Wake-on-LAN, Energy Efficient Ethernet and Deep Power Down.

3.4 Industrial Ethernet Features

The DP83822 is designed for ease of use when operating with various Industrial Field Buses. The following features are included in the DP83822 and are not supported by the TLK devices.

3.4.1 Fast Link Drop Bootstrap

The DP83822 can be configured for Fast Link Drop using bootstraps for enabling a <15 μs link drop window. The TLK only allow activation of Fast Link Drop through register access, but the DP83822 allows for configuration in hardware and software.

3.4.2 SPEED and LINK LEDs

The DP83822 can be configured for two LEDs at power-up (LED Speed and LED Link) and three LEDs when using register access. The TLK devices only allow for a single LED at power-up and only two LEDs when using register access.

3.4.3 Short IPG

The DP83822 supports IPG down to 120 ns by default. This allows for even more bandwidth utilization by eliminating additional IDLEs between frames.

3.4.4 Auto-MDIX in Forced Modes

Auto-MDIX is supported when operating the DP83822 in either forced 100BASE-TX or 10BASE-Te modes.

4 Conclusion

This application note provided details on migrating a TLK105, TLK106, TLK105L or TLK106L design to a DP83822 design. Additionally, this application discussed the added features within the DP83822.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265