Application Report
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DS90UB953-Q1 Backwards Compatibility Modes for Operation With Parallel Output Deserializers

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ABSTRACT

The DS90UB953-Q1 is capable of supporting forward channel 28-bit frames combined with an asynchronous back channel that are backwards compatible with either the DS90UB934-Q1 or the previous generation DS90UB914A-Q1 deserializers. This application report describes how to configure the DS90UB953-Q1 to support backwards compatibility modes.

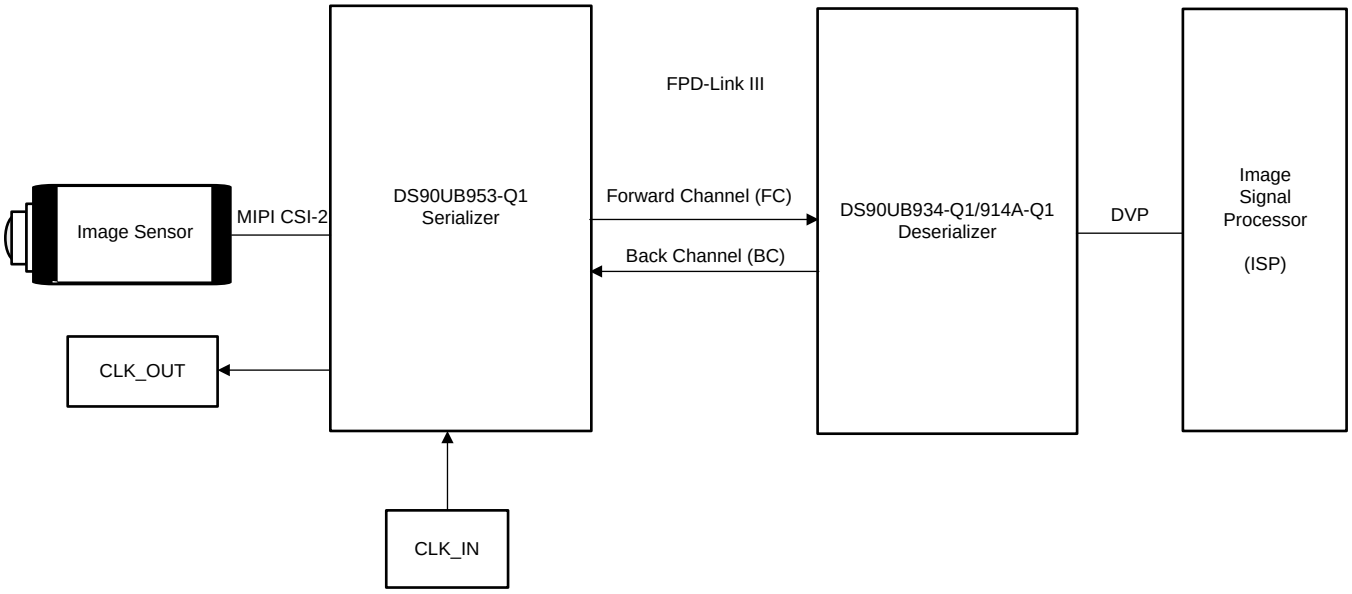

Figure 1. Typical System Block Diagram for DVP Mode Using the DS90UB953-Q1

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Trademarks

1 Introduction

The primary function of the FPD-Link III forward channel transmitter is to transmit sensor data from the serializer to the deserializer. On the DS90UB953-Q1, the FPD-Link III forward channel transmitter can operate in either of two separate modes: standard (40-bit) operation mode, and backwards compatible (28-bit) Digital Video Port (DVP) mode. 28-bit and 40-bit modes refer to the size of the data packets transmitted across the forward channel. The mode used must be compatible with the deserializer for the deserializer to be able to properly receive the transmitted data.

In the standard 40-bit mode, the DS90UB953-Q1 device will operate with deserializers such as the DS90UB954-Q1 or DS90UB960-Q1. In the 28-bit DVP mode configuration, the DS90UB953-Q1 device will operate with DVP parallel output type deserializers such as the DS90UB934-Q1 or the DS90UB914A-Q1. The throughput in DVP mode is significantly slower, and many of the advanced features of the DS90UB953-Q1 are not available when operating in backwards compatible DVP mode. A typical use case for enabling backwards compatibility mode would be connecting sensors with CSI-2 output to existing designs containing DS90UB934-Q1 or DS90UB914A-Q1 deserializers.

To compensate for this slower data rate and emphasis on DVP mode, hardware checks on both the DS90UB953-Q1 and deserializer side must be conducted with verification through software. While many of the hardware settings can be overridden in software, it is important to note that a final system should have the pins strapped to correct settings on power up.

2 Hardware Checks

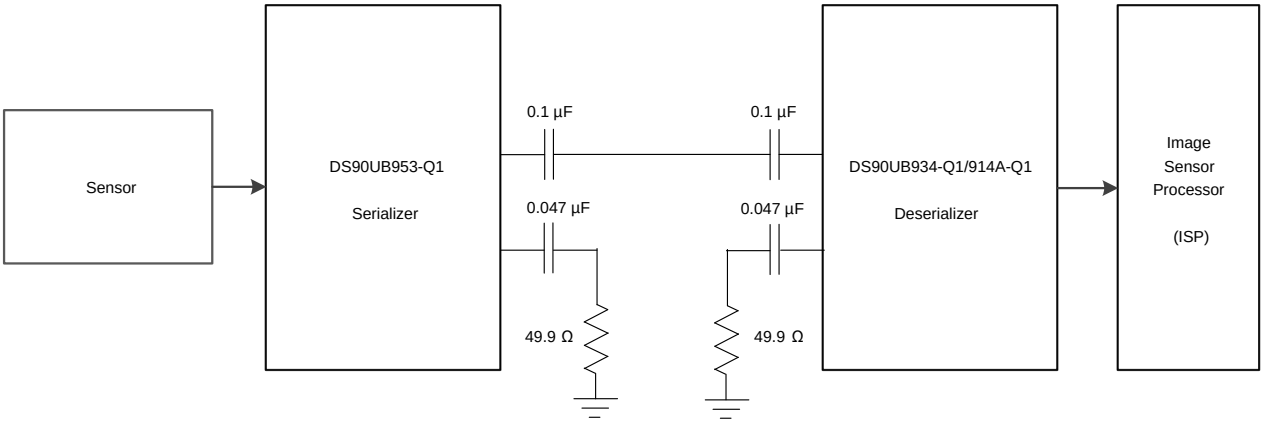

Figure 2. AC Capacitors Needed for DVP Mode

1. Because of lower back channel speed of 2.5-MHz, 100-nF, AC-coupling capacitors on the positive input are needed for both serializer and deserializer sides. To balance the impedance seen at the positive terminals, a 50-nF, or 47-nF capacitor, is used on the negative terminals as well as a 50-Ω, or 49.9-Ω, load to ground. This is shown in Figure 2.
2. TI recommends disconnecting the Power-over-Coax (PoC) network for debugging purposes. Connect an external supply to the serializer locally. The PoC network has to meet return loss profile of <–10 dB at 1 GHz and <–21.8 dB at 2 MHz. More information regarding PoC networks using the DS90UB914A-Q1 can be found in the *Sending Power Over Coax In DS90UB913A Designs* application report (SNLA224). Note that if the design is required to operate in either legacy (28-bit) mode or standard mode, the Power-over-Coax network must be designed to span the frequency range from 20 MHz to over 2 GHz—which can be found in the application note *Power-over-Coax Design Guidelines for DS90UB953-Q1* (SNLA272).
3. The DS90UB953-Q1 contains a Mode pin (21) that straps the DS90UB953-Q1 into a specific clocking mode. Table 1 shows the mode options for the DS90UB953-Q1. Because the DS90UB953-Q1 will be interfacing with the DS90UB934-Q1 or DS90UB934-Q1, the DS90UB953-Q1 must use the DVP mode to use the 28-bit frame. The DVP mode assumes there is an external oscillator on the DS90UB953-Q1 board that is fed into the CLKIN (20) pin of the DS90UB953-Q1. Note that if a DS90UB953-Q1EVM is used a 0 ohm 0201 resistor should be populated at R1 on the DS90UB953-Q1EVM to enable the onboard external clock. Further steps are discussed in the software Section 3.1.

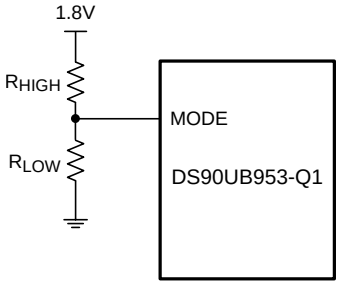

Figure 3. DS90UB953-Q1 MODE Configuration

Table 1. DS90UB953-Q1 MODE Configuration Table

MODE NO.	V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		DESCRIPTION
	V_{MIN}	V_{TYP}	V_{MAX}	$V_{(VDD)}$ = 1.8 V	R_{HIGH} (Ω)	R_{LOW} (Ω)	
1	CSI-2 Synchronous mode – Mode not supported in backwards compatible operation. Please refer to *DS90UB953-Q1 Datasheet* for description of standard operating modes.						
2	CSI-2 Non-synchronous CLK_IN - Mode not supported in backwards compatible operation						
3	0.622 x V_{VDD}	0.668 x V_{VDD}	0.728 x V_{VDD}	1.202	10000	20100	DVP with External CLKIN

4. The DS90UB934-Q1 and DS90UB914A-Q1 deserializers also contain a Mode pin (37). However, the mode pin on the deserializer determines the expected data format: RAW10, RAW12 LF, or RAW12 HF. Note that RAW12 LF is not supported on the DS90UB953-Q1.
5. In addition to defining the data format, the DS90UB934-Q1 mode also selects if the system uses a shielded-twisted pair (STP) or coaxial (Coax) cable between the serializer and deserializer. Finally, make sure the DS90UB934-Q1 is set up for the correct RAW12 HF, or RAW10 data format. Note this strapped setting can be changed in software.

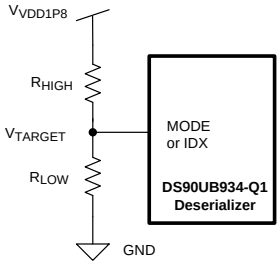

Figure 4. DS90UB934-Q1 Mode Pin Configuration

Table 2. Strap Configuration Mode Select

MODE NO.	V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		COAX/STP	RX MODE
	V_{MIN}	V_{TYP}	V_{MAX}	(V); $V_{(VDD18)}$ = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)		
0-5	Not supported in backwards compatible DVP mode. Please refer to *DS90UB934-Q1 Datasheet* for description of standard operating modes.							
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.42	25.5	95.3	COAX	RAW12 HF
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10	OPEN	COAX	RAW10

6. The DS90UB914A-Q1 can support up to 3 modes: RAW12 LF, RAW12 HF, and RAW10. Note this strapped setting can be overridden in software. For more information about modes, visit Section 6. Note RAW12 LF is not a supported mode with the DS90UB953-Q1.

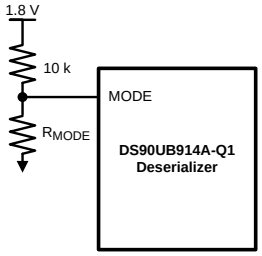

Figure 5. Mode Pin Configuration on DS90UB914A-Q1

Table 3. DS90UB914A-Q1 Strap Configuration Mode Select

MODE SELECT	R_{MODE} RESISTOR VALUE (kΩ)
12-bit low frequency mode (Not supported by DS90UB953-Q1) Please refer to *DS90UB914A-Q1 Datasheet* for description of standard operating modes.	N/A
12-bit high frequency mode 37.5-75 MHz PCLK, 10/12-bits DATA+ 2 SYNC. Note: No HS/VS restrictions (raw).	3
10-bit mode 50–100 MHz PCLK, 10-bits DATA+ 2 SYNC. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles.	11

7. The DS90UB914A-Q1 and DS90UB934-Q1 have Output Enable (OEN) and Output State Select (OSS_SEL) pins, 4 and 5 on both devices respectively, that must be set high for GPIO and data to be active. This is shown in Table 4. These settings can be overridden in software if necessary, consult Section 5 for the DS90UB914A-Q1 and Section 4 for the DS90UB934-Q1.

Table 4. Output States

INPUTS				OUTPUTS			
SERIAL INPUTS	PDB	OEN	OSS_SEL	LOCK	PASS	DATA, GPIO	CLK
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L or H	L	L	L
X	1	0	1	L or H	Z	Z	Z
Static	1	1	0	L	L	L	L/Osc (Register Bit Enable)
Static	1	1	1	L	Previous State	L	L
Active	1	1	0	H	L	L	L
Active	1	1	1	H	Valid	Valid	Valid

3 Software: DS90UB953-Q1 Serializer Settings

3.1 Mode Settings

1. The DS90UB953-Q1 must be placed into DVP mode to be backward compatible with the DS90UB934-Q1 or DS90UB914A-Q1. While the Mode should have been configured using the Mode pin on the DS90UB953-Q1, the register MODE_SEL register 0x03[2:0] can be used to verify or override the current mode. This field always indicates the MODE setting of the device. When bit 4 of this register is 0, this field is read-only and shows the Mode Setting. Mode is latched from strap value when PDB transitions LOW to HIGH and the value should read back 101 (0x5) if the resistive strap is set correctly to DVP External Clock Backwards Compatible Mode. Alternatively when bit 4 of this register is set to 1, the MODE field is read/write and can be programmed to 101 to assign the correct backwards compatible MODE. This is shown in Table 5.

Table 5. DS90UB953-Q1 MODE_SEL (Address 0x03)

BIT(S)	FIELD	TYPE	DEFAULT VALUE	DESCRIPTION
7	RESERVED	RW	0	Reserved
6	RESERVED	S, RW	S	Reserved
5	RESERVED	RW	0	Reserved
4	MODE_OV	RW	0	0: Serializer Mode from the strapped MODE pin 1: Register Mode overrides strapped value
3	MODE_DONE	R	0	Indicates MODE value has stabilized and been latched
2:0	MODE	S,RW	S	This field always indicates the MODE setting of the device. When bit 4 of this register is 0, this field is read-only and shows the Mode Setting. When bit 4 of this register is 1, this field is read/write and can be used to assign MODE. Mode is latched from strap value when PDB transitions LOW to HIGH. Mode of operation: 000: CSI-2 Synchronous Mode (Not supported by the DS90UB953-Q1 for DVP compatible operation) 001: Reserved 010: CSI-2 non-synchronous CLK_IN Mode (not supported by the DS90UB953-Q1 for DVP compatible operation) 101: DVP External Clock Backwards Compatible Mode (requires local clock source)

2. Using DVP External Clock mode requires a certain range of external clock frequencies that depend on RAW10 or RAW12 HF and how many lanes are used. This is tabularized in Table 6 and more specifically in Table 15.
   - RAW10: CLKIN frequency must be between 25 MHz and 66.5 MHz
   - RAW12 HF: CLKIN frequency must be between 25 MHz and 70 MHz, regardless of how many lanes are used.

NOTE: CSI-2 input data provided to the DS90UB953-Q1 must be synchronized to the Input frequency applied to CLKIN when using DVP external clock mode. The PCLK frequency output from the DS90UB934-Q1 or DS90UB914A-Q1 deserializer will also be related to CLKIN when in DVP external clock mode (See Table 15).

Table 6. Mode Summary

953 MODE	914A/934 MODE	REFERENCE SOURCE	REF FREQUENCY (f)	FC DATA RATE	CSI THROUGHPUT	CLK_OUT
DVP External Clock	RAW10	CLKIN (1)	25 - 66.5 MHz	f × 28	f × 20	f × 28 /(HS_CLK_DIV) × (M/N)
	RAW12 HF	CLKIN(1)	25 - 70 MHz	f × 28	f x 18	f x 28/(HS_CLK_DIV) × (M/N)

(1) Local reference clock source is needed. Provide a clock source to the DS90UB953-Q1's CLKIN pin. Calculations in this table assume a CLKIN_DIV (0x05[6:4]) value of 1, the required setting for DVP operation.

3.2 BC and Status Settings

1. Configure DS90UB953-Q1 for RAW10 or RAW12 HF mode using the BC_MODE_SELECT register 0x04. Note 75-MHz RAW12 refers to the mode known as RAW12 HF—as a result the RAW12 LF is not supported by the DS90UB953-Q1. This is shown in Table 7. Note that the same mode must also be selected on the DS90UB934-Q1 or DS90UB914A-Q1 deserializer.

Table 7. BC_MODE_SELECT (Address 0x04)

ADDR (HEX)	REGISTER NAME	BIT(S)	FIELD	TYPE	DEFAULT	DESCRIPTION
0x04	BC_MODE_SELECT	7:3	RESERVED		0x00	
		2	MODE_OVERWRITE_100m	RW	0	28-bit RAW 10 Mode operation Backwards compatible RAW 10 DVP mode (28-bit) is automatically configured by the Bidirectional Control Channel once RX lock has been detected. Software may overwrite the value, but must also set the DVP_MODE_OVER_EN to prevent overwriting by the Bidirectional Control Channel
		1	MODE_OVERWRITE_75m	RW	0	28-bit RAW 12 Mode operation Backwards compatible RAW 12 HF DVP mode (28-bit) is automatically configured by the Bidirectional Control Channel once RX lock has been detected. Software may overwrite the value, but must also set the DVP_MODE_OVER_EN to prevent overwriting by the Bidirectional Control Channel
		0	DVP_MODE_OVER_EN	RW	0	Prevent auto-loading of the backwards compatible DVP mode (28-bit) operation by the Bidirectional Control Channel

2. Set the DVP_CFG register configuration which forces the DS90UB953-Q1 to pass all packets regardless of data type. This is done by changing bit 4 in register 0x10[4] = 1. This register and alternative options are listed in Table 8.

Table 8. DVP_CFG (Address 0x10)

ADDR (HEX)	REGISTER NAME	BIT(S)	FIELD	TYPE	DEFAULT	DESCRIPTION
0x10	DVP_CFG	7:5	RESERVED	R/W	0x0	Reserved
		4	DVP_DT_ANY_EN	R/W	0	When asserted, allows any packet with a Long data type (DT) packet through DVP
		3	DVP_DT_MATCH_EN	R/W	0	When asserted, allows data type matching based on the value in the DVP_DT register. Note: When this bit is asserted, writes to the DVP_DT register are blocked
		2	DVP_DT_YUV_EN	R/W	0	When asserted, allows YUV 10-bit DTs through DVP when mode_100M is also asserted (YUV 10-bit DTs are 0x19, 0x1d, and 0x1f)
		1	DVP_FV_IN	R/W	0	Invert Frame Valid Polarity
		0	DVP_LV_INV	R/W	0	Invert Line Valid Polarity

3. If bit 3 in the DVP_CFG register, DVP_DT_MATCH_EN, was asserted, configure the data type value in the DVP_DT register 0x11. Note this must be a Long data type value for a match occur. DS90UB953-Q1 only supports 10 bit or 12 bit RAW or similar formats in backwards compatible mode. Formats that fall in same structure as RAW10 or RAW12 can be supported. For example, there are 3 YUV types that have the same pixel packing as RAW10 and can also be used: YUV420 10 bit, YUV420 10 bit Chroma shifted or YUV422 10bit. Register 0x10[2] should be set to one in these cases. YUV 8 bit formats are not supported as the CSI-2 pixel packing structure is different from that of RAW10 or RAW12.

Table 9. DVP_DT (Address 0x11)

ADDR (HEX)	REGISTER NAME	BIT(S)	FIELD	TYPE	DEFAULT	DESCRIPTION
0x11	DVP_DT	7:5	RESERVED	R/W	0x0	Reserved
		5:0	DVP_DT_MATCH_VAL	R/W	0x0	When the DVP_CFG.dvp_dt_match_en is asserted, the DVP block will allow packets with this DT through regardless of the mode_75M or mode_100M setting. The DT value must be a Long DT value (either bit 5 or 4 must be set) for a match to occur.

4. After configuring the DS90UB953-Q1 and DS90UB934-Q1 or DS90UB914A-Q1 deserializer appropriately, use the lock and/or pass indicators of the deserializer to monitor the status of the link. These can be found in the PASS and LOCK bits of the DEVICE_STS register 0x04[3:2] on the DS90UB934-Q1 and in the Lock bit of the General Status register 0x1C[0] on the DS90UB914A-Q1. Note that the General Status register 0x52 of the DS90UB953-Q1 does not function the same in DVP mode and will never indicate RX Lock.

3.3 Table of DS90UB953-Q1 DVP Register Settings

Table 10. List of Registers Used for DVP Configuration on DS90UB953-Q1

DEVICE	REGISTER NUMBER	REGISTER NAME	REGISTER DESCRIPTION
DS90UB953-Q1	0x03	MODE_SEL	Used to override and verify strapped value if necessary and configure for DVP with an external CLKIN
DS90UB953-Q1	0x04	BC_MODE_SELECT	Allows DVP mode overwrites to RAW 10 or RAW 12
DS90UB953-Q1	0x10	DVP_CFG	Allows configuration of data in DVP mode. This includes data types like long, YUV, and specified types
DS90UB953-Q1	0x11	DVP_DT	Allows packets with certain data type regardless of RAW 10 or 12 mode if DVP_DT_MATCH_EN is asserted

4 Software: DS90UB934-Q1 Deserializer Settings

1. Verify mode configuration on the DS90UB934-Q1 is the same as the DS90UB953-Q1 by looking at the PORT_CONFIG, 0x6D [2:0]. This is shown in Table 11. Check that the desired port is selected for reads in the RX_READ_PORT bit in the FPD3_PORT_SEL register (0x4C[4]) to ensure that the relevant information is being shown in PORT_CONFIG register.

Table 11. PORT_CONFIG (Address 0x6D)

ADDR (HEX)	REGISTER NAME	BIT(S)	FIELD	TYPE	DEFAULT	DESCRIPTION
0x6D	PORT_CONFIG	7:3	RESERVED	RW	0x0F	Reserved
		2	COAX_MODE	RW, S	0	Enable coax cable mode 0: Shielded-twisted pair (STP) mode 1: Coax mode This bit is loaded from the MODE pin strap at power-up.
		1:0	FPD3_MODE	RW, S	0	FPD3 input mode 00: Reserved 01: RAW12 LF mode (Not supported by the DS90UB953-Q1 in DVP mode) 10: RAW12 HF mode 11: RAW10 mode This field is loaded from the MODE pin strap at power-up.

2. Output Enable (OEN) and Output Sleep State Select (OSS_SEL) must be set high for GPIO and data to be active. These settings can be overridden in the General Configuration register, 0x02[3:2]. This is shown in Table 12
   - Bit [5] must be asserted to override the OEN and OSS_SEL bits.

Table 12. General Configuration (Address 0x02)

ADDR (HEX)	REGISTER NAME	BIT(S)	FIELD	TYPE	DEFAULT	DESCRIPTION
0x02	General Configuration	7	INPUT_PORT_OVERRIDE	RW	0	Input port override bit allows control of the input port selection through the INPUT_PORT_SEL bit in this register.
		6	INPUT_PORT_SEL	RW	0	Input port select. This bit either controls the input mode (if INPUT_PORT_OVERRIDE is set) or indicates the status of this SEL pin.
		5	OUTPUT_OVERRIDE	RW	0	Output Control Override bit. The OUTPUT_ENABLE and OUTPUT_SLEEP_STATE_SEL values typically come from the device input pins. If this bit is set, the register values in the register will be used instead.
		4	RESERVED	RW	1	Reserved
		3	OUTPUT_ENABLE	RW	1	Output enable control (in conjunction with output sleep state select). If OUTPUT_SLEEP_STATE_SEL is set to 1 and this bit is set to 0, the TX output will be forced into a high impedance state. If OUTPUT_OVERRIDE is 0, this register indicates the value on the OEN pin.
		2	OUTPUT_SLEEP_STATE_SEL	RW	1	OSS Select controls the output state when LOCK in low (used in conjunction with Output Enable). When this bit is set to 0, the TX outputs is forced into a HS-0 state. If OUTPUT_OVERRIDE is 0, this register indicates the value on the OSS_SEL pin.
		1	RX_PARITY_CHECKER_EN	RW	1	FPD3 Receiver Parity Checker Enable. When enabled, the parity check function is enabled for the FPD3 receiver. This allows detection of errors on the FPD3 receiver data bits. 0: Disable 1: Enable
		0	RESERVED	RW	0	Reserved

5 Software: DS90UB914A-Q1 Deserializer Settings

1. Verify mode configuration on the DS90UB914A-Q1 is the same as the DS90UB953-Q1 by looking at the Mode and OSS Select register 0x1F [4:0]. This is shown in Table 14.
   - Note bit [4] must be asserted to override the strapped setting.
2. Verify that the expected input is active as the BC will not function properly otherwise. This can be checked by looking at the SEL register 0x4C on the DS90UB914A-Q1 deserializer.

Table 13. DS90UB914A-Q1 SEL Register (Address 0x4C)

ADDR (HEX)	REGISTER NAME	BIT(S)	FIELD	TYPE	DEFAULT	DESCRIPTION
0x4C	SEL Register	7	Pin Channel SEL Override	RW	0	0: SEL pin selects the FPD-III serial input 1: 0x4C[6] selects the FPD-III serial input
		6	Channel SEL	RW	0	OEN configuration from register.
		5	RESERVED			Reserved.

3. Output Enable (OEN) and Output State Select (OSS_SEL) must be set high for GPIO and data to be active. These settings can be overridden in the Mode and OSS select register 0x1F[7:5]. This is shown in Table 14.

Table 14. DS90UB914A-Q1 Mode and OSS Select (Address 0x1F)

ADDR (HEX)	REGISTER NAME	BIT(S)	FIELD	TYPE	DEFAULT	DESCRIPTION
0x1F	Mode and OSS Select	7	OEN_OSS Override	RW	0	Allows overriding OEN and OSS select coming from Pins. 1: Overrides OEN/OSS_SEL selected by pins. 0: Does NOT override OEN/OSS_SEL select by pins.
		6	OEN Select	RW	0	OEN configuration from register.
		5	OSS Select	RW	0	OSS_SEL configuration from register.
		4	MODE_OVERRIDE	RW	0	Allows overriding mode select bits coming from forward-channel. 1: Overrides MODE select bits. 0: Does not override MODE select bits.
		3	PIN_MODE_12–bit HF mode	R	0	Status of mode select pin.
		2	PIN_MODE_10-bit mode	R	0	Status of mode select pin.
		1	MODE_12–bit High Frequency	RW	0	Selects 12-bit high frequency mode. This bit is automatically updated by the mode settings from MODE pin unless MODE_OVERRIDE is SET. 1: 12-bit high frequency mode is selected. 0: 12-bit high frequency mode is not selected. To select 12-bit low frequency mode by register override, set 0x1F[1] = 0x1F[0] = 0
		0	MODE_10–bit mode	RW	0	Selects 10-bit mode. This bit is automatically updated by the mode settings from MODE pin unless MODE_OVERRIDE is SET. 1: Enables 10-bit mode. 0: Disables 10-bit mode.

6 Data Rate Calculations

When creating a system that requires the use of the DVP modes, there are two different approaches that will determine the clocks needed for the system: required throughput or fixed external clock frequency. In both approaches, the data coming from the DS90UB953-Q1 must equal the data going into the deserializer.

When starting with a target throughput, a required image bandwidth for the application drives the need for a specific recovered PCLK and throughput. Since the PCLK and throughput are tied to the data rate, CSI-2 CLK frequency, and CLKIN frequency, these parameters can be calculated. The equation for the output throughput, below, allows the required RX PCLK to be calculated since the number of bits per pixel is set by the mode:

General: output throughput = RX PCLK × # bits/pixel
RAW10: output throughput = RX PCLK × 10
RAW12: output throughput = RX PCLK × 12

Once the RX PCLK has been selected, the required CLKIN can be calculated using the following equation where the ratio is 2 in RAW10 mode and 1.5 in RAW12 mode:

General: RX PCLK = CLKIN × Ratio
RAW10: RX PCLK = CLKIN × 2
RAW12: RX PCLK = CLKIN × 1.5

This CLKIN then determines the CSI-2 throughput of the serializer according to the equations (note that in DVP mode the CSI-2 throughput must exactly match the output throughput):

General: CSI-2 Throughput = CLKIN × Ratio
RAW10: CSI-2 Throughput = CLKIN × 20
RAW12: CSI-2 Throughput = CLKIN × 18

The CSI-2 CLK, CSI-2 data rate, and # of lanes can be chosen to be any values that follow the equations:

CSI-2 Throughput = CSI-2 Data Rate × # of Lanes

CSI-2 Data Rate = 2 × CSI-2 CLK

Conversely, if the CSI-2 CLK or CLKIN frequency is fixed, the appropriate PCLK, data rate, and data throughput can be calculated using the same equations. Note that RAW10 and RAW12 HF will change the equations for each parameter which can be found in Section 6.1.

These can be scaled for higher throughputs, as long as it is within the DS90UB953-Q1 and deserializer limits and the ratios are maintained. It is important that the sensor be synced to the external clock (either directly or by the DS90UB953-Q1 CLKOUT), because a variation or drift in CSI-2 data could cause buffer overflows.

6.1 Examples

Example 1:

RAW10 Ratios: CSI-2 throughput / external clock = 20, RX PCLK/CLKIN = 2

External clock = 25 MHz

CSI-2 data rate = 500 Mbps (either 1 lane at 500 Mbps, or 2 lanes at 250 Mbps, or 4 lanes at 125 Mbps)

Forward channel = 25 MHz × 28 = 700

Example 2:

RAW12 HF Ratios: CSI-2 throughput / external clock = 18, RX PCLK/CLKIN = 1.5

External clock = 25 MHz

CSI-2 data rate = 450 Mbps (either 1 lane at 450 Mbps, or 2 lanes at 225 Mbps, or 4 lanes at 112.5 Mbps)

Forward channel = 25 MHz × 28 = 700 Mbps

6.2 Limits for CLKIN Modes

Table 15. Setup Example Using External CLKIN Mode

SERIALIZER (DS90UB953-Q1)							DESERIALIZER (DS90UB914A-Q1/DS90UB934-Q1)	
	DATA TYPE	CLKIN (MHz)	CSI-2 CLK (MHz)	CSI-2 DATA RATE (Mbps)	# OF LANES	CSI-2 THROUGHPUT (Mbps)	RX PCLK (MHz)	OUTPUT THROUGHPUT (Mbps)
RAW10	MIN	25	250	500	1	500	50	500
		25	125	250	2	500	50	500
		25	62.5	125	4	500	50	500
	MAX	66.5	665	1330	1	1330	133	1330
		66.5	332.5	665	2	1330	133	1330
		66.5	166.25	332.5	4	1330	133	1330
RAW12 HF	MIN	25	225	450	1	450	37.5	450
		25	112.5	225	2	450	37.5	450
		25	56.25	112.5	4	450	37.5	450
	MAX	70	630	1260	1	1260	105	1260
		70	315	630	2	1260	105	1260
		70	157.5	315	4	1260	105	1260

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2017) to A Revision **Page**

- Revised DS90UB953-Q1 MODE Configuration table to clarify that CSI-2 synchronous and non-synchronous modes are not supported in backwards compatible operation. 4
- Fixed datasheet link to be to DS90UB934-Q1 as intended 4
- Removed mention of STP modes for the DS90UB914A-Q1 being incompatible with DS90UB953-Q1. 5
- Added link to DS90UB914A-Q1 datasheet and changed the resistor for RAW12 LF from 0 to N/A 5
- Expanded description of MODE_SEL bits. 5
- Updated MODE_SEL register table to match the latest DS90UB953-Q1 datasheet and to clarify which modes are not supported in backwards compatible operation. 6
- Clarified note about timing of CSI-2 input data in backwards compatible operation 6
- Added explanation of what data types are supported in backwards compatible mode 7
- Removed GENERAL_STATUS register from Table 10. 8

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