Splitter Mode Operations With the DS90UB941AS-Q1

Application Report

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Superframe Splitting With the DS90UB941AS-Q1

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More and more In-Vehicle Infotainment (IVI) systems use multiple displays for delivering entertainment and information content to end users, but using multiple application processors (APs) to drive multiple displays, or developing APs that can drive multiple displays, can be expensive. The DS90UB941AS-Q1 brings functionality that allows designs of more economical IVI system designs with only a single AP for delivering content to two symmetric or asymmetric displays. In these systems, the AP receives and combines two video frames into a superframe while the DS90UB941AS-Q1 performs splitting of the superframe, and forwarding of the resultant frames, to the compatible FPD-Link III deserializers and attached displays.

The DS90UB941AS-Q1 is compatible with the FPD-Link III DS90UB948-Q1, DS90UB928Q-Q1, or DS90UB926QQ1 deserializers, and can supply 1- or 2-lane high-speed serial streams over cost-effective, 50-Ω, single-ended coaxial cables or 100-Ω, differential shielded twisted-pair (STP) and shielded twisted-quad (STQ) cables.

This application report discusses superframe formatting requirements, provides guidance on configuring the DS90UB941AS-Q1 for splitter applications, and gives programming examples.

1.1 Trademarks

All trademarks are the property of their respective owners.

1.2 Introduction

The DS90UB941AS-Q1 splitter and cropping functions allow system designers to use cost-effective IVI systems with only a single AP for delivering content to two symmetric or asymmetric displays. An application processor can receive and combine two video frames into a superframe, and perform the necessary video data formatting to ensure that the data is compatible with the DS90UB941AS-Q1 signal processing functions (see Figure 1-1). The DS90UB941AS-Q1 performs further video formatting and splits of the superframe into two symmetric frames before forwarding them to the compatible FPD-Link III deserializers and attached displays. If necessary, the DS90UB941AS-Q1 can also crop either one or both resultant frames for the formation of asymmetric frames before forwarding the frames to the deserializers and asymmetric displays.

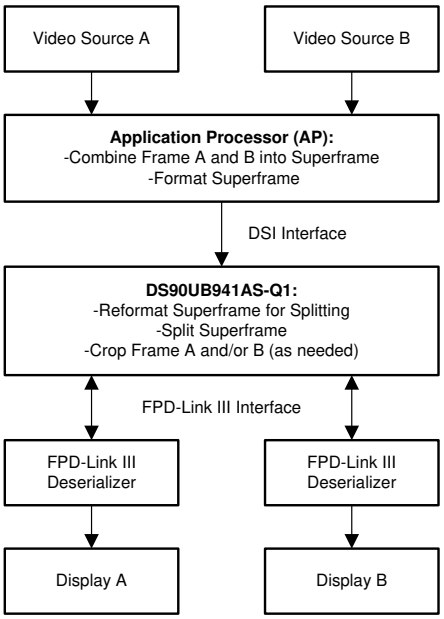

Figure 1-1. Superframe Creation and Splitting System Block Diagram

1.3 Superframe Requirements

The DS90UB941AS-Q1 supports superframe options with the following formats:

- Left/Right 3D format
- Alternate Line 3D format
- Alternate Pixel 3D format

For the first two options, the DS90UB941AS-Q1 reorganizes the superframe into an alternating pixel format for easy splitting at the DS90UB941AS-Q1 output. For the Alternate Pixel option, the superframe is already in the proper format for splitting.

For proper transition between operating modes, only enable 3D modes when the DSI input is disabled.

1.3.1 Left/Right 3D Format

The DS90UB941AS-Q1 can format a superframe as a dual side-by-side (left or right) image consistent with the side-by-side 3D format specified in the HDMI 1.4b specification. The system designer can reprogram the DS90UB941AS-Q1 to reformat the left or right formatted video into a single image with alternating pixels for superframe splitting. The resultant superframe has the same number of lines of the same size, but the pixels are reordered. The DS90UB941AS-Q1 can split the superframe and send the frame to two independent FPD-Link III deserializers.

The following are requirements for proper operation:

- Images must have identical video format (lines, pixels, blanking intervals).
- Pixel clock used must be twice the frequency as required for sending a single image.
- Horizontal blanking components (front porch, sync period, back porch) must be twice the number of pixels as required for a single image.
- Vertical blanking periods must be the same number as required for a single image. Note that the total time spent on vertical blanking in the dual image is twice that of the time spent in the single image, as the vertical blanking happens for two times the number of lines in a single image.
- The maximum line size allowed for the combined image is 8191 pixels (24-bit).

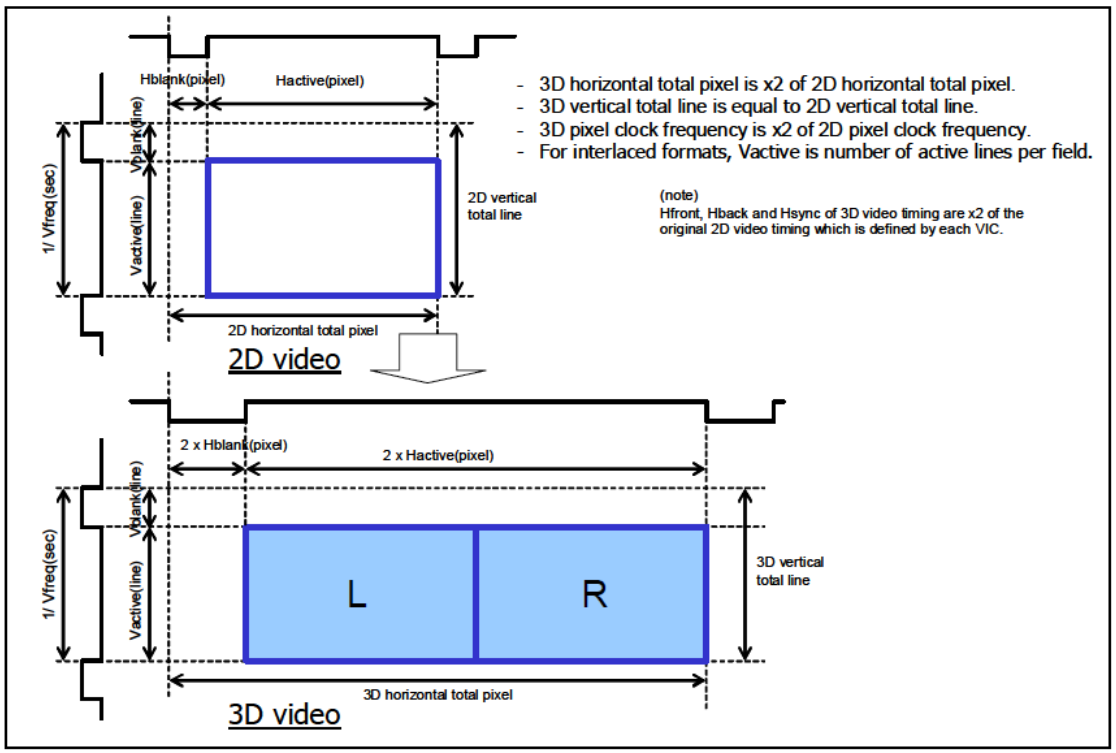

Figure 1-2. HDMI 1.4b Side-by-Side (Full) 3D Format

The system designer can set the LEFT_RIGHT_3D register bit in the BRIDGE_CFG2 register (register 0x56[7]) to enable left or right input mode. Software must also set the 2D image line size, IMG_LINE_SIZE (registers 0x32 and 0x33), as well as the IMG_DELAY control (registers 0x34 and 0x35). The IMG_DELAY is used to properly delay image regeneration, and is typically set to a small value (for example, 12 clocks). IMG_LINE_SIZE is used to configure the active line size, and is set to 1280 pixels by default to align with the default 720p60 timing (1280x720 at 60 fps).

The designer can also monitor the left or right video processing in the VIDEO_3D_STS register (register 0x58).

1.3.2 Alternate Line 3D Format

The DS90UB941AS-Q1 can format a superframe as a dual-image with alternating lines consistent with the Alternate Line 3D format specified in the HDMI 1.4b specification. The DS90UB941AS-Q1 can be programmed to reformat the alternate line formatted video into a single image with alternating pixels for superframe splitting. The resultant superframe has half the number of video lines that are twice the length. This superframe can be split by the DS90UB941AS-Q1 at the FPD-Link III output and send the new frames to two independent deserializers.

The following are requirements for proper operation:

- Images must have identical video format (lines, pixels, blanking intervals)
- Pixel clock used must be twice the frequency as required for sending a single image
- Vertical blanking components (front porch, sync period, back porch) must be twice the number of video line periods as required for a single image.
- Horizontal blanking periods must be the same number of pixels as required for a single image. Note that the total time spent on horizontal blanking in the dual image is twice that of the time spent in the single image, as the horizontal blanking happens for two times the number of lines in a single image.
- The maximum line size allowed is 4095 pixels (24-bit).

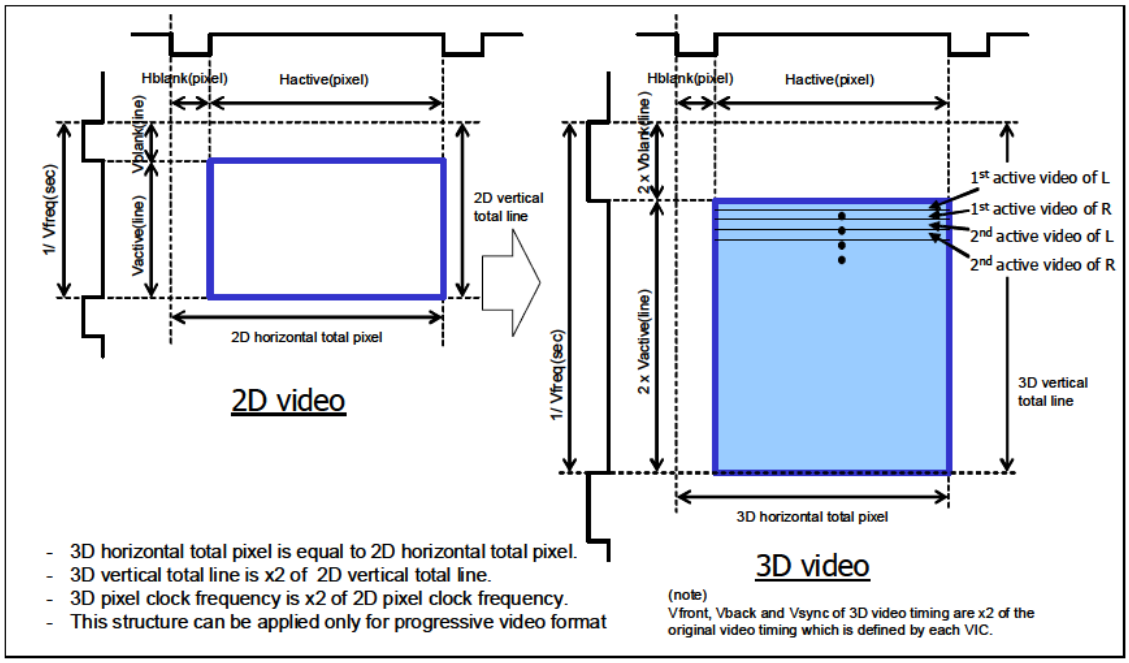

Figure 1-3. HDMI 1.4b Alternate Line 3D Format

The designer can set the ALT_LINES_3D register bit in the BRIDGE_CTL register (register 0x4F[4]) to enable the alternate line mode.

Alternate Line video processing status can be monitored in the VIDEO_3D_STS register (register 0x58).

1.3.3 Alternate Pixel 3D Format

The DS90UB941AS-Q1 formats a superframe as a dual-image with alternating pixels. The DS90UB941AS-Q1 does not require any special processing on this image format. This superframe can be split by the DS90UB941AS-Q1 and sent to two independent deserializers.

The following are requirements for proper operation:

- Images must have identical video format (lines, pixels, blanking intervals).
- Pixel clock used must be twice the frequency as required for sending a single image.
- Horizontal blanking components (front porch, sync period, back porch) must be twice the number of pixels as required for a single image.
- Vertical blanking periods must be the same number as required for a single image. Note that the total time spent on vertical blanking in the dual image is twice that of the time spent in the single image, as the vertical blanking happens for two times the number of lines in a single image.
- The maximum line size allowed is 4095 pixels (24-bit).

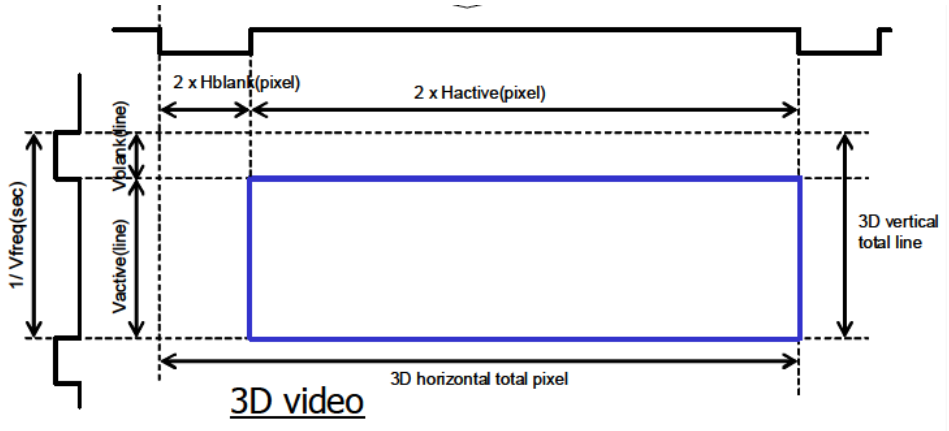

Figure 1-4. HDMI 1.4b Alternate Pixel 3D Format

Alternate Pixel mode is the default mode of operation for the DS90UB941AS-Q1.

If splitter mode is enabled, there are two options to properly regenerate Horizontal Sync timing. The preferred option is to use the default setting for the IMG_DELAY, and enable a register override of the Horizontal Sync and Horizontal Back porch periods for each port using the IMG_HSYNC_CTLx registers. Front Porch value may be determined from total line length - (Active line length + Horizontal Back Porch + Horizontal Sync). The second option is to allow automatic generation of the Horizontal Sync timing and set the IMG_DELAY value in registers 0x34 0x35 to greater than the Horizontal Sync period plus the Horizontal Back Porch period for the 3D image in pixels.

1.4 Video Processing Status Monitoring

The VIDEO_3D_STS register may be used to monitor the Left/Right video and Alternate Line video processing status for errors. If any processing error occurs, the register field is set to 1 and only cleared on read. It is important to read the register carefully based on the different splitting configuration for the LINE_MISMATCH field.

1.4.1 VIDEO_3D_STS Register (Address = 58h) [reset = 0h]

VIDEO_3D_STS is described in Table 1-1.

Table 1-1. VIDEO_3D_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	LINE_OV_ERR	R/RC	0h	Line Buffer Overflow: When set to a 1, an error has been detected in the 3D video line buffers due to receiving a video line that was too long for the buffer. For Alternate Line 3D mode, this flag is set if a video line contains 4096 or more pixels. For Left/Right 3D, or Alternate Pixel 3D modes, this flag is set if a video line contains 8192 or more pixels. This flag will be cleared on read.
1	LINE_VID_ERR	R/RC	0h	Line Video Error: When set to a 1, an error has been detected in the 3D video processing likely due to invalid line length or blanking intervals. This flag is cleared on read.
0	LINE_MISMATCH	R/RC	0h	Line Mismatch Error. Alternate Line 3D mode: When set to a 1, odd or even video line length mismatch has been detected. This occurs if the odd and even lines of a video are note the same length. This flag is cleared on read. Left/Right 3D mode: When set to a 1, a line length error has been detected. This occurs if the received video line is not twice the IMG_LINE_SIZE value. If the received line length is less than IMG_LINE_SIZE, an error may not be detected. This flag is cleared on read. If the image is cropped in the horizontal dimension, this error flag may not be accurate.

1.5 Superframe Splitting

The superframe may be split at the DS90UB941AS-Q1, as shown in Figure 1-5. Splitter options must be configured prior to enable to enabling DSI inputs. This ensures the device enters the appropriate mode prior to forwarding video. Splitter mode can be enabled by either register settings or strap mode. For register settings, select the Forced Splitter Mode selection on the FPD3_TX_MODE control in the Dual_CTL1 register (0x58 [2:0] = 111). Mode_SEL [1:0] can be configured for splitter mode based on the voltage ratio set by the pullup and pulldown resistor. The *Device Functional Modes* section of the *DS90UB941AS-Q1 data sheet* provides information on the hardware configuration.

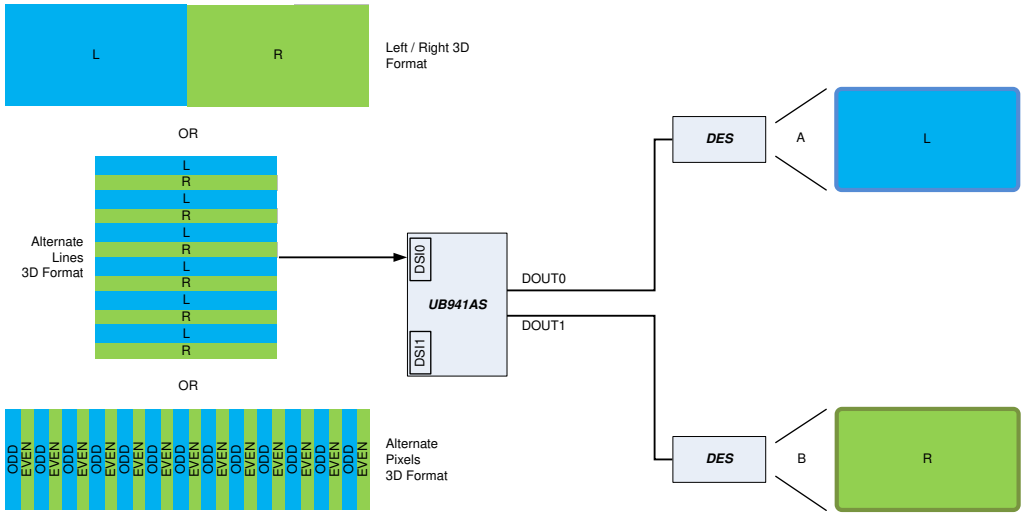

Figure 1-5. Symmetric Splitting

1.6 Frame Cropping

Asymmetric splitting of frames can be accomplished by cropping the resultant output images. The input video requirements are the same as those for the symmetric splitting. The superframe must include two identical size images. Those images are cropped in both the horizontal and vertical dimensions to produce reduced size images. Note that the clock frequency remains half the frequency of the superframe. In addition, the horizontal and vertical blanking intervals are increased by the magnitude of the cropping.

Figure 1-6 shows one superframe stream input on the DSI0 (DSI1 also possible) that is split into two different video resolutions. When the superframe is received, it is reformatted to the alternate pixels 3D format before the superframe is split into two images. The cropping function is then performed on either one or both of the resultant images to get the desired resolutions before the images are forwarded to the compatible deserializers and attached displays.

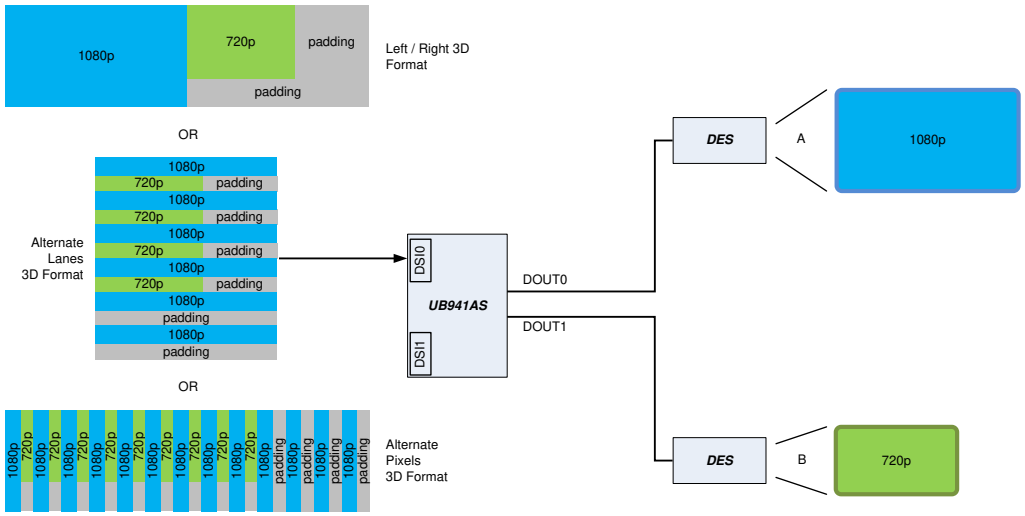

Figure 1-6. Asymmetric Splitting With Cropping

The engineer can enable image cropping on each image to handle asymmetric splitting. To crop each image, the engineer must program the horizontal and vertical dimensions in the registers described in Section 1.6.1. The origin of the frame begins at the start of the active video as shown in the figure below. Typically, for asymmetric split, the difference between the active videos in both horizontal and vertical dimensions is added to the front porch of the smaller video. However, in the SuperFrame image, the resultant image can be offset such that the front porch and back porch can have different values. shows the relation between the resultant crop image and the blanking parameters.

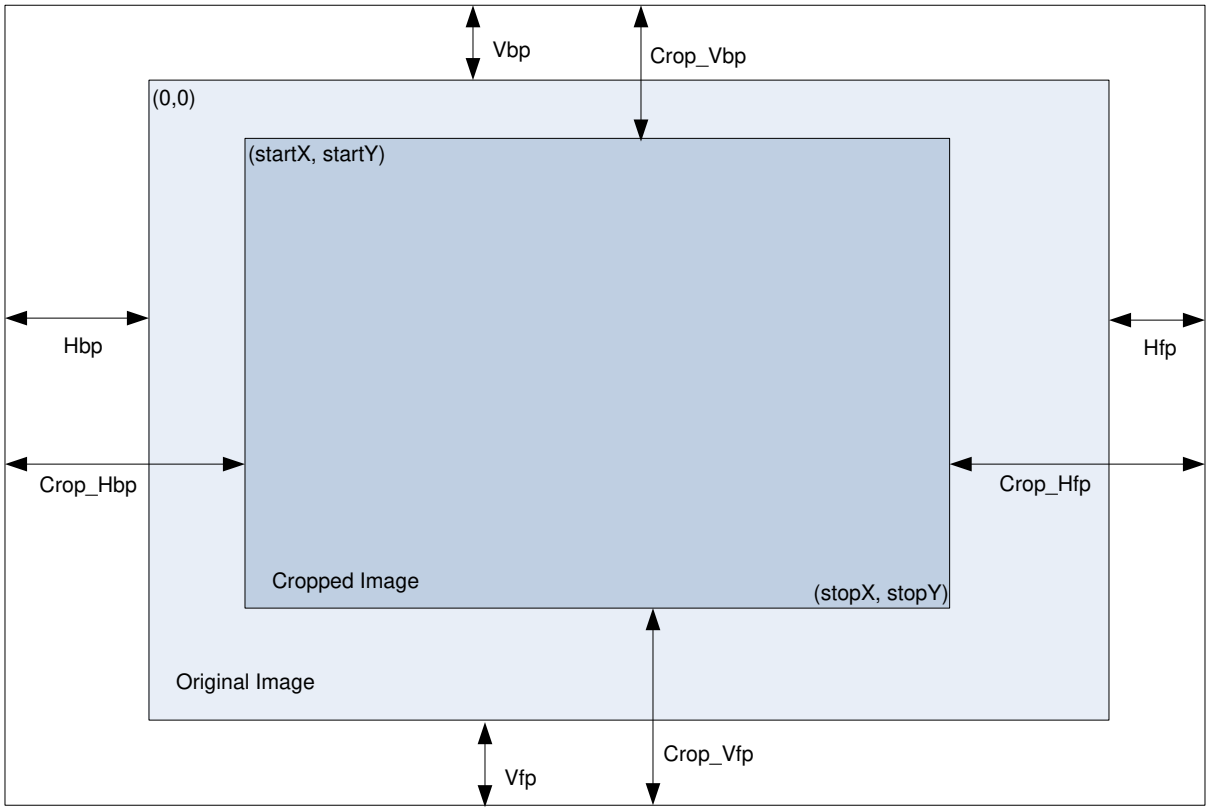

Figure 1-7. Cropping Example

1.6.1 Cropping Control Registers

Cropping is controlled by the CROP_START_X/Y and CROP_STOP_X/Y registers for each port.

1.6.1.1 CROP_START_X0_CROP_START_X0_P1 Register (Address = 36h) [reset = 0h]

CROP_START_X0_CROP_START_X0_P1 is described in Table 1-2.

Table 1-2. CROP_START_X0_CROP_START_X0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_START_X_7:0__CROP_START_X_P1_7:0	R/W	0h	Crop Start X0 Register. In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Image Cropping Start X position (bits 7:0). The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position will not be forwarded, replaced with blank (DE is de-asserted). Pixel positions range from 0 to N-1, where N is the line length in pixels.

1.6.1.2 CROP_START_X1_CROP_START_X1_P1 Register (Address = 37h) [reset = 0h]

CROP_START_X1_CROP_START_X1_P1 is described in Table 1-3.

Table 1-3. CROP_START_X1_CROP_START_X1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CROP_ENABLE_CROP_ENABLE_P1	R/W	0h	Crop Start X1 Register. In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Enable Video Cropping: Setting this bit to a 1 enables cropping of video for the selected port. Cropping is controlled by setting the X,Y start and stop positions using the CROP_START_X/Y and CROP_STOP_X/Y registers.
6-5	RESERVED	R	0h	Reserved
4-0	CROP_START_X_12:8__CROP_START_X_P1_12:8	R/W	0h	Image Cropping Start X position (bits 12:8). In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Start X position indicates the horizontal starting position for the portion of the video line to forward. Pixels prior to the start X position are not forwarded, replaced with blank (DE will be deasserted). Pixel positions range from 0 to N-1 where N is the line length in pixels.

1.6.1.3 CROP_STOP_X0_CROP_STOP_X0_P1 Register (Address = 38h) [reset = 0h]

CROP_STOP_X0_CROP_STOP_X0_P1 is described in Table 1-4.

Table 1-4. CROP_STOP_X0_CROP_STOP_X0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_STOP_X_7:0__CROP_STOP_X_P1_7:0	R/W	0h	Image Cropping Stop X position (bits 7:0). In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position are not forwarded, replaced with blank (DE is deasserted). Pixel positions range from 0 to N-1 where N, is the line length in pixels.

1.6.1.4 CROP_STOP_X1_CROP_STOP_X1_P1 Register (Address = 39h) [reset = 0h]

CROP_STOP_X1_CROP_STOP_X1_P1 is described in Table 1-5.

Table 1-5. CROP_STOP_X1_CROP_STOP_X1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved.
4-0	CROP_STOP_X_12:8__CROP_STOP_X_P1_12:8	R/W	0h	Image Cropping Stop X position (bits 12:8). In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Stop X position indicates the position of the last pixel to be forwarded when cropping is enabled. Pixels following the Stop X position are not forwarded, replaced with blank (DE is deasserted). Pixel positions range from 0 to N-1, where N is the line length in pixels.

1.6.1.5 CROP_START_Y0_CROP_START_Y0_P1 Register (Address = 3Ah) [reset = 0h]

CROP_START_Y0_CROP_START_Y0_P1 is described in Table 1-6.

Table 1-6. CROP_START_Y0_CROP_START_Y0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_START_Y_7:0__CROP_START_Y_P1_7:0	R/W	0h	Crop Start Y0 Register. In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Image Cropping Start Y position (bits 7:0). The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Pixels prior to the Start Y position is not forwarded, replaced with blank lines (DE is deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame. In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port.

1.6.1.6 CROP_START_Y1_CROP_START_Y1_P1 Register (Address = 3Bh) [reset = 0h]

CROP_START_Y1_CROP_START_Y1_P1 is described in Table 1-7.

Table 1-7. CROP_START_Y1_CROP_START_Y1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved.
4-0	CROP_START_Y_12:8__CROP_START_Y_P1_12:8	R/W	0h	Image Cropping Start Y position (bits 12:8). In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Start Y position indicates the first video line to be forwarded when cropping is enabled. Video lines following the Start Y position are not forwarded, replaced with blank lines (DE is deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

1.6.1.7 CROP_STOP_Y0_CROP_STOP_Y0_P1 Register (Address = 3Ch) [reset = 0h]

CROP_STOP_Y0_CROP_STOP_Y0_P1 is described in Table 1-8.

Table 1-8. CROP_STOP_Y0_CROP_STOP_Y0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CROP_STOP_Y_7:0__CROP_STOP_Y_P1_7:0	R/W	0h	Crop Stop Y0 Register. In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. Image Cropping Stop Y position (bits 7:0). The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position are not forwarded, replaced with blank lines (DE is deasserted). Line positions range from 0 to N-1, where N is the number of lines in the frame.

1.6.1.8 CROP_STOP_Y1_CROP_STOP_Y1_P1 Register (Address = 3Dh) [reset = 0h]

CROP_STOP_Y1_CROP_STOP_Y1_P1 is described in Table 1-9.

Table 1-9. CROP_STOP_Y1_CROP_STOP_Y1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved.
4-0	CROP_STOP_Y_12:8__CROP_STOP_Y_P1_12:8	R/W	0h	Image Cropping Stop Y position (bits 12:8). In Splitter or Independent 2:2 modes, this controls the selected FPD-Link III port. The Image Cropping Stop Y position indicates the last video line to be forwarded when cropping is enabled. Video lines following the Stop Y position are not forwarded, replaced with blank lines (DE is deasserted). Line positions range from 0 to N-1 where N is the number of lines in the frame.

In addition to the cropping options, the Horizontal Sync width and Horizontal Back Porch period may be modified. Front Porch value may be determined from total line length - (Active line length + Horizontal Back Porch + Horizontal Sync). Typically, these values are automatically generated based on the input video (half of the values in the dual image), but these can be overridden by setting the IMG_HSYNC_CTL registers. The Horizontal Sync period and the Horizontal Back Porch can be individually overridden by setting the HSYNC_OV_EN or HBACK_OV_EN controls, as well as the IMG_HSYNC and IMG_HBACK parameters. When overriding the IMG_HBACK parameter, the resultant back porch is half of the programmed value, rounded up, plus one extra pixel. When overriding the IMG_HSYNC parameter, the resultant sync width is half the programmed value, rounded up. If the HSYNC and HBACK values are reduced, then the difference is added to the horizontal front porch. If the HSYNC and HBACK values are increased, then the difference is subtracted from the horizontal front porch.

1.7 Splitter Mode Pixel Clocks

By default, asymmetric splitting generates each resultant image at half the frequency of the superframe image. Options exist to use external reference clocks or M/N divided versions of the DPHY Lane clock for each resultant image. To avoid jitter clocks, TI recommends programming M to a value of 1. To prevent short pulse-widths to the Dual-Image buffer memories, the splitter mode dividers must have N greater than M. Additionally, the 1 divided by the ratio M/N must be an integer. The default settings for M/N provide a half clock frequency normally required for splitting symmetric video. The use of the half ratio results in an image with significant horizontal blanking; increasing the N value reduces the horizontal blanking. Note that this does not affect the vertical blanking.

1.7.1 SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1 Register (Address = 3Eh) [reset = 81h]

SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1 is described in Table 1-10.

Table 1-10. SPLIT_CLK_CTL0_SPLIT_CLK_CTL0_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPLIT_CLK_DIV_EN_SPLIT_CLK_DIV_EN_P1	R/W	1h	Splitter Mode Clock Control Register 0. This controls the selected FPD-Link III port. Splitter mode clock divider enable. This register enables the splitter mode clock divider. In splitter mode, if this register is set to 0, the pixel clock for splitter operation is disabled. The divider should be disabled prior to changing the Splitter Divider settings, SPLIT_CLK_SEL, SPLIT_CLK_DIV_M, and SPLIT_CLK_DIV_N. In addition, changes to divider settings must only be done when the DSI input is disabled to ensure proper mode transition. These values are ignored if Splitter mode is disabled. This controls the selected FPD-Link III port.
6-5	SPLIT_CLK_SEL	R/W	0h	Splitter mode clock select. This register selects the clock source for the FPD-Link III transmit side of the splitter operation for the selected port. 00 : Input pixel clock divided by 2 (default). 01 : M/N divider from the DPHY input clock. 10 : M/N divider from the external clock on the REFCLK0 pin. 11 : M/N divider from the external clock on the REFCLK1 pin.
4-0	SPLIT_CLK_DIV_M_SPLIT_CLK_DIV_M_P1	R/W	1h	Splitter mode clock divider M value. This register controls the M setting for the M/N divider used to generate the splitter mode pixel clock from the selected input clock. The default settings for M/N provide a half clock frequency normally required for splitting symmetric video. These values are ignored if Splitter mode is disabled. This controls the selected FPD-Link III port.

1.7.2 SPLIT_CLK_CTL1_SPLIT_CLK_CTL1_P1 Register (Address = 3Fh) [reset = 2h]

SPLIT_CLK_CTL1_SPLIT_CLK_CTL1_P1 is described in Table 1-11.

Table 1-11. SPLIT_CLK_CTL1_SPLIT_CLK_CTL1_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPLIT_CLK_DIV_N_SPLIT_CLK_DV_N_P1	R/W	2h	Splitter Mode Clock Control Register 1. This controls the selected FPD-Link III port. Splitter mode clock divider N value. This register controls the N setting for the M/N divider used to generate the splitter mode pixel clock from the selected input clock. The default settings for M/N provide a half clock frequency normally required for splitting symmetric video. These values are ignored if Splitter mode is disabled. This controls the selected FPD-Link III port.

1.8 Programming Example

The example code configures the devices for splitting a 2560x720 (2x1280x720, 60 fps, 100-MHz PCLK) superframe with Left/Right 3D from a 4-Lane DSI source to two remote displays with standard 720 and 480p resolutions. The 720p display is assumed to be connected to FPD-Link Port 0, while the 480p display is assumed to be connected to FPD-Link Port 1. The example code also configures the device for cropping the Port1 video after the splitting and before forwarding the data to the 720p display.

```
WriteI2C (0x01,0x08)    //Disable DSI
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 0
WriteI2C (0x4F,0x0C)    //Set DSI_CONTINUOUS_CLOCK, 4 lanes, DSI Port 0
WriteI2C (0x5B,0x07)    //Force Splitter mode
WriteI2C (0x56,0x80)    //Enable Left/Right 3D processing to allow superframe splitting
WriteI2C (0x1E,0x02)    //Select FPD-Link III Port 1
WriteI2C (0x4F,0x0C)    //Set DSI_CONTINUOUS_CLOCK, 4 lanes, DSI Port 1
WriteI2C (0x5B,0x07)    //Force Splitter mode
WriteI2C (0x56,0x80)    //Enable Left/Right 3D processing to allow superframe splitting
WriteI2C (0x32,0x00)    //Set the line size to 1280(LSB)
WriteI2C (0x33,0x05)    //Set the line size to 1280 (MSB)

//Crop Port0 720p image
WriteI2C (0x1E,0x01)    //Select FPD-Link III Port 1
WriteI2C (0x36,0x00)    //Set crop start X position to 0 (LSB)
WriteI2C (0x37,0x80)    //Set crop start X position to 0 (MSB) and enable cropping
WriteI2C (0x38,0xFF)    //Set crop stop X position to 1279 (LSB)
WriteI2C (0x39,0x04)    //Set crop stop X position to 1279 (MSB)
WriteI2C (0x3A,0x00)    //Set crop start Y position to 0 (LSB)
WriteI2C (0x3B,0x00)    //Set crop start Y position to 0 (MSB)
WriteI2C (0x3C,0xCF)    //Set crop stop Y position to 719 (LSB)
WriteI2C (0x3D,0x02)    //Set crop stop Y position to 719 (MSB)
//Crop Port1 480p image
WriteI2C (0x1E,0x02)    //Select FPD-Link III Port 1
WriteI2C (0x36,0x00)    //Set crop start X position to 0 (LSB)
WriteI2C (0x37,0x80)    //Set crop start X position to 0 (MSB) and enable cropping
WriteI2C (0x38,0x7F)    //Set crop stop X position to 639 (LSB)
WriteI2C (0x39,0x02)    //Set crop stop X position to 639 (MSB)
WriteI2C (0x3A,0x00)    //Set crop start Y position to 0 (LSB)
WriteI2C (0x3B,0x00)    //Set crop start Y position to 0 (MSB)
WriteI2C (0x3C,0xDF)    //Set crop stop Y position to 479 (LSB)
WriteI2C (0x3D,0x01)    //Set crop stop Y position to 479 (MSB)

//Program TSKIP_CNT DSI parameter on DSI Port0
WriteI2C (0x40,0x04)    //Select DSI Port 0 digital registers
WriteI2C (0x41,0x05)    //Select DPHY_SKIP_TIMING register
WriteI2C (0x42,0x1E)    //Write TSKIP_CNT value for 300 MHz DSI clock frequency


WriteI2C (0x01,0x00)    //Enable DSI
```

1.9 Summary

The DS90UB941AS-Q1 provides video processing functions system designers can use to create IVI systems with multiple displays using cost-effective application processors. Engineers can split superframes symmetrically or asymmetrically by following the suggestions and programming examples given in this report.

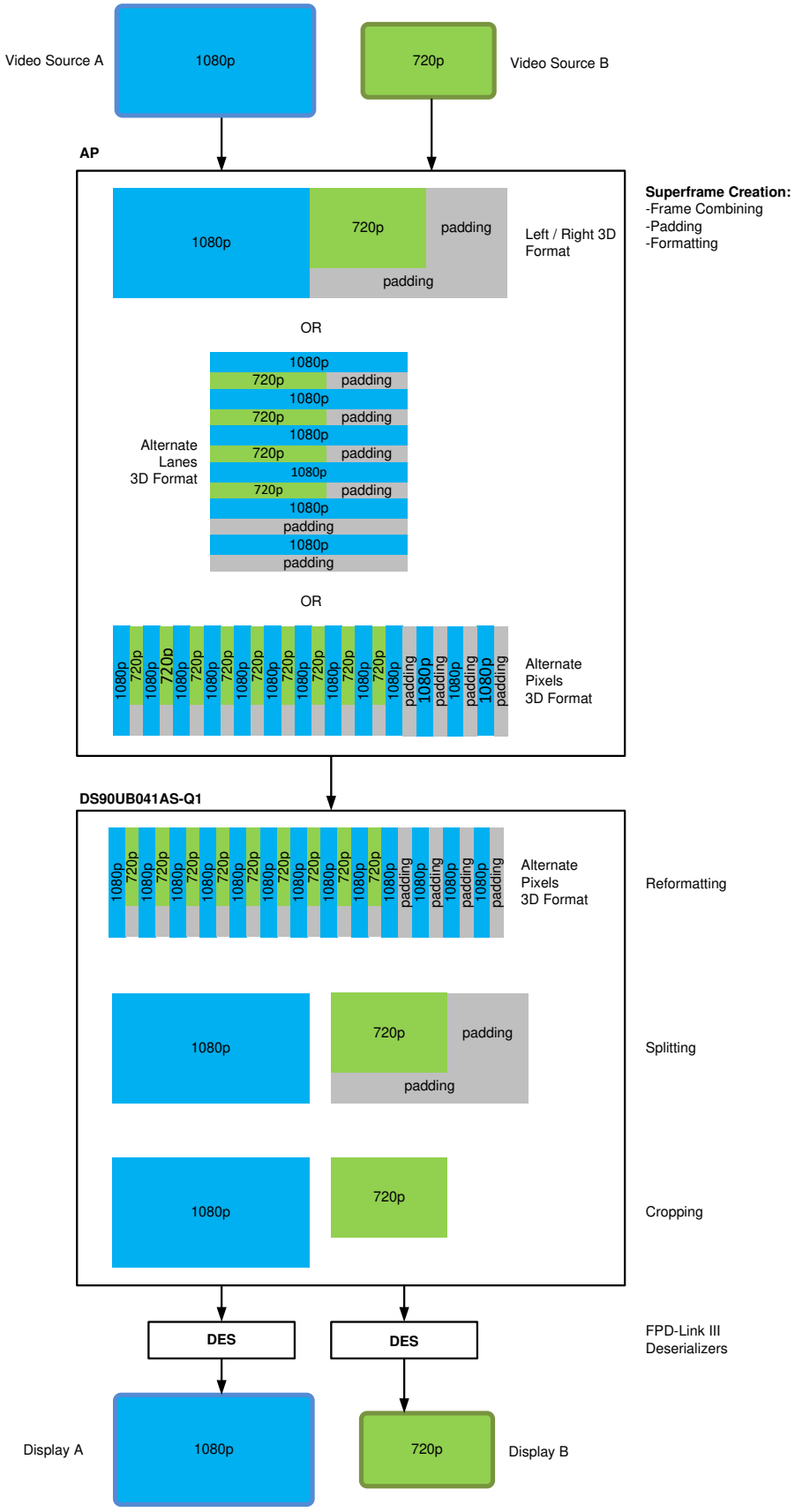

Figure 1-8. Superframe Creation and Splitting Flow Diagram

1.10 References

- *DS90UB941AS-Q1 DSI to FPD-Link III Bridge Serializer* (SNLS640)
- *High-Definition Multimedia Interface Specification Version 1.4a* (March 4, 2010), HDMI Licensing, LLC.

Handling Interrupts With the DS90UH941AS-Q1

2.1 Interrupt Control and Status (INTB and REM_INTB Pin)

The HDCP Transmitter can generate an interrupt signal to the attached controller through the INTB pin. This method allows the controller to process some portion of the authentication flow, or to indicate errors in the link status or authentication. The INTB pin is an open-drain, active-low signal that may be shared with other interrupt sources. The HDCP Interrupt Control Register (HDCP_ICR, address 0xC6) enables the various interrupt conditions, while the HDCP Interrupt Status Register (HDCP_ISR, address 0xC7) is used to monitor the interrupt conditions. Bit 0 of the HDCP_ICR is the global interrupt enable that must be set along with at least one other interrupt enable to generate an interrupt on the active low INTB pin.

Upon an interrupt detection, the controller must read the HDCP_ISR register to determine the interrupt condition. Bit 0 of the HDCP_ISR indicates whether or not an interrupt occurred, and the individual status bits indicate which conditions were triggered. The read of the HDCP_ISR also clears the interrupt, which releases the INTB pin. If desired, the controller may then read the HDCP_STS register to determine the current device status. For details on the available interrupt conditions, see the HDCP_ICR and HDCP_ISR register definitions in the data sheet.

The Receiver interrupt—which is bit 5 of HDCP_ICR and HDCP_ISR registers—is a special case. This interrupt is used to propagate an external interrupt from the HDCP Receiver INTB_IN pin to the HDCP Transmitter interrupt pin (INTB). The interrupt is active low and is handled similarly to other interrupt conditions. When the controller detects a falling edge of the interrupt signal, the HDCP Transmitter latches on the interrupt condition, sets the IS_RX_INT bit in the HDCP_ISR register, and asserts the INTB pin low. To clear the interrupt signal, the controller must read the HDCP_ISR to release the INTB and clear the HDCP_ISR. The controller may then check the HDCP_STS:RX_INT bit to determine the current status of the HDCP Receiver's INTB_IN pin. The INTB pin remains deasserted until the next falling edge of the INTB_IN signal. Figure 2-1 shows a typical diagram for the Receiver interrupt propagation.

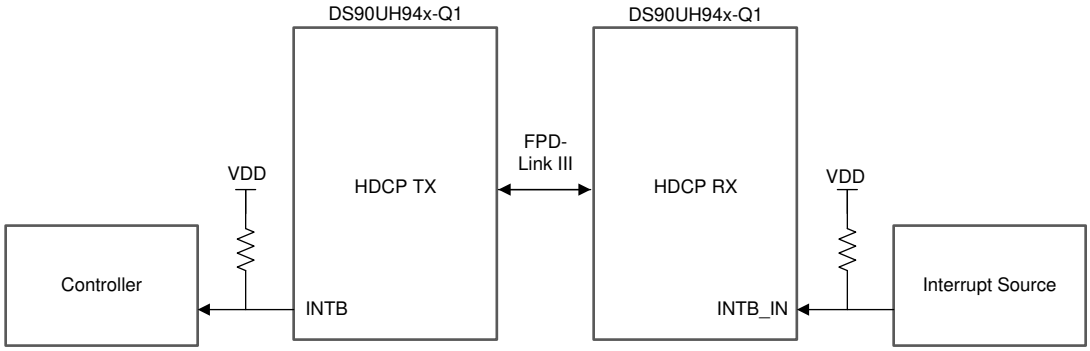

Figure 2-1. Receiver Interrupt Propagation Block Diagram

The sequence for handling the Receiver Interrupt is as follows:

1. INTB_IN is pulled low by a downstream device.
2. HDCP Transmitter pulls INTB low.
3. Controller detects the INTB low and reads the HDCP_ISR register to determine the interrupt source. This clears the interrupt at HDCP Transmitter, which releases the INTB.
4. The controller typically accesses the remote interrupt source to process the downstream interrupt, which clears the interrupt condition driving INTB_IN.
5. System is ready to capture another interrupt condition.

2.2 Handling Interrupts in Splitter Mode Using Remote Interrupt Pin (REM_INTB)

The DS90UH941AS-Q1 includes a dedicated remote interrupt pin (REM_INTB). This pin provides a pass-through of the INTB signal from an attached FPD-Link III deserializer (for example, the DS90UH948-Q1). During a valid link connection, the value of the deserializer INTB_IN is reflected to the DS90UH041-Q1 REM_INTB pin. In Dual FPD3 mode, the REM_INTB pin indicates the INTB_IN from the attached dual-capable deserializer.

If multiple deserializers are connected, the REM_INTB typically indicates a combined interrupt from INTB_IN pins of multiple deserializers. The combined interrupt is asserted if either connection reports a remote interrupt. If desired, the Remote Interrupt Control (REM_INTB_CTRL, address 0x30) allows independent remote interrupts from both deserializers. Figure 2-2 shows a typical diagram for the receiver interrupt propagation for independent remote interruption.

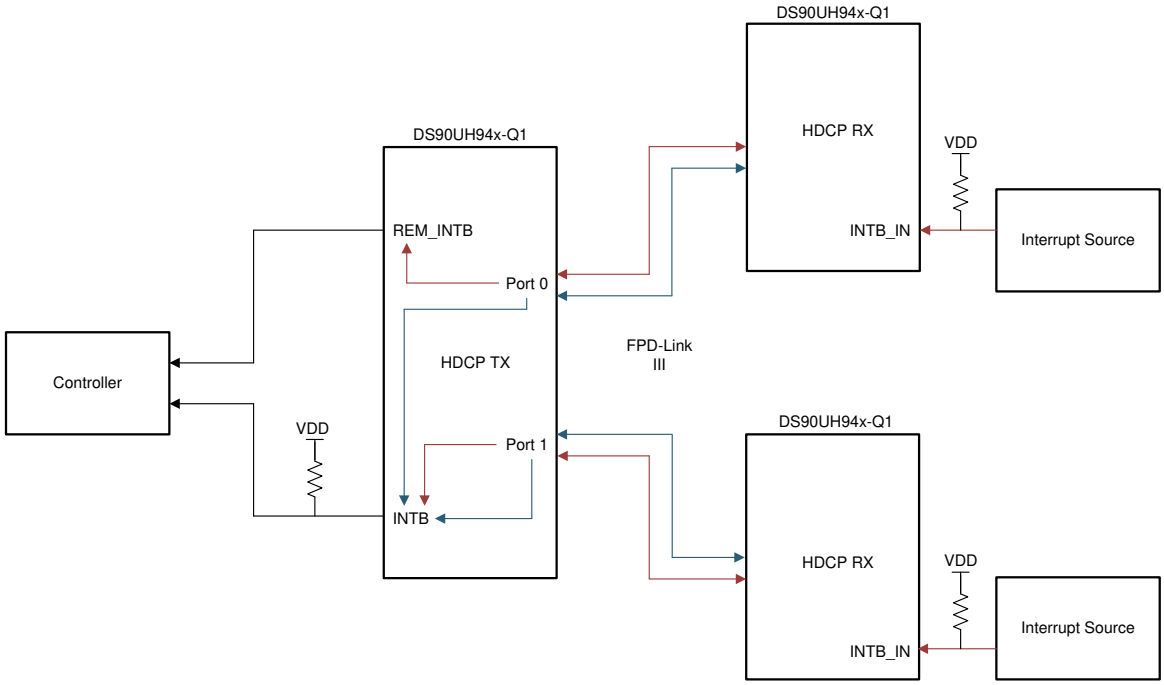

Figure 2-2. Interrupt Propagation in Splitter Mode Block Diagram

Selection 0001 of REM_INTB_MODE field brings a port 0 remote interrupt to the REM_INTB pin, and a port 1 remote interrupt to the INTB pin. For the INTB pin, the remote interrupt is combined with the HDCP interrupt register sources, but HDCP interrupts are only active if they are enabled through the HDCP_ICR register. For the REM_INTB pin, the controller must check the status registers of the interrupt sources.

The sequence for handling the receiver interrupt is as follows:

1. INTB_IN is pulled low by a downstream device.
2. HDCP Transmitter pulls REM_INTB low if the interrupt comes from port 0, or pulls INTB low if the interrupt comes from port 1.
3. If the controller detects the INTB low, the controller reads the HDCP_ISR register to determine the interrupt source (port 0 or 1). This clears the interrupt at the HDCP Transmitter and releases the INTB, provided that the interrupt came from one of the HDCP Receiver devices.
4. If INTB is still not cleared, then the interrupt came from a remote interrupt source, and the controller must access the status register of the remote interrupt source.
5. The controller accesses the remote interrupt source to process the downstream interrupt, clearing the interrupt condition driving INTB_IN from port 1.
6. If the controller detects REM_INTB low, the controller must check the status registers of the interrupt sources, clearing the interrupt condition driving INTB_IN from port 0. The REM_INTB copies the signal from the INTB_IN to port 0, so REM_INTB also clears.

2.3 REM_INTB_CTRL Register (Address = 30h) [reset = 0h]

REM_INTB_CTRL is described in Table 2-1.

Table 2-1. REM_INTB_CTRL Register Field Description

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	REM_INTB_MODE	R/W	0h	Allows choosing different pins to output the remote interrupt. if multiple links are available (Not in Dual FPD-Link III operation), the REM_INTB is typically a combined interrupt from both ports. See selection 0001 below for the exception that allows independent remote interrupts from both ports. Determines the pin that Remote Interrupt outputs on: 0000: NOT ENABLED 0001: REM_INTB indicates port 0 remote interrupt, INTB indicates port1 remote interrupt 0001x,01xx Reserved 1000: GPIO0 1001: GPIO1 1010: GPIO2 1011: GPIO3 1100: D_GPIO1 1101: D_GPIO2 1110: D_GPIO3 1111: D_GPIO4

High-Speed GPIO Operation in Splitter Mode

3.1 Introduction

The DS90Ux94x-Q1 family of devices incorporates both forward and reverse communication channels using one or two links. Forward channel data typically carries video information, but can also include additional bandwidth for other communications. The back channel signaling provides slower speed communication in the reverse direction. GPIO signals may be sent in both forward and reverse directions over either one or both links.

3.2 High-Speed Control Configuration

The High-Speed control channel mode can be configured by setting the following register control in the deserializer using the I2C register interface. HSCC Modes must only be enabled after the deserializer detects a valid receiver Lock condition (through the LOCK pin or LOCK status in register 0x0C). This ensures that the serializer has properly determined the deserializer capabilities prior to enabling the high-speed modes. In addition, if Receiver Lock is lost, HSCC mode must be disabled until a valid lock condition is restored

HSCC mode is split into two registers. The first two bits are under HSCC_MODE_2:1 field in Table 3-2. Bit 0 is under HSCC_MODE_0 field in Table 3-1 .

3.2.1 DES_CAP1 Registers (Address = 20h)

DES_CAP1 is described inTable 3-1

Table 3-1. DES_CAP1 Register Field Description

Bit	Field	Type	Reset	Description
7	FREEZE_DES_CAP FREEZE_DES_CAP_1	R	0h	If PORT1_SEL is set, this register indicates Port1 Capabilities Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Bidirectional Control Channel. The Capabilities are frozen at the values written in registers 0x20 and 0x21.
6	HSCC_MODE_0 _HSCC_MODE_P1_0	R/W	0h	High-Speed Control Channel bit 0 Lowest bit of the 3-bit HSCC indication. The other 2 bits are contained in Deserializer Capabilities 2. This field automatically configured by Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	DUAL_LINK_CAP DUAL_LINK_CAP_1	R/W	0h	Dual link Capabilities Indicates if the Deserializer is capable of dual link operation. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel..

Table 3-1. DES_CAP1 Register Field Description (continued)

Bit	Field	Type	Reset	Description
2	DUAL_CHANNEL_CAP DUAL_CHANNEL_CAP_1	R/W	0h	Dual Channel 0/1 Indication In a dual-link capable device, indicates if this is primary or secondary channel. 0: Primary channel (channel 0) 1: Secondary channel (channel 1) This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
1	VID_24B_HD_AUD VID_24B_HD_AUD_P1	R/W	0h	Deserializer supports 24-bit video concurrently with HD audio This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
0	DES_CAP_FC_GPIO DES_CAP_FC_GPIO_P1	R/W	0h	Deserializer supports GPIO in the Forward Channel Frame This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.

3.2.2 DES_CAP2 Registers (Address = 21h)

DES_CAP2 is described inTable 3-2

Table 3-2. DES_CAP2 Register Field Description

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	FC_BCC_CRC6	R/W	0h	Enabled enhanced CRC and start sequence
2	RGB_CHKSUM_ERR	R	0h	RGB Checksum Error Detected: If RGB Checksum is enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected.
1-0	HSCC_MODE_2:1 HSCC_MODE_P1_2:1	0,RW	0h	High-Speed Control Channel bit 0 Upper bits of the 3-bit HSCC indication. The lowest bit is contained in Deserializer Capabilities 1. 000: Normal Frame, GPIO Mode 001: High-Speed GPIO mode, 1 GPIO 010: High-Speed GPIO mode, 2 GPIOs 011: High-Speed GPIO mode,4 GPIOs 100: Reserved 101: Reserved 110: High-Speed, Forward Channel SPI Mode 111: High-Speed, Reverse Channel SPI Mode In Single Link devices, only Normal back channel frame modes are supported

3.3 Back Channel Frequency Configuration

The deserializer includes oscillator divider control to support additional back-channel frequencies other than the default 5-Mbps speed. The engineer can configure the OSC_DIVIDER controls in register 0x32, as well as the BC_FREQ_SELECT control in register 0x23[2], to control the oscillator divider. The supported frequencies are 100 MHz/N or 50 MHz/N. Table 3-3 lists the back-channel frequency settings.

The non-default settings of the OSC_DIVIDER are for evaluation purposes only, as they may cause other functions in the device to operate at unexpected frequencies. Note that if BC_HIGH_SPEED is set to a 1, only even values of N are supported.

Table 3-3. Back Channel Frequency Settings

OSC_Divider	DIV Ratio N	BC_FREQ_SELECT (Mbps) 0	BC_FREQ_SELECT (Mbps) 1	BC_HIGH_SPEED (Mbps) 1
0x0	1	50	100	N/A
0x1	2	25	50	100
0x2	3	16.67	33.33	N/A
0x3	4	12.5	25	50
0x4	5	10	20	N/A
0x5	6	8.33	16.67	33
0x6	7	7.14	14.28	N/A
0x7	8	6.25	12.5	25
0x8	9	5.55	11.11	N/A
0x9	10	5 (default)	10	20
0xA	11	4.55	9.1	N/A
0xB	12	4.17	8.33	16.67
0xC	13	3.85	7.69	N/A
0xD	14	3.57	7.14	14.28
0xE	15	3.33	6.67	N/A
0xF	16	3.125	6.25	12.5

3.4 Splitter Mode GPIO

Each GpIO or DGPIO may be configured for either forward or reverse direction. For the GPIO to operate correctly, both the serializer and deserializer must be configured for the proper operation. Configuration of the GPIO and DGPIO is described in the register documentation for each device. See descriptions of the GPIO Configuration registers. Note that in back channel, high-speed GPIO modes, only certain DGPIO pins are available for options that only send one or two GPIO signals in the back channel.

In splitter mode, GPIO signals go over DS90Ux941AS-Q1 FPD3 TX Port 0 and D_GPIO signals over DS90Ux941AS-Q1 FPD3 TX Port 1. Figure 3-1 shows a possible setup.

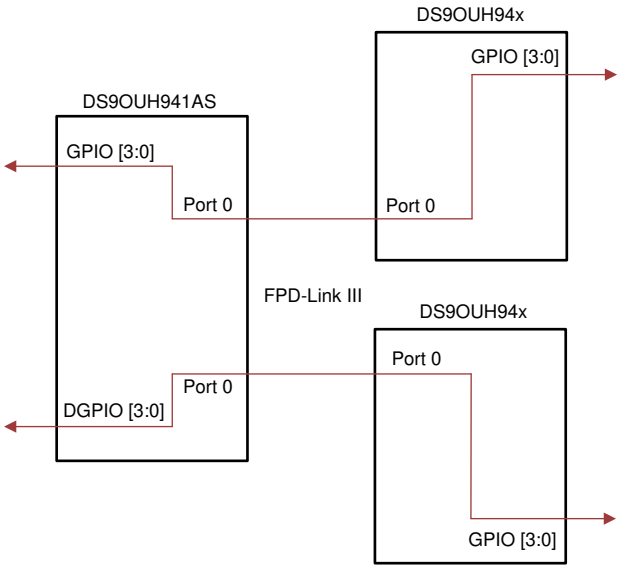

Figure 3-1. Splitter Mode GPIO Block Diagram

3.5 GPIO_0_Config Register (Address = Dh) [reset = 20h]

GPIO_0_Config is described in Table 3-4.

Table 3-4. GPIO_0_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REV_ID	R	2h	GPIO and D_GPIO Configuration. If PORT1_SEL is set, this register controls the D_GPIO0 pin Revision ID 0010: DS90Ux941AS-Q1
3	GPIO_OUTPUT_VALUE_D_GPIO0_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote-Default mode if the link is lost.
2-0	GPIO0_MODE_D_GPIO0 MODE	R/W	0h	GPIO 0 Mode. Determines operating mode for the GPIO pin: x00: Functional input mode, GPIO0 input x10: Tri-state 001: GPIO mode, output 011: GPIO mode, input 101: Remote-Hold - output remote data, maintain data on link-loss 111: Remote-Default - output remote data Drive default data (OUTPUT VALUE) on link-loss

3.6 GPIO_1_and_GPIO_2_Config Register (Address = Eh) [reset = 0h]

GPIO_1_and_GPIO_2_Config is described in Table 3-5.

Table 3-5. GPIO_1_and_GPIO_2_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO2_OUTPUT_VALUE_D_GPIO2_OUTPUT_VALUE	R/W	0h	GPIO1/GPIO2 and D_GPIO1/D_GPIO2 Configuration. If PORT1_SEL is set ,this register controls the D_GPIO1 and D_GPIO2 pins. Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote_Default mode if the link is lost.
6-4	GPIO2_MODE_D_GPIO2_MODE	R/W	0h	GPIO 2 Mode. Determines operating mode for the GPIO pin: x00: Functional input mode, I2S_DC input x10: Tri-State 001: GPIO mode, output 011: GPIO mode, input 101: Remote-Hold - output remote data, maintain data on link-loss 111: Remote-Default - output remote data Drive default data (OUTPUT VALUE) on link-loss
3	GPIO1_OUTPUT_VALUE_D_GPIO1_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote-Default mode if the link is lost.
2-0	GPIO1_MODE_D_GPIO1_MODE	R/W	0h	GPIO 1 Mode. Determines operating mode for the GPIO pin: x00: Functional input mode, I2S_DC input x10: Tri-State 001: GPIO mode, output 011: GPIO mode, input 101: Remote-Hold - output remote data, maintain data on link-loss 111: Remote-Default - output remote data Drive default data (OUTPUT VALUE) on link-loss

3.7 GPIO_3_Config Register (Address = Fh) [reset = 0h]

GPIO_3_Config is described in Table 3-6.

Table 3-6. GPIO_1_and_GPIO_2_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	GPIO3 and D_GPIO3 Configuration. If PORT1_SEL is set ,this register controls the D_GPIO3. Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote_Default mode if the link is lost.
3	GPIO3_OUTPUT_VALUE_D_GPIO3_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. This value is also output to the GPIO pin in Remote-Default mode if the link is lost.
2-0	GPIO1_MODE_D_GPIO3_MODE	R/W	0h	GPIO 3 Mode. Determines operating mode for the GPIO pin: x00: Functional input mode, I2S_DC input x10: Tri-State 001: GPIO mode, output 011: GPIO mode, input 101: Remote-Hold - output remote data, maintain data on link-loss 111: Remote-Default - output remote data Drive default data (OUTPUT VALUE) on link-loss

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