Application Report
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Optimal Implementation of 25G/28G Retimers versus Redrivers in Common Applications

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ABSTRACT

This document provides application-based criteria to assist system developers in selecting between 25G/28G retimers and redrivers. Functional background and description of relevant performance parameters and features for these devices are included to facilitate part number comparison and selection. Channel insertion loss, networking standard compliance needs and link training support are all reviewed in the context of component selection of retimers versus redrivers to achieve signal conditioning and link reach extension.

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Trademarks

1 Overview of TI 25G/28G Retimers and Redrivers

Figure 1 and Figure 2 illustrate the functional block diagrams for TI's 25G/28G retimers and redrivers. As evident from the block diagrams, the retimer and redriver have a few key functional differences.

- The retimer implements clock and data recovery (CDR) and sampler functional blocks, thus enabling it to output a retimed version of the input signal with lower jitter. The redriver on the other hand does not incorporate the retiming-CDR related functional blocks.
- The redriver implements a two-stage continuous time linear equalizer (CTLE) as its only form of receive equalization.
- In addition to CTLE, the retimer also implements a decision feedback equalizer (DFE). Thus the retimer is equipped with more enhanced post-cursor equalization function.
- The retimer incorporates additional diagnostic functions not available on the redriver, including PRBS pattern generation and checking and eye monitor functions.

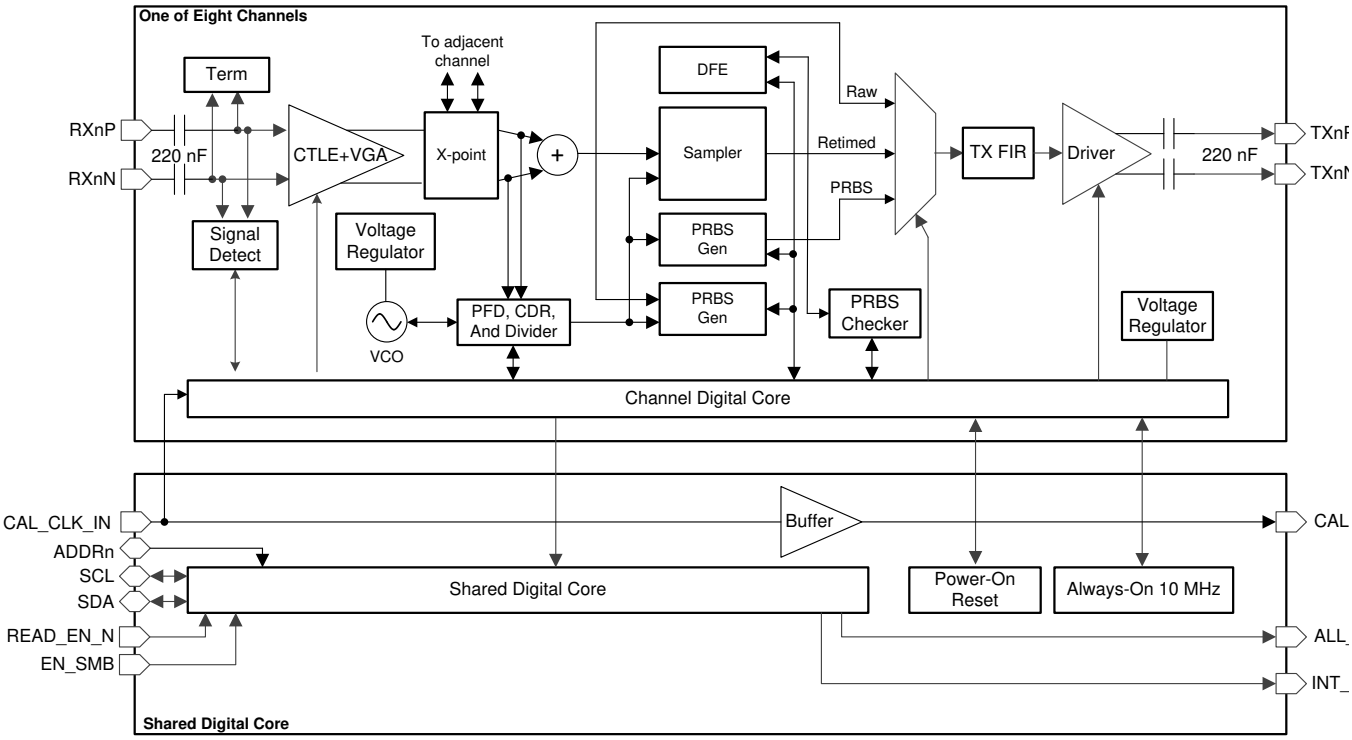

Figure 1. DS280DF810 Retimer Functional Block Diagram

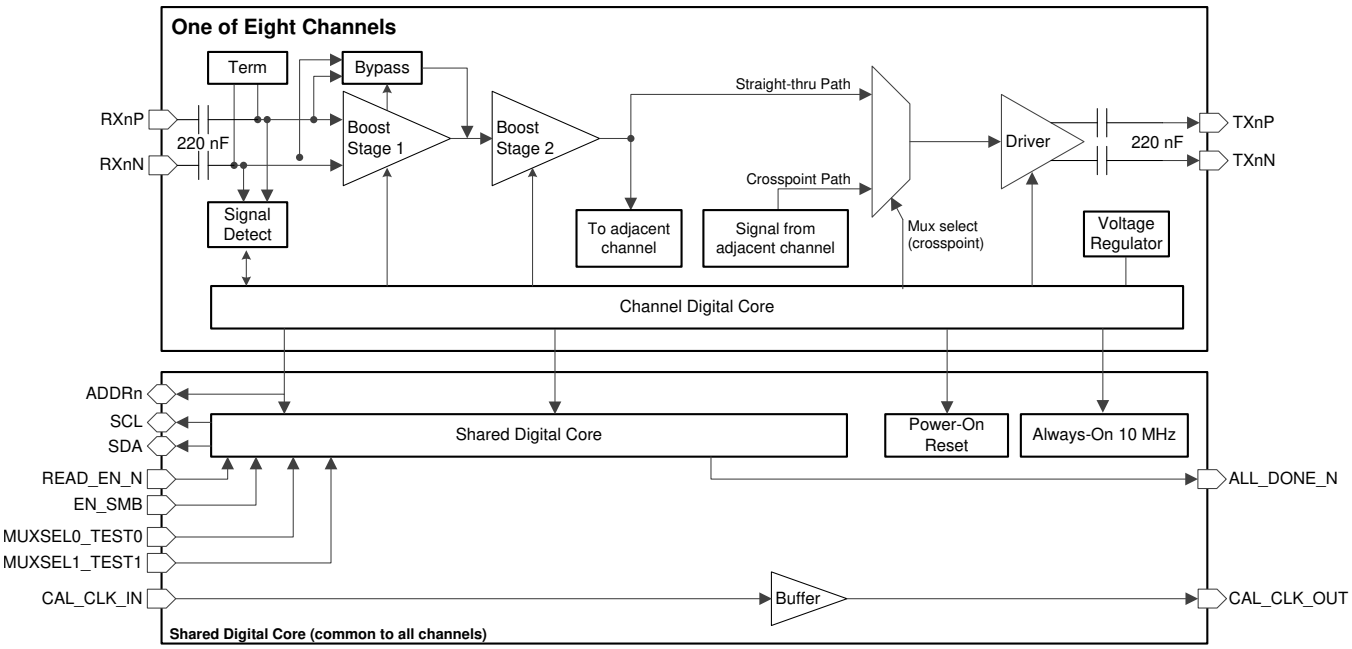

Figure 2. DS280MB810 Redriver Functional Block Diagram

2 When to use a Retimer Versus Redriver

Table 1 lists a high-level summary of chip-to-chip interface types based on their transmission channel's insertion loss at around the Nyquist frequency for 25Gbps data rate. The amount of channel loss will dictate the level of signal conditioning required for an error free chip-to-chip link. Some portion of system interconnects will have channel loss that is within the equalization compensation capability of the chips being linked together. Such links do not require signal conditioning. Links requiring a moderate amount of compensation (up to 20dB) may use a redriver instead of a retimer, in that way realizing some relative savings in power consumption and cost. Links involving transmission across a channel with very high loss require the use of a retimer.

Table 1. Retimer Versus Redriver Selection Based On Chip-to-Chip Channel Insertion Loss

25Gbps CHIP-TO-CHIP LINK CASE	RECOMMENDED SIGNAL CONDITIONING (SigCon) LEVEL
Channel loss within the chip's compensation capability	No SigCon required
Channel loss exceeding chip compensation by up to 20dB	TI 25G/28G redriver
20dB < channel loss < 35dB	TI 25G/28G retimer

3 Retimers for Common Network Interfaces

Referring back to Section 5, TI's 25G/28G retimer part numbers cover slightly different but over-lapping data rates, as each is targeted for specific sets of high-speed interface applications as part of a networking system. Table 2 lists the most common high-speed networking interface standards utilizing TI retimers along with recommendations on the most appropriate TI retimer part numbers.

Table 2. Retimer Part Numbers Mapping To Networking Standards Interfaces

STANDARD NETWORKING HIGH-SPEED INTERFACE CASE	DATA RATE(S) INVOLVED, IN UNIT OF Gbps	SUITABLE RETIMER PART NUMBER(S)
CEI-25G electrical interfaces (SR, MR and LR)	25.78125	DS250DF810, DS280DF810, DS250DF410, DS250DF210, DS250DF230
CEI-28G very short reach (VSR) interfaces	28	DS280DF810
25G Ethernet long reach backplane or copper cable interfaces (i.e. KR4, CR4)	25.78125	DS250DF810, DS280DF810, DS250DF410, DS250DF210, DS250DF230
25G/10G Ethernet front port optical host interfaces	25.78125, 10.3125	DS250DF810, DS280DF810, DS250DF410, DS250DF210, DS250DF230
OTU4 and OTU2 telecom system front port optical host interfaces	27.95, 10.7	DS280DF810
CPRI-7 chip-to-chip or chip-to-module interfaces	24.33 plus legacy CPRI rates	DS250DF230 (preferred solution), DS250DF810, DS280DF810, DS250DF410
16G Fibre Channel switch chip-to-module or chip to chip-to-chip interfaces	14.025, 8.5 and 4.25	DS280DF810

4 Link Training Support With TI Signal Conditioning Devices

Link training is an optional Physical Coding Sublayer (PCS) function specified by the IEEE 802.3 Ethernet specification. It is also used by other standards such as PCIe and Fibre Channel. Link training is a state-machine based algorithm that enables two interconnected systems to converge on their respective optimal transmit equalization settings. Typically the switch ASIC (either front-port or backplane) implements the link training function. Signal conditioners such as TI retimers and redrivers are by definition mid-channel devices. In other words, these devices are placed in the middle of the ASIC-to-ASIC link to provide channel reach extension. The level of link training support offered by signal conditioners can be broken down into three categories, as described in Table 3.

Table 3. Standard Link Training Support Levels For Physical Interface Devices

LINK TRAINING CATEGORY	DESCRIPTION	TI 25G/28G SigCon PRODUCTS IN CATEGORY
No link training support	These devices neither implement the link training digital logic nor do they pass through the link training amplitude info	DS250DF810, DS280DF810, DS250DF410, DS250DF210, DS250DF230
Link training pass-through	Highly linear devices such as TI's 25G/28G redrivers will seamlessly pass through the link training amplitude info from one end to the other	DS280BR820., DS280MB810
Full link training support	These devices implement the digital logic required to execute the link training process in accordance with network standards	Not supported by TI retimers or redrivers

- Recommendation: 25G system developers requiring Link Training support may implement TI's 25G/28G redrivers for mid-channel reach extension.

5 Retimer and Redrivers Part Selection

Table 4 provides a summary of TI's portfolio of signal conditioning devices aimed at 25Gbps to 28Gbps system applications. TI's signal conditioning portfolio spans both retimer and redriver product types. TI's devices are suitable for use in systems spanning a wide range of applications requiring chip-to-chip channel reach extension, from Ethernet data center switches to telecommunications routers and CPRI equipment. Table 4 lists multiple features for each part number including channel count, package type and electrical performance parameters. TI's portfolio has the following differentiating features worth highlighting:

- TI's 25G/28G product family includes 2-channel, 4-channel and 8-channel signal conditioning devices, allowing the system developer to chose a device that optimizes their system board area and layout.
- TI's eight channel retimers and redrivers are fully pin-to-pin and footprint compatible. This 8-channel BGA footprint thus provides the ultimate flexibility for system developers, as they can chose to populate with either the retimer or the redriver based on the needs of specific sections of their board.

Table 4. TI 25G/28G Signal Conditioning Products Comparison

Features	DS280BR820	DS280MB810	DS250DF230	DS250DF410	DS280DF810
Type	redriver	redriver	Retimer	Retimer	Retimer
Data rate	up to 28.4Gbps	up to 28.4Gbps	19.6-25.8Gbps 9.8-12.9Gbps 4.9-6.45Gbps	20.2-25.8Gbps 10.1-12.9Gbps 5.05-6.4Gbps	20.2-28.4Gbps 10.1-14.2Gbps 5.05-7.1Gbps
Channel	8	8	2	4	8
Mux	N/A	Quad 2x2	Single 2x2	Dual 2x2	Quad 2x2
Rx Signal Conditioning Features	2-Stage CTLE, Post-CTLE DC Gain	2-Stage CTLE, Post-CTLE DC Gain	Adaptive 4-Stage CTLE, VGA, Post-CTLE DC Gain, Adaptive 5-Tap DFE, CDR	Adaptive 4-Stage CTLE, VGA, Post-CTLE DC Gain, Adaptive 5-Tap DFE, CDR	Adaptive 4-Stage CTLE, VGA, Post-CTLE DC Gain, Adaptive 5-Tap DFE, CDR
Tx Signal Conditioning Features	3-Tap FIR (Optional)	Linear Only	3-Tap FIR	3-Tap FIR	3-Tap FIR
Channel Reach Extension	17dB+	17dB+	35dB	35dB+	35dB+
Vcc	2.5V	2.5V	2.5V	2.5V	2.5V
Power	90mW/ch	90mW/ch	315mW/ch	315mW/ch	315mW/ch
Latency (Typ)	100ps	100ps	<500ps	<500ps	<500ps
Integrated AC Coupling	Receiver Only	Receiver Only	N/A	N/A	Receiver and Transmitter
Seamless FEC Pass-Through	Yes	Yes	Yes	Yes	Yes
Link training support	Seamless Pass-Through	Seamless Pass-Through	Not supported	Not supported	Not supported
Flow through Routing	Yes	Yes	Yes	Yes	Yes
Package	8mmx13mm nFBGA 0.8mm Pitch	8mmx13mm nFBGA 0.8mm Pitch	5mmx5mm nFBGA 0.8mm Pitch	6mmx6mm fcBGA 0.5mm Pitch	8mmx13mm fcBGA 0.8mm Pitch
Front-Port Optical and Passive Connectors Supported	QSFP28 SFP28 CFP2/CFP4 CDFP 25G QSFP-DD	QSFP28 SFP28 CFP2/CFP4 CDFP 25G QSFP-DD	QSFP28 SFP28 CFP2/CFP4 CDFP 25G QSFP-DD	QSFP28 SFP28 CFP2/CFP4 CDFP 25G QSFP-DD	QSFP28 SFP28 CFP2/CFP4 CDFP 25G QSFP-DD
IEEE Standards Supported	100G-SR4/LR4/CR4 100G-KR4 CAUI-4	100G-SR4/LR4/CR4 100G-KR4 CAUI-4	100G-SR4/LR4/CR4 100G-KR4 (LT Disabled) CAUI-4	100G-SR4/LR4/CR4 100G-KR4 (LT Disabled) CAUI-4	100G-SR4/LR4/CR4 100G-KR4 (LT Disabled) CAUI-4
OIF Standards Supported	OIF-CEI-25G-LR/MR/SR/VSR	OIF-CEI-25G-LR/MR/SR/VSR	OIF-CEI-25G-LR/MR/SR/VSR	OIF-CEI-25G-LR/MR/SR/VSR	OIF-CEI-25G-LR/MR/SR/VSR

Table 4. TI 25G/28G Signal Conditioning Products Comparison (continued)

Features	DS280BR820	DS280MB810	DS250DF230	DS250DF410	DS280DF810
Other Standards Supported	CPRI, eCPRI, JESD204, OTN(ITU-T G.709), Infiniband EDR Fibre Channel	CPRI, eCPRI, JESD204, OTN(ITU-T G.709), Infiniband EDR Fibre Channel	CPRI, eCPRI, JESD204, OTN(ITU-T G.709), Infiniband EDR Fibre Channel	CPRI, eCPRI, JESD204, OTN (ITU-T G.709), Infiniband EDR Fibre Channel	CPRI, eCPRI, JESD204, OTN(ITU-T G.709), Infiniband EDR Fibre Channel
Debug Features	Signal Detect Interrupt Pin	Signal Detect Interrupt Pin	On-Chip Eye Opening Monitor PRBS Gen/Chkr Signal Detect, Interrupt Pin	On-Chip Eye Opening Monitor PRBS Gen/Chkr Signal Detect, Interrupt Pin	On-Chip Eye Opening Monitor PRBS Gen/Chkr Signal Detect, Interrupt Pin
Pin Compatible With	DS280BR810, DS280MB810, DS250DF810, DS280DF810	DS280BR810, DS280BR820, DS250DF810, DS280DF810	N/A	N/A	DS280BR810, DS280BR820, DS280MB810, DS250DF810

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2019) to A Revision	Page
• Updated application note throughout	2

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