Application Note

KSZ8081MNX/RNB to DP83826 System Rollover

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ABSTRACT

This application report outlines the necessary and potential steps for replacing the Microchip KSZ8081MNX/RNB 10/100 Mb/s Ethernet PHY with TI's DP83826.

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Trademarks

1 Purpose

While the KSZ8081MNX/RNB and the DP83826 have many similarities, several extra features are included in the DP83826, improving performance and system optimization. This system rollover document outlines how to replace the Microchip KSZ8081MNX/RNB PHY with TI's DP83826 by comparing differences including required external components, pin functions, feature set, and register operation. The impact to a design is dependent on the PHY configuration and features used. For more information on the DP83826 in EtherCAT applications, refer to 'How and Why to Use the DP83826E for EtherCAT Applications'.

2 Required Changes

This section describes the modifications required to transition from the KSZ8081MNX/RNB to the DP83826.

2.1 Strap Resistor Value

The DP83826 supports either BASIC Mode or ENHANCED Mode. BASIC Mode supports the same bootstrap options as the KSZ8081. To set the DP83826 for BASIC Mode, pin 1, ModeSelect, must be tied to ground. In a KSZ8081 design, Pin 1 is already tied to GND, so there is no change needed to select the correct mode. To understand the difference between DP83826 BASIC Mode and ENHANCED Mode, refer to the DP83826 Datasheet.

Both devices use a 2-level strap that may require a pull-up or pull-down resistor. The table below shows the difference in pull-up and pull-down resistor values between the DP83826 and the KSZ8081. Refer to the TI Precision Labs Video 'How Do Ethernet bootstraps work?' to properly calculate the correct strap resistors.

Table 2-1. Strap Resistor Values

	KSZ8081MNX/RNB	DP83826
Pull-Up Resistor Value	4.7 kΩ	2.49 kΩ
Pull-Down Resistor Value	1.0 kΩ	2.49 kΩ

For specific strap options, please refer to the Appendix of this Application Note.

2.2 External Capacitor on Pin 2

The KSZ8081 requires two external decoupling capacitors on pin 2; 2.2uF and 0.1uF. The DP83826 only requires one external decoupling capacitor on pin 2 (CEXT); 2nF.

Table 2-2. Value of External Capacitor(s) on Pin 2

	KSZ8081MNX/RNB	DP83826
External Capacitor Value	2.2 µF and 0.1 µF	2 nF

2.3 Duplex Strap on Pin 16 (DP83826 Basic Mode)

- No change is needed on pin 16 whether KSZ8081 was being used in Half-Duplex or Full-Duplex mode, DP83826 will be in the same mode as KSZ8081 for given circuit.

Table 2-3. Full/Half Duplex Comparison

Pin NO.	KSZ8081MNX/RNB	DP83826 Basic Mode
Pin 16	1: Half Duplex (Default) 0: Full Duplex	1: Half Duplex (Default) 0: Full Duplex

2.4 Selecting 10M with Auto-Negotiation Enabled (DP83826 Basic Mode)

KSZ8081MNX and DP83826 default to 100M speed. To select 10M speed, KSZ8081 recommends a pull-down on the strap along with a series resistor on LED. For DP83826 Basic Mode, 10M speed selection is done through register configuration and the strap resistor on Pin 31 shall be removed.

- Remove the strap resistor on Pin 31 for 10M selection
- Program register 0x0004 with 0x0061 to select 10M speed when Auto-Negotiation is enabled
- Program register 0x0000 with 0x3300 to restart Auto-Negotiation

2.5 Configuring LED_1 for Tx and Rx Activity for EtherCAT Slave (DP83826 Basic Mode)

The DP83826 and KSZ8081MNX/RNB can use LED_1 to indicate Tx and Rx activity from a host ASIC or FPGA. Extended register configurations are required for DP83826.

- Program register 0x0460 either with 0x1000 for the LED to stay high OR with 0x0008 for a blinking LED
- Program register 0x0469 with 0x0004

2.6 Thermal Pad Adjustments in Layout

The DP83826 thermal pad is smaller than KSZ8081. The table below shows the difference in package and DAP dimensions between the KSZ8081 and DP83826. With the rollover between devices, there is still a sufficient gap between pins and DAP so that pins will not be shorted.

Table 2-4. Package and DAP dimension differences

	KSZ8081	DP83826
Package dimmsions	5x5 mm	5x5 mm
Max DAP dimensions	3x3 mm	2.2x2.2 mm

The recommended solution for best practices on the layout would be to match the solder paste stencil with the DP83826 thermal pad. This means reducing the solder paste from 3x3mm to 2.1x2.1mm.

2.7 Physical Layer ID Register

The PHY Identifier Register #1 (PHYIDR1) and #2 (PHYIDR2) allow system software to determine applicability of device specific software based on the vendor model number. The Identifiers Register #1 and Register #2 can be found in sections 9.5.3 and 9.5.4 of the DP83826 Datasheet. The vendor model number is represented by bits 9 to 4 in PHYIDR2 (Address 0x3) outlined below.

Table 2-5. PHYID Comparison

Register Address	Register Name	Register Description	Device	
			DP83826	KSZ8081MNX/RNB
0x03	PHYIDR2	PHY ID 2	0x010001b - BASIC 0x010011b - ENHANCED	0x010110b

3 Potential Changes

The following section describes the specific changes that may need to be changed in converting to a DP83826 design. The default values for the DP83826 vs. KSZ8081MNX/RNB may be enough for transition between parts.

3.1 MDIO Pull-Up Resistor on Pin 11

KSZ8081 requires an external pull-up resistor on the MDIO pin of the PHY. The DP83826 has an internal pull-up resistor of 10 kΩ on this pin. An additional external pull-up resistor can be added if necessary.

3.2 MDIO Register Writes

The DP83826 and KSZ8081MNX/RNB have both standard and extended SMI/MIIM (MDIO) registers.

DP83826 can access the standard registers through the indirect method (using standard registers 0x000D and 0x000E as outlined in IEEE 802.3). However, Microchip KSZ8081MNX/RNB can only access the standard register set through the direct method (without using 0x000D and 0x000E registers).

KSZ8081MNX/RNB also specifies the MMD address for all extended registers (for example “2 h”) while DP83826 only uses MMD address 31 (0x001F) for all extended register writes and reads.

3.3 Capacitors on Center Tap of Magnetics

KSZ8081MNX/RNB and DP83826 can use one 0.1uF capacitor on each center tap of magnetics if needed.

4 Informational Changes

This section describes feature differences between the DP83826 and KSZ8081.

Table 4-1. DP83826 vs. KSZ8081MNX/RNB Feature Set Comparison

Features	KSZ8081MNX/RNB	DP83826
VDDIO	1.8V, 2.5V, 3.3V	1.8V, 3.3V
NAND Tree Support	Supported	Not Supported
PHY Broadcast Address	Supported	Not Supported
MII Back-2-Back Mode	Supported	Supported in ENHANCED Mode for Repeater Functionality
Slow Oscillator Mode	Supported	Supported - known as Deep Power Down Mode

5 Pinout Mapping

5.1 Pin Mapping

The table below shows the pinout mapping between the DP83826 and KSZ8081MNX/RNB. For more details on the pin mapping as well as any updates made, please refer to the DP83826 Data sheet.

Table 5-1. Pinout Mapping

Pin No.	KSZ8081MNX/RNB Pin Functions	DP83826 BASIC Mode Pin Functions	DP83826 ENHANCED Mode Pin Functions
1	GND	Mode Select	Mode Select
2	VDD_1.2	CEXT	CEXT
3	VDDA_3.3	VDDA3V3	VDDA3V3
4	RXM	RD_M	RD_M
5	RXP	RD_P	RD_P
6	TXM	TD_M	TD_M
7	TXP	TD_P	TD_P
8	XO	XO	XO
9	XI	XI/50MHzIn	XI/50MHzIn
10	REXT	RBIAS	RBIAS
11	MDIO	MDIO	MDIO
12	MDC	MDC	MDC
13	PHYAD0 (RXD3)	RX_D3	RX_D3
14	PHYAD1 (RXD2)	RX_D2	RX_D2
15	RXD1/ PHYAD2	RX_D1	RX_D1
16	RXD0/ DUPLEX	RX_D0	RX_D0
17	VDDIO	VDDIO	VDDIO
18	RXDV/ CONFIG2	RX_DV/CRS _DV	RX_DV/CRS _DV
19	RXC/ B-CAST_OFF	RX_CLK/50 MHz_Output	RX_CLK/50 MHz_RMII
20	RXER/ ISO	RX_ER	RX_ER
21	INTRP/ NAND_Tree#	INT	PWRDN/INT
22	TXC	TX_CLK	TX_CLK
23	TXEN	TX_EN	TX_EN
24	TXD0	TX_D0	TX_D0
25	TXD1	TX_D1	TX_D1
26	TXD2	TX_D2	TX_D2
27	TXD3	TX_D3	TX_D3
28	COL/ CONFIG0	COL	COL/LED2/GPIO
29	CRS/ CONFIG1	CRS	CRS/LED3
30	LED0/ NWAYEN I	LED0	LED0
31	LED1/ SPEED	LED1	LED1
32	RST#	RST_N	RST_N

6 DP83826 Strap Configurations

6.1 Bootstrap Configurations

The following tables outline the DP83826 strap configurations in BASIC Mode. Unless stated otherwise in the previous subsections, the KSZ8081MNX/RNB strap configurations are analogous. This table and more details about the bootstrap configurations can be found in the DP83826 Data sheet.

Table 6-1. PHY Address Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D3	Strap7	13	1		PHY_ADD0
				0	0
				1	1
RX_D2	Strap8	14	0		PHY_ADD1
				0	0
				1	1
RX_D1	Strap9	15	0		PHY_ADD2
				0	0
				1	1

Table 6-2. MAC Mode Selection Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Strap 10	Strap 3	Strap4	Function
COL	Strap4	28	0	0	0	0	MII MAC Mode
				0	0	1	RMII Master Mode
				1	0	1	RMII Slave Mode
CRS	Strap3	29	0	Reserved			
RX_DV	Strap10	18	0				

Table 6-3. Auto Negotiation Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED0	Strap2	30	1	0	Auto Negotiation Disable
				1	Auto Negotiation Enable

Table 6-4. Speed Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED1	Strap1	31	1	0	Speed 10M
				1	Speed 100M

Table 6-5. Full/Half Duplex Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D0	Strap0	16	1	0	Full Duplex
				1	Half Duplex

Table 6-6. MII Isolate Bootstraps

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_ER	Strap6	20	0	0	MII Isolate Disable
				1	MII Isolate Enable

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2020) to Revision A (August 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.....1
- Updated Pin Mapping Section..... 6
- Added row for RMII slave mode configuration in Table 6-2 7

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