

# How and Why to Use the DP83826A for EtherCAT® Applications



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## ABSTRACT

This document describes how to connect DP83826A to an EtherCAT® ESC.

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## 1 Introduction

When starting an EtherCAT® design, first review [EtherCAT® Protocol, Physical Layer, EtherCAT™ Processing Unit, FMMU, SyncManager, SII EEPROM, Distributed Clocks Data Sheet](#). This document describes how to connect an Ethernet PHY onto an EtherCAT® ESC. The document also describes the needed interfaces between the ESC and Ethernet PHYs. These interfaces are the PHY Management Interface (PHY MI) and EtherCAT Interface, and are illustrated in Figure 1 from the previously referenced data sheet. In chapter 4 (Physical Layer Common Features) and 5 (Ethernet Physical Layer), the interface between the ESC and the PHY is described. Some key points to takeaway here include:

- ESC in reset state has to leave the PHY disabled (No link connection until active ESC)
- MII interface has special use for TX\_CLK, COL, CRS, TX\_ER pins; for details, see table 14 (Special/Unused MII Interface signals).
- EtherCAT® has a special setup to determine Link Detection in several steps; see section 5.6 for details
- LINK\_MII signal, this is typically an LED output signal which indicate a 100 Mbit/s Full Duplex link
- Enhanced link detection which is making sure that the link signal is checked every approximately 10µs; see section 5.6.2 for details

## 2 EtherCAT® Specification Requirements and Recommendations

Another reference to look into is for EtherCAT PHY specification. This is found in the [PHY Selection Guide](#) application note on the EtherCAT® home page.

The following list shows version 3.1 of the PHY Selection Guide (2025-05-05) compared with DP83826A's compliance to the requirements. Additional data sheet reference for DP83826A is provided in parenthesis.

1. The PHYs have to comply with IEEE 802.3 100Base-TX or 100Base-FX.
  - a. *DP83826A is IEEE 802.3 compliant (9.1)*
2. The PHYs have to support 100Mbit/s Full Duplex links.
  - a. *DP83826A supports 10Mbit/s and 100Mbit/s full duplex operation (8.5.1.5)*
3. The PHYs have to provide an MII (or RMII/RGMII) interface.
  - a. *DP83826A provides an MII or RMII interface (9.1)*
4. The PHYs have to use auto-negotiation in 100Base-TX mode.
  - a. *DP83826A has a strap controlled auto-negotiation feature (8.3.1)*
5. The PHYs have to support the MII management interface.
  - a. *DP83826A supports serial management interface (8.3.11)*
6. The PHYs have to support MDI/MDI-X auto-crossover in 100Base-TX mode.
  - a. *DP83826A supports this via Auto-MDIX feature (8.3.2)*
7. PHY link loss reaction time (link loss to link signal/LED output change) has to be faster than 15 µs to enable redundancy operation.
  - a. *DP83826A has Fast link-Drop (FLD) functionality, which shortens the observation window to 10 µs before enabling the link loss indication (8.3.17)*
8. The PHYs must not modify the preamble length.
  - a. *DP83826A does not modify the preamble length (N/A)*
9. The PHYs must not use IEEE802.3az Energy Efficient Ethernet.
  - a. *DP83826A supports the IEEE802.3az standard. This feature is disabled by default (8.3.3.1)*
10. The PHYs must offer the RX\_ER signal (MII/RMII) or RX\_ER as part of the RX\_CTL signal (RGMII).
  - a. *DP83826A supports MII/RMII including the RX\_ER signal (8.3.9)*
11. The PHYs have to provide a signal indicating a 100Mbit/s (Full Duplex) link, typically a configurable LED output. The signal polarity is active low or configurable for some ESCs.
  - a. *DP83826A has programmable LED outputs which can each show 100Mbit/s Full Duplex link (8.5.1.67)*

12. The PHY addresses can be equivalent to the logical port number (0–3). Some ESCs also support a fixed offset (for example, offset 16, PHY addresses are logical port number plus 16: 16-19), an arbitrary offset, or even individually configurable PHY addresses. If none of these possibilities can be used, the PHY address can be configured to logical port number plus 1 (1–4), although some features (for example, Enhanced Link Detection) cannot be used in this case, because apart from the optional configurable PHY address offset, the PHY addresses are hard-coded inside the ESCs.
  - a. *DP83826A has eight PHY addresses which can be set using strap resistors (8.4.1.1)*
13. PHY configuration must not rely on configuration via the MII management interface, that is, required features have to be enabled after power-on, for example, by default or by strapping options. PHY startup needs to not rely on MII management interaction, that is MDC clocking, since many ESCs do not communicate with the PHY via management interface unless the EtherCAT® master requests this (only the EtherCAT® IP Core with MI Link detection and configuration can communicate without master interaction).
  - a. *DP83826A has bootstrap configurations for setting the PHY in a specific mode which allows EtherCAT® communication (5)*
14. All PHYs connected to one ESC and the ESC itself must share the same clock source, so a TX FIFO can be omitted. This can be achieved by sourcing the PHYs from an ESC clock output or by sourcing the PHYs and the ESC from the same quartz oscillator. The ESC10/20 uses TX\_CLK as a clock source, both PHYs have to share the same quartz oscillator.
  - a. *This can be resolved using an external clock source for DP83826A as long as specification for this clock source is followed. DP83826A also has a clock out option which can be used to source second PHY's clock (8.3.8)*
15. The phase offset between TX\_CLK and the clock input of the PHYs is compensated inside the ESC, either manually by configuration or automatically. The clock period cannot change between the devices since the PHYs and the ESC have to share the same clock source.
  - a. *This requirement is for the MAC interface and is PHY independent (N/A)*
16. Manual TX Shift compensation: ET1100, ET1200, and IP Core provide a TX Shift configuration option (configurable TX\_EN/TXD signal delay by 0/10/20/30ns) which is used for all MII ports. Thus, all PHYs connected to one ESC must have the same fixed phase relation between TX\_CLK and the clock input of the PHY, with a tolerance of  $\pm 5$  ns. The phase relation has to be the same each time the PHYs are powered on, or establish a link. As the ESC10/20 use TX\_CLK as device clock source, configuration is not necessary, but the requirements for manual TX Shift compensation have to be fulfilled anyway.
  - a. *DP83826A has a nominal  $\pm 2$ ns tolerance of this specification, with maximum of  $\pm 4$ ns (7.6)*
17. Automatic TX Shift compensation: The IP Core supports automatic TX Shift compensation individually for each port. With automatic TX Shift compensation, the PHYs are not required to have the same fixed phase relation each time they are powered on, or establish a link.
  - a. *This requirement is for the MAC interface and is PHY independent (N/A)*

Table 2-1 shows a copy of *PHY Selection Guide*, application note document version 3.1 (2025-05-05) compared with DP83826A's compliance to the recommendation. Additional data sheet reference for DP83826A is provided in parenthesis.

**Table 2-1. PHY Selection Guide**

<b>PHY Selection Guide Recommendation</b>	<b>DP83826A Compliance Recommendation</b>
Receive and transmit delays needs to be deterministic, and as low as possible.	DP83826A RX and TX signal latency based on the MII interface is $\pm 2\text{ns}$ (7.6)
Maximum cable length needs to be $\geq 120\text{m}$ to maintain a safety margin if the standard maximum cable length of 100m is used.	DP83826A has been tested to be above 150m (1)
ESD tolerance needs to be as high as possible (4kV, or better)	DP83826A has been tested without external protection to withstand ESD Ratings based on HBM for MDI pins ( $\pm 5\text{kV}$ ) and all pins other pins ( $\pm 2\text{kV}$ ) and on CDM for all pins $\pm 0.75\text{kV}$ . With external protection IEC 61000-4-2 ESD: $\pm 8\text{kV}$ contact, $\pm 15\text{kV}$ air and for IEC 61000-4-4 EFT: $\pm 4\text{kV}$ at 5kHz and 100kHz. (7.2, 1)
Baseline wander needs to be compensated (the PHYs needs to cope with the ANSI X3.263 DDJ test pattern for baseline wander measurements at maximum cable length)	DP83826A has been tested and shows excellent performance compensating the baseline wander. It is recommended that register 0xB[0] is set to 0, otherwise the baseline wander test can fail because the PHY drops the link as to the energy detection mechanism is seeing the test pattern as a link drop. (8.5.1.12)
The PHYs needs to detect link loss within the link loss reaction time of $15\mu\text{s}$ also if only one of the RX+ and RX- lines gets disconnected.	Fast Link-Drop functionality shortens the observation window to $10\mu\text{s}$ before enabling the link loss indication (8.3.17)
The PHYs needs to maintain the link state regardless of the received symbols, as long as the symbols are valid.	The PHY can be able to maintain the link state so long as the fast link drop functionality determines no reason to drop link (8.3.17)
Ethernet PHYs for 100Base-FX needs to implement Far- End-Fault(FEF) completely (generation and detection).	DP83826A is a 100Base-TX PHY and does not support 100Base-FX (1)
MDC needs to not incorporate pullup, pulldown resistors, as this signal is used as a configuration input signal by some ESCs.	MDC has an internal pulldown resistor (nominal $10\text{k}\Omega$ ). This has to be taken into account when defining pullup (7.5)
Restriction of Auto-negotiation advertisement to 100Mbit/s/ Full Duplex is desirable (configured by hardware strapping options).	Advertisement can be set by strap configuration (8.4.1)
Power consumption needs to be as low as possible.	Worst-case power consumption for MII interfaced 100BaseTX is a total of 70mA at 3.3V VDDA and VDDIO levels (7.5)
I/O voltage: 3.3V needs to be supported for current ASIC and FPGA ESCs, an additional 2.5V, 1.8V I/O support is recommended for recent FPGA ESCs.	DP83826A supports 3.3V and 1.8V I/O voltage (7.3)
Single power supply according to I/O voltage.	DP83826A supports single power supply at 3.3V (8.1)
The PHY needs to use a 25MHz clock source (quartz oscillator or ESC output).	The DP83826A supports Crystal and oscillator inputs (9.2.4)
Industrial temperature range needs to be supported.	DP83826AE supports a temperature range from $-40$ to $105^\circ\text{C}$ (1)

### 3 Different Methods of Setting up the PHY

To setup the PHY in the correct mode for it to work in the EtherCAT® environment there are some settings which either have to be setup using the Serial Management Interface or by using strap configuration. This setup is like programming the PHY to be setup in a specific mode. The following two sections describe how to setup the PHY.

#### 3.1 Using Strap Configuration to Set Up DP83826A PHY for EtherCAT® Configuration

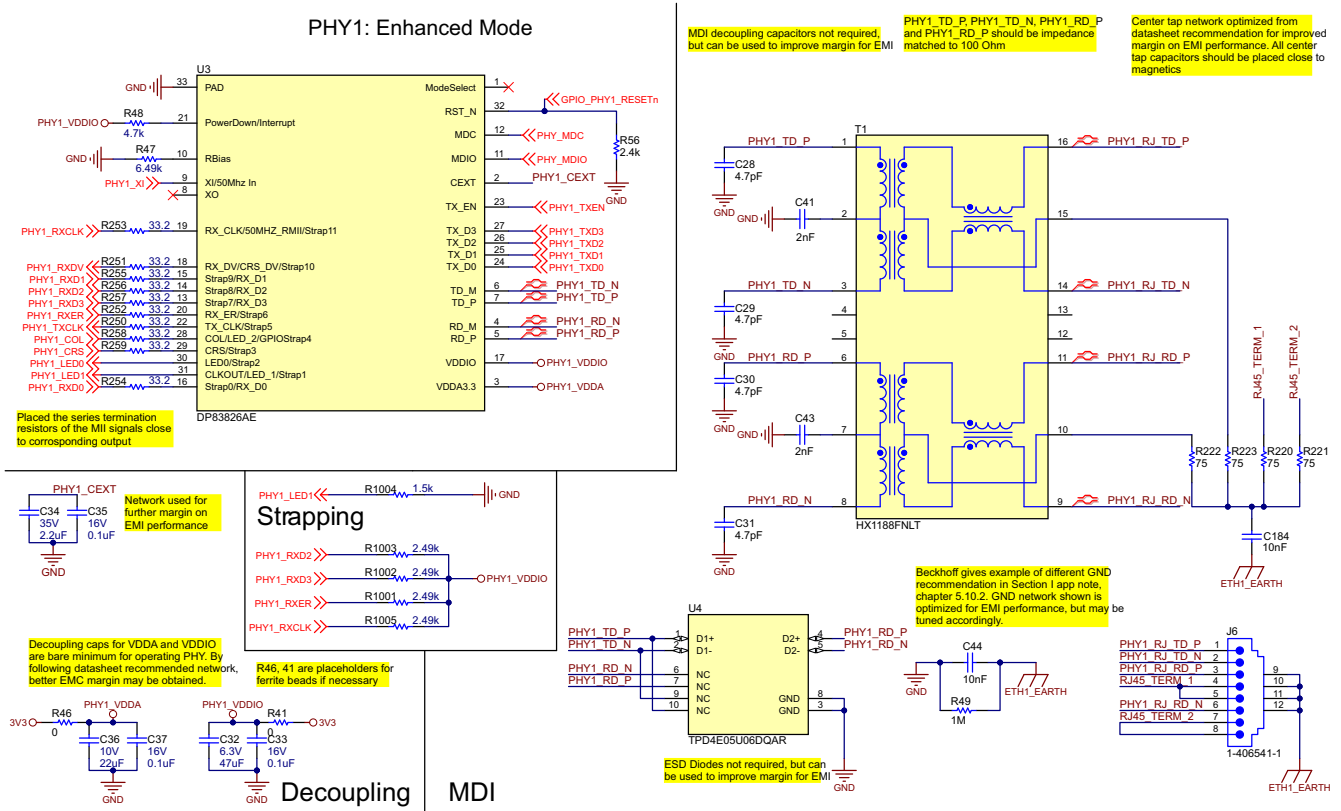


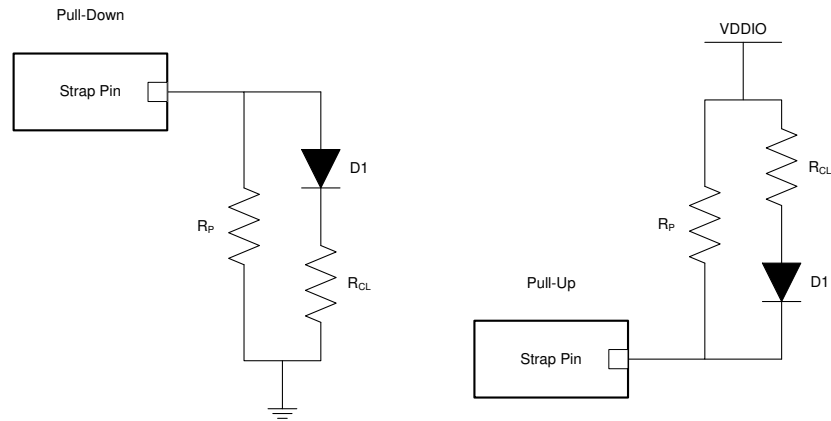
Figure 3-1. DP83826A Enhanced Mode Example

#### 3.1.1 Strapping Options

The *Hardware Bootstraps Configuration* section in the [DP83826A Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY](#) data sheet describes how the device can be configured without using the Serial Management Interface (SMI). This section of the data sheet presents configuration options in *ENHANCED* and *BASIC* modes. If SMI is not used to program the PHY, the DP83826A must be hardware set up in *Enhanced* mode to enable EtherCAT functionality.

When setting up the PHY to work in an EtherCAT® system, the PHY has an LED which is set up to show 100Mbit full duplex and the signal polarity is active low or configurable for some ESCs.

To define the LED polarity, the following circuit can be used to make either active-high or -low polarity configuration. The PHY has an internal circuit which measures the polarity that is needed and automatically configures depending on the input signal. [Figure 3-2](#) shows the recommended networks for an active high pull-down strap circuit and an active low pull-up circuit.  $R_P$  is used to define the strap network, while  $R_{CL}$  is a current limiting resistor to protect the LED component.



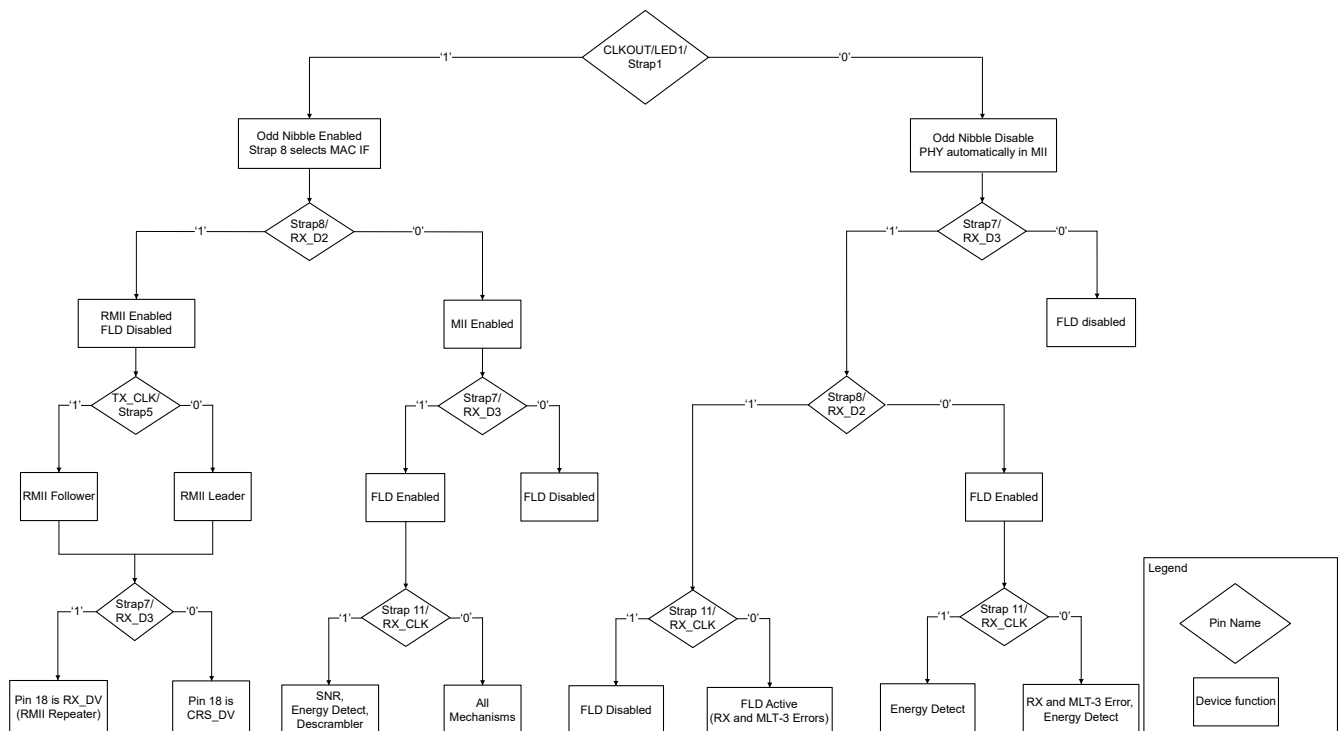
**Figure 3-2. Example Strap Connections**

In some cases, pending the strap settings this automatic LED feature has been disabled, see section 9.4.1, *Hardware Bootstrap Configuration*, in data sheet for more details.

Table 3-1 can be used to determine resistor values for bootstrapping the PHY.

**Table 3-1. 2-Level Strap Resistor Ratios**

Mode	Suggested Resistors	
	R <sub>HI</sub> (kΩ)	R <sub>LO</sub> (kΩ)
<b>Internal 10kΩ Pulldown (PD) Pins</b>		
0-DEFAULT	OPEN	OPEN
1	2.49	OPEN
<b>Internal 10kΩ Pullup (PU) Pins</b>		
0	OPEN	1.5
1-DEFAULT	OPEN	OPEN



**Figure 3-3. DP83826A Enhanced Mode Strapping Flowchart**

FLD needs to be enabled using Signal or Energy loss as a detection feature for robust immunity performance. When setting up the DP83826A device in an EtherCAT system, use the configuration shown in [Table 3-2](#).

**Table 3-2. DP83826A Strap Pin Configuration for EtherCAT®**

Strap Number   Pin (Pin Name)	Enhanced Mode Functionality	Default	Strap Setting
Strap 0   pin 16 (RX_D0)	Auto negotiation configuration Force 100Mbps if auto-negotiation is disabled	0	0 (Enable auto-negotiation)
Strap 1   pin 31 (CLKOUT/LED1)	Odd Nibble Detection configuration When enabled, if PHY sees an uncompleted nibble of data on line, can corrupt the data and yield RX Errors.	1	0 (Disable Odd-Nibble Detection) MII is selected as the MAC interface.
Strap 2   pin 30 (LED0)	PHY_ADD0	0	Define address with pull up
Strap 3   pin 29 (CRS/LED3)	PHY_ADD1	0	Define address with pull up
Strap 4   pin 28 (COL/LED2)	PHY_ADD2	0	Define address with pull up
Strap 5   pin 22 (TX_CLK)	RMII mode configuration (Leader/Follower)	0	0 (Leader mode) Don't care, Strap 1 forces MII
Strap 6   pin 20 (RX_ER)	Functionality on Pin 31 (CLKOUT or LED1)	0	1 (LED1)
Strap 7   pin 13 (RX_D3)	Enable Fast Link Drop functionality	0	1 (FLD enabled)
Strap 8   pin 14 (RX_D2)	Strap low for signal energy detect FLD	0	0 (Signal Energy Detect)
Strap 9   pin 15 (RX_D1)	Auto MDIX Configurability	0	0 (Auto-MDIX enabled)
Strap 10   pin 18 (RX_DV)	Auto-MDIX Disable mode: Set MDI or MDIX	0	0 (MDIX) Don't care, auto MDIX enabled
Strap 11   pin 19 (RX_CLK)	Toggles RX and MLT3 error counters for FLD detection	0	1 (Disable error-counter FLD)
Pin 1 (ModeSelect)	Mode Select: Enhanced or Basic	1	1 (Enhanced mode)

### 3.2 Using Serial Management Interface to Setup DP83826A PHY

For this design, the serial management interface method was used to program the PHY. Note that the PHY is in Basic mode for this example to force reliance on register programming.

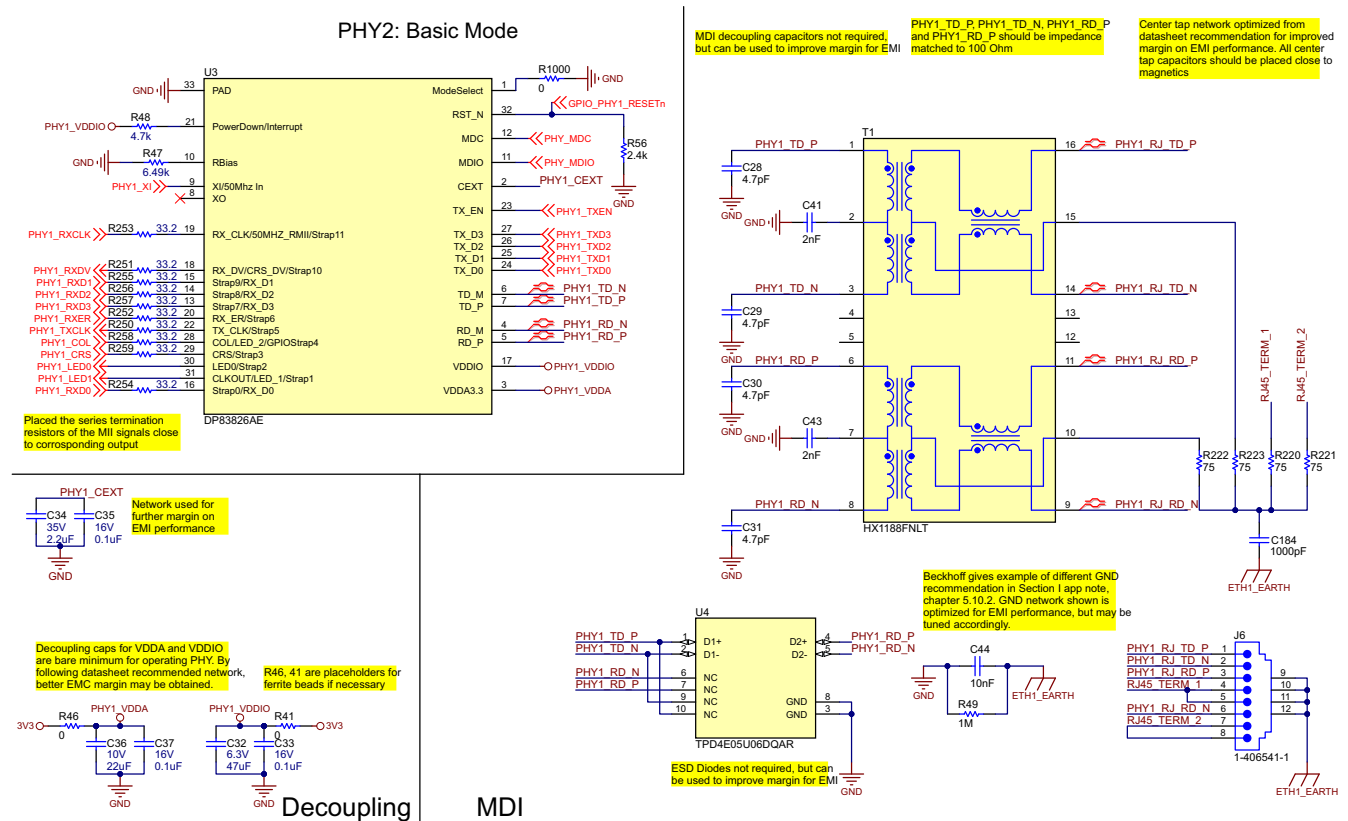


Figure 3-4. DP83826A Basic Mode Example

#### 3.2.1 Programming Options

##### DP83826A Register Setup

When setting up DP83826A to work for EtherCAT®, the following registers are written as follows:

- LED 0**  
Write to PHY register 0x0019 value 0x8020 (*Auto-MDIX enable and enable LED0 config*)  
Write to PHY register 0x0018 value 0x0080 (*Active High polarity*)
- LED 1**  
Write to PHY register 0x0460 value 0x0005 (*100Mbit speed*)  
Write to PHY register 0x0469 value 0x0004 (*Active High polarity*)  
Write to PHY register 0x0304 value 0x0008 (*Set pin 31 function to LED1*)
- Auto Negotiate Enable**  
Write to PHY register 0x0004 value 0x01E1 (*Advertise which modes PHY support*)  
Write to PHY register 0x0009 value 0x0020 (*Enable Robust Auto MDIX*)  
Write to PHY register 0x0000 value 0x3300 (*Enable Auto negotiate and restart process*)
- Odd-nibble Detection Disable**  
Write to PHY register 0x000A value 0x0002 (*Disable odd-nibble detection*)
- Fast Link-Drop Enable**  
Write to PHY register 0x00B value 0x0001 (*Enable FLD with Signal/Energy loss*)

With the previous write functions, the following register settings can now be read out of both PHYs.

**Table 3-3. DP83826A Register Dump in Working EtherCAT® Configuration**

Register Address	MDIO PHY Address
0x0	0x3100
0x1	0x786D
0x3	0xA11X
0x4	0x01E1
0x7	0x2001
0x8	0x0000
0x9	0x0020
0xA	0x0002
0xB	0x0001
0xF	0x0000
0x11	0x10B
0x14	0x0000
0x15	0x0000
Extended Registers <sup>(1)</sup>	
0x25	0x0041
0x304	0x0008
0x460	0x0005
0x469	0x0004

(1) Extended Register access requires a [4-step process](#)

## 4 References

1. Texas Instruments, *DP83826A Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY*, data sheet.
2. Texas Instruments, *KSZ8081 to DP83826E System Rollover*, application note.
3. Beckhoff, *PHY Selection Guide*, application note.
4. Beckhoff, *EtherCAT® Protocol, Physical Layer, EtherCAT® Processing Unit, FMMU, SyncManager, SII EEPROM, Distributed Clocks*, data sheet

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