DS3884A

Application Note 744 Futurebus+ Wired-OR Glitch Effects and Filter

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Futurebus+ Wired-OR Glitch Effects and Filter

National Semiconductor
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INTRODUCTION

Futurebus+ addresses the needs of the high-end user who requires more bus performance than what has previously existed. In order to optimize bus performance, the backplane bandwidth has been increased to where the backplane line delays are in the same order of magnitude as the transfer periods. At this level, the backplane can no longer be treated as lumped loads but must be modeled as distributed loads which is in the realm of transmission lines. Designers must now deal with transmission line effects and be aware of glitches that occur when performing wired-OR functions. As the name implies, the wired-OR glitch occurs on lines that perform wired-OR logic. Wired-OR logic is implemented by connecting open-collector drivers in parallel and tying their collectors to a resistor pull-up (*Figure 1*). National Semiconductor's Futurebus+ Handshake Transceiver addresses this concern by incorporating a programmable low pass filter into the receiver. It provides optimum noise rejection while maintaining high bus through-put.

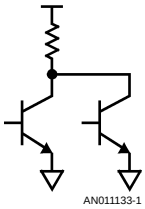

FIGURE 1.

BTL (Backplane Transceiver Logic) is the driving technology behind the Futurebus+ physical layer. Driver outputs are open-collector with a series Schottky diode. The additional diode on BTL drivers isolates the normally large collector capacitance associated with the output transistor from the bus thus reducing bus loading. BTL is used on all the bus lines in a Futurebus+ backplane. Termination of the bus is done at both ends as shown in *Figure 2*. All Futurebus+ lines are connected in a wired-OR fashion, however, only a subset of these lines actually perform the wired-OR logic. These lines are the handshake, status, capability and arbitration lines. The critical timing lines used in handshaking must have wired-OR glitch filters to maintain signal integrity. The lines requiring glitch filtering are AK*, AI*, DK*, DI*, AP*, AQ*, AR*, and RE*.

In the wired-OR configuration, the glitch observed on the backplane is caused by the release of one or more drivers on the bus while others remain asserted. The resulting positive voltage pulse is the glitch characteristic that could cross the receiver threshold and degrade signal integrity. The transmission line effect, enhanced by the fast transition times and transmission line propagation delay, dictates how the wave reflections will affect the data signal. If the rise and fall times were longer than the line delays, the reflections would be included (shadowed) in these transition portions of the signal. Then the bus would not exhibit transmission line effects. However, the Futurebus+ transition times on the backplane can be one fourth to one fifth of the line delay. A transition at one end of the backplane takes some time before it reaches the other end and voltage levels will vary significantly, due to reflections, before equilibrium.

Low to High Transition of Open Collector Bus Driver

First the low to high transition of a single driver releasing the bus will be studied. The same characteristics are involved for the wired-OR glitch as will be seen later. Referring to *Figure 3*, what happens when Q1 releases?

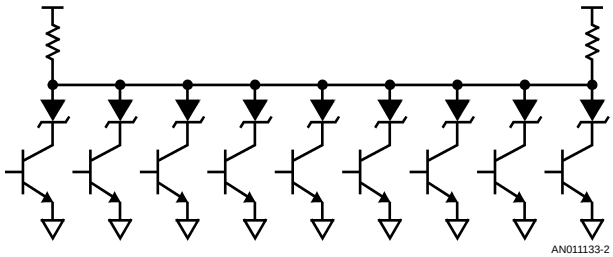

FIGURE 2.

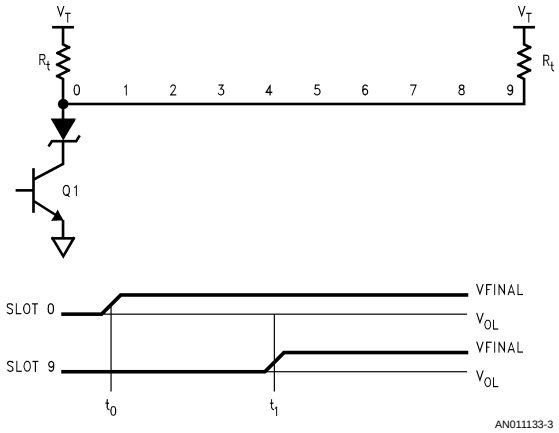

FIGURE 3.

$t < t_0$; Q1 is on (asserted) and maintains a V_{OL} level on the bus.

$$V_{OL} = V_T * \frac{Zdriver}{Zdriver + (R_t/2)}$$

where Zdriver = driver output impedance

$t = t_0$; Q1 releases and a low to high wave front propagates from slot 0 towards slot 1. The current which was previously sunk by Q1 now gets injected back into the line. The driver sees an impedance of the termination resistance in parallel with the line impedance. The amplitude of the signal propagating down the line is described by the following equation:

$VFINAL = V_{OL} + [I_{OL} * (R_t//Z_0')]$

$$= V_{OL} + \frac{V_T - V_{OL}}{R_t/2} * (R_t//Z_0') \quad (1)$$

For $R_t = Z_0'$, where Z_0' is the unloaded line impedance.

$VFINAL = V_{OL} + V_T - V_{OL}$

$= V_T$

If the driver was located in slots 1 to 8 then the equation would be;

$$VFINAL = V_{OL} + \frac{V_T - V_{OL}}{R_t/2} * (Z_0'//Z_0') \quad (2)$$

$t = t_1$; The signal reaches slot 9. For $R_t = Z_0'$, all the energy is absorbed at slot 9 by the termination and the bus will be at equilibrium. For $R_t \neq Z_0'$ then secondary reflections will occur until the reflections settle.

Figure 4 shows the actual waveform from a 10 slot backplane with 1 in. pitch and 39Ω termination resistors. The 3 waveforms were obtained by probing the backplane at the solder points of the board connectors. In this case there were two boards inserted into the backplane, slots 0 and 9. The driver in slot 0 is switching while the other in slot 9 is off. The propagation delay of the line, tpd, is then defined as $t_1 - t_0$. This is plainly illustrated by the delay in the waveform probed at slot 0 and at slot 9. The tpd = 3 ns in this arrangement.

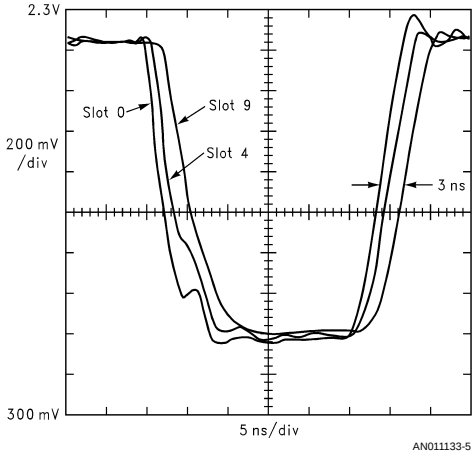

FIGURE 4.

Wired-OR Glitch

As shown in *Figure 5*, things become more complicated by adding another driver at the opposite end of the bus. Initially, both drivers are asserted. Assuming they share the current from the termination equally, the V0 will be less than V_{OL} for a single driver. V0 is also influenced by the fact that the driver impedance increases with reduced current through the transistor. When Q1 releases, a glitch occurs at the drivers bus slot with a pulse-width equal to 2 times the line delay. The glitch amplitude is dependent on the amount of current that was sunk by the driver prior to releasing the line. So the more drivers that release the line simultaneously, the greater the amplitude of the glitch.

$t < t_0$ Both Q1 and Q9 are on keeping the bus voltage low. Note that V0 results from the resistor divider between the parallel driver output impedance and the parallel termination resistance. V2 is slightly higher because only one driver is on and the bus voltage is then just the resistor divider between a single driver output impedance and the two termination resistors in parallel.

$t = t_0$ Q1 turns off and transitions into a high impedance state, a low to high wave front propagates down the bus towards slot 9.

$$V1 = V0 + \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0' \quad (3)$$

For $R_t = Z_0'$

$$V1 = V0 + \frac{1}{2}(V_T - V0)$$

$$= \frac{1}{2}(V_T + V0) \quad (4)$$

$t = t_1$ The glitch reaches slot 9 and the reflection at slot 9 is negative because the output impedance of the driver is small compared to the termination resistor and backplane impedance.

$$V2 = V1 + \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0' * \rho$$

$$\text{where } \rho = \frac{R_t//Z\text{driver} - Z_0'}{R_t//Z\text{driver} + Z_0'} \text{ (negative number)}$$

$t = t_2$ The reflected wave reaches slot 0. It is important to point out that the output of Q1 is in a high impedance state when turned off. Therefore, the mismatch at slot 0 is only due to the backplane impedance and termination. For $R_t = Z_0'$, all the energy is absorbed at slot 0 by the termination and the bus will be at equilibrium. When $R_t \neq Z_0'$, then secondary reflections will occur and will continue until the reflections settle to the termination voltage.

The pulse width at the end of the backplane where the driver is still asserted is as wide as the propagation delay of the bus. Since the reflection must return to the released driver end, the pulse width there will be 2 tpd, where tpd = $(t_1 - t_0)$ = $(t_2 - t_1)$.

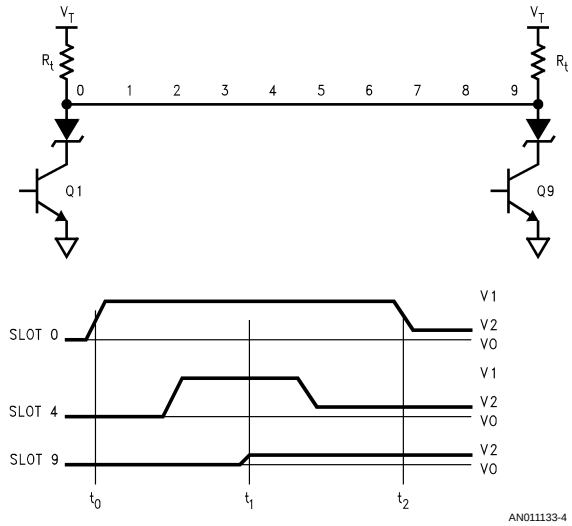

FIGURE 5.

Wired-OR Glitch Calculation for Futurebus+

To simplify the wired-OR glitch calculation for a Futurebus+ backplane, the following assumptions are used;

Z_0'	60Ω	Unloaded Backplane with Connector and Vias
Z_0"	31Ω	Fully Loaded Backplane
R_t	33Ω	Termination Resistor
$R_t//Z_0$'	21Ω	
$R_t//Z_0$"	16.0Ω	
R_t//Zdriver	4.3Ω	
Zdriver	5Ω	Driver Series Resistance
Vdriver	0.7V	Driver on Voltage in Series with the Resistance
V_T	2.1V	Termination Voltage
V_{TH}	1.47V to 1.62V	Receiver Input Threshold
tpd	1.8 ns	Unloaded, 10 Slot by 1 in. Pitch Backplane
	4.4 ns	Same Backplane Fully Loaded

For drivers at each end (*Figure 5*) and assuming an Unloaded condition we have;

$$V0 = Vdriver - (V_T - Vdriver) * \frac{\frac{1}{2}Zdriver}{\frac{1}{2}Zdriver + \frac{1}{2}R_t}$$

V0 = 0.52V

From *Equation (3)*

$$V1 = V0 + \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0$$

V1 = 1.3V

When the reflected wave hits the mismatch at slot 9, a negative reflection adds to V1.

$$V2 = V1 + \rho^1 * V_x^1 \qquad \rho^1 = \frac{R_t//Zdriver - Z_0'}{R_t//Zdriver + Z_0'}$$

$$= 0.62V \qquad Vx^1 = \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0'$$

When this wave front reaches slot 0, another negative reflection adds to V2.

$$V3 = V2 + \rho^2 * Vx^2 \qquad \rho^2 = \frac{R_t - Z_0'}{R_t + Z_0'}$$

$$= 0.78V \qquad Vx^2 = Vx^1 * \rho^2$$

Subsequent reflections will be smaller and smaller until equilibrium is reached on the line.

The glitch has a maximum amplitude of 1.3V for two drivers sharing the bus current equally, which is below the receiver threshold of 1.47V. This isn't enough amplitude to false trigger the receiver and thus data corruption will not occur. The glitch also has a maximum pulse width equal to 2 tpd or 3.6 ns. If Q1 was sinking most of the current, then the resulting glitch will have a greater amplitude than that calculated, but the pulse width will remain the same. The greater amplitude may cross the receiver threshold and cause false triggering. The purpose of the glitch filter on the DS3884 is to filter any glitch that crosses the receiver threshold and thereby

prevent false triggering. Since the glitch width is independent of amplitude, a filter can be set to reject certain duration glitches.

Figure 6 shows actual waveforms from the 10 slot backplane. The drivers are mounted in the end slots and R_t = 39Ω. The Vdriver (1 driver on) level is 685 mV and VO (2 drivers on) is 545 mV. The switching driver is shown without the other driver asserted, waveform A in *Figure 6*. Then the wired-OR glitch is shown at the end slots with one driver switching and the other holding the asserted level, waveforms B and C. As predicted by the model, the amplitude and pulse width of the glitch is greatest at the driver slot that is releasing the line. The maximum amplitude of the glitch is 1.25V. The propagation delay of the backplane with 2 boards inserted was shown in *Figure 4* to be 3 ns. The model predicted the pulse width to be twice this delay, but it is shown to be 2.33 times the delay at 50% of the amplitude. This is because the model does not take into account the wave dispersion effects of the backplane which filter the high frequency components and round the signal corners. Since the glitch amplitude will never equal V_T as indicated by *Equation (3)*, the glitch pulse width at the receiver threshold will always be less than the 50% amplitude pulse width. Two times the measured backplane propagation delay is the worst case width that will be seen at the receiver threshold.

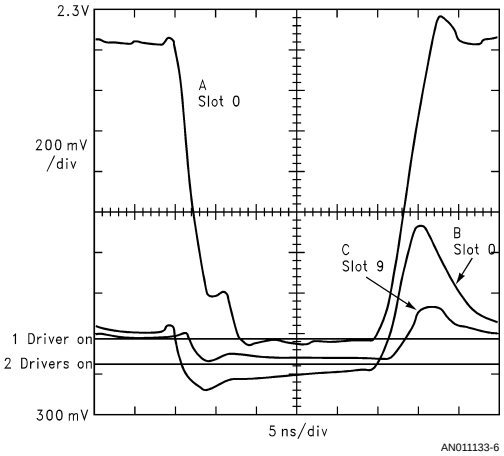

FIGURE 6.

Theory states that glitch width is only dependent on the bus propagation delay. (*Figure 7* and *Figure 8* are included to demonstrate this theory in the backplane application. *Figure 7* shows the glitch for a 1 MHz signal. The pulse width is the same as that in *Figure 6* which has a 20 MHz signal. *Figure 8* is the same situation as *Figure 6* except that the backplane slots between 0 and 9 are loaded with 10 pF to 12 pF each. This increases the propagation delay of the backplane. The width of the pulse is 10.7 ns. Using the fully loaded backplane tpd of 4.4 ns, this pulse width is 2.43 times the propagation delay. This figure correlates well with the previous partially loaded glitch width. The amplitude is noticeably less when the backplane is fully loaded due to the decreased impedance seen by the driver.

The simultaneous release of the bus line by more than one driver at a time will increase the amplitude of the glitch but the width still depends on the propagation delay of the bus. The current of more than one driver injected into the line directly affects the amplitude of the pulse. *Figure 9* shows the glitch when 2 drivers release the line simultaneously and 1 holds the line asserted. The releasing drivers are in slots 0 and 3, and the hold driver is in slot 9. The glitch amplitude of 1.81V will cause a false trigger of receivers on the line. The pulse width of the glitch at the receiver threshold low is 6 ns, about 2 tpd. The 50% of amplitude pulse width is slightly larger than the case of 2 drivers on the bus, but this is explained by the additional load capacitance of the third driver which increases the line delay.

WIRED-OR FILTER

The worst case glitch that can occur on the bus will have a pulse width equal to the round trip delay of the backplane. The filter must reject glitch pulses which are equal to and less than the worst case round trip bus delay, 2 tpd. Since the line delay is dependent on the length and the loading of the backplane, the simplest way to determine the worst case delay is by measuring the line delay of a fully populated backplane. Once the worst case delay is determined, the receivers should provide a filter that will reject the glitch and allow signals to pass through with minimum delay.

The DS3884A Handshake Transceiver which is part of National's Futurebus+ chip set has a built in glitch filter. The filter can be tailored to a specific backplane delay to minimize timing delays. Four different settings — (5 ns, 10 ns, 14 ns and 24 ns) are available via the pulse select pins — PS1 and

PS2. For example, if the round trip delay of the backplane is 8 ns, then the filter setting should be rounded-off to the higher setting which is 10 ns.

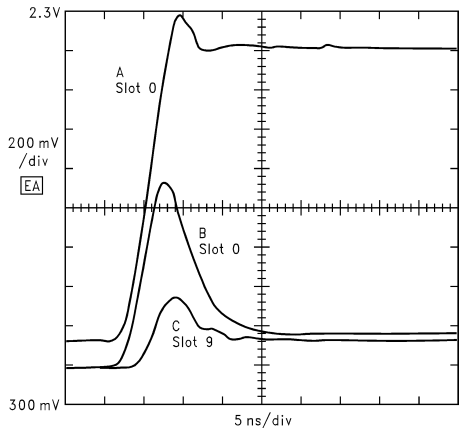

FIGURE 7.

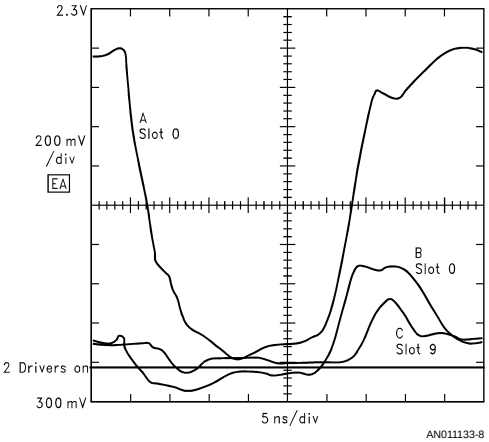

FIGURE 8.

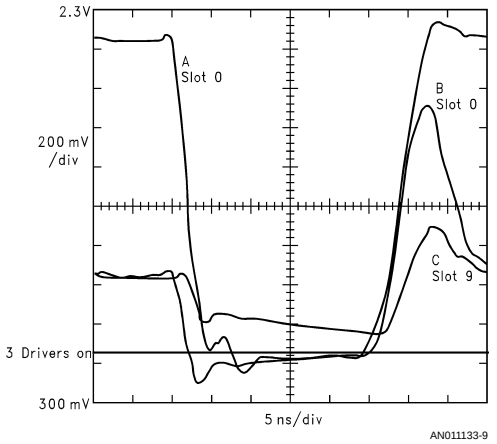

FIGURE 9.

This setting will reject glitches with pulse widths of 10 ns and less. The maximum propagation delay from the transceiver bus input, Bn, to the filtered receiver output, FRn, for the receiver high to low transition will be 21 ns at this setting. *Figure 10* shows three waveforms from the DS3884A operating in slot 0 of the same backplane configuration as *Figure 9*. Waveform B1 results from the same 2 drivers releasing the line simultaneously as Waveform B slot 0 in *Figure 9*. The lower signal amplitude is due to probing directly at the receiver input pin rather than the backplane solder point as in *Figure 9*. R1 and FR1 are the waveforms from DS3884A, channel 1, for the receiver and filtered receiver outputs respectively. PS1 and PS2 are both set to 0V to obtain a glitch rejection of 5 ns and less. Waveform FR1 clearly rejects the false triggering of the glitch, which is about 3 ns wide at the 1.5V receiver threshold. *Figure 11* shows the propagation delays for B1 to R1 and FR1 for both the high to low and low to high transitions at the 5 ns glitch rejection setting. The t_{PHL} is extended from 5 ns to 10 ns for the filtered output. The ringing on the receiver output signals results from wire wrap board frequency response limits.

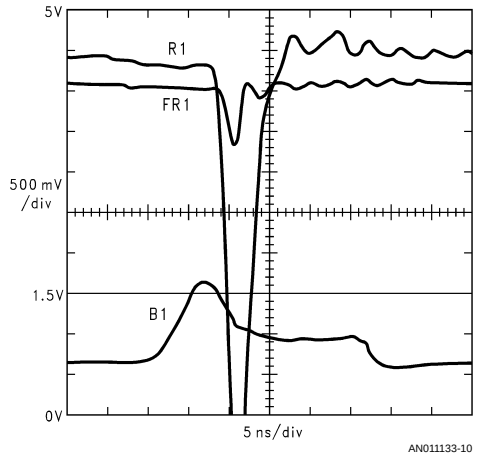

FIGURE 10.

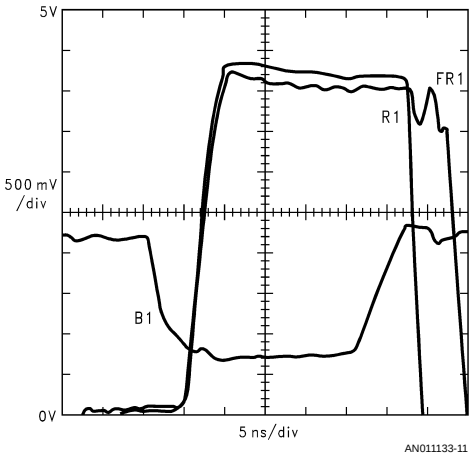

FIGURE 11.

The wired-OR glitch is inherent in wired-OR busses and will exist in a high speed transmission line environment. However, it is comforting to know that it is a well understood phenomena and there are ways of maintaining signal integrity through the use of filters.

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