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External Lead Finish for Plastic Packages

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External Lead Finish for Plastic Packages

For plastic packages, National Semiconductor offers two primary lead finishes: solder plate and solder dip. The component lead finish serves as a protective coating to prevent oxidation of the lead base material prior to use. The lead finish will ensure the leads are solderable for board mount applications as well as provide long term protection against lead corrosion. The lead finish composition and thickness is dependent on the package type and the applications in which the package is used.

SOLDER PLATE

For National's plastic packages, the most common lead finish is electroplated solder. Solder plating provides a uniform coating conforming to the shape of the lead. A tin-lead alloy plating is used and the typical composition is approximately 85% tin and 15% lead. A plating thickness of 200 microinches minimum is required.

SOLDER DIP

A solder dip lead finish is applied to plastic pin grid array packages (PPGA) and selected molded dual in-line packages (MDIP). Typical solder dip composition for application to MDIPs is a eutectic alloy of approximately 60% tin and 40% lead. The PPGA external lead finish is approximately 90% tin and 10% lead. A thickness of 200 microinches minimum is required and is measured at the major flat of the lead.

SOLDER BALL

Tin-lead eutectic solder balls with a composition of 63 tin and 37 lead are specified for array based packages (FBGA,EBGA,SBGA,PBGA) . Depending on the type of package , the solder ball diameters vary from 0.13 mm to 0.6 mm and the pitch varies from 0.5 to 1.27 mm with details specified in the relevant market outline drawings.

GOLD FLASH

The laminate based CSP packages are supplied with gold plated pads (0.5 micron nominal gold over 5 micron nickel) and meet the solderability requirements after 8 hr steam ageing.

For either lead finish, the cleaning and plating or dipping process is designed such that the component meets solderability requirements after 8 hours steam aging.

The following table is provided as a reference to determine which lead finish is used for each plastic package type offered at National Semiconductor.

Lead Finish for Plastic Packages

Package Type (Code)	Package Designator	External Lead Finish
Small Outline Transistor (SOT)	M; MA	Solder Plate
Small Outline Package — EIAJ and JEDEC (SOP)	M; MA	Solder Plate
Shrink Small Outline Package — EIAJ and JEDEC (SSOP)	ME; MQ; MS	Solder Plate
Very Small Outline Package (VSOP)	M; MA	Solder Plate
Thin Small Outline Package (TSOP)	MB	Solder Plate
Thin Shrink Small Outline Package (TSSOP)	MT	Solder Plate
Molded Dual-In-Line Package (MDIP)	N; NA	Solder Plate or Solder Dip
Plastic Pin Grid Array (PPGA)	UP	Solder Dip
Plastic Leaded Chip Carrier (PLCC)	V; VA	Solder Plate
Plastic Quad Flat Pack (PQFP)	V (xx)	Solder Plate
Plastic Transistor Outline Package (TO)	C; P; PA; R; RA; RC; T; TA; TS; Z	Solder Plate
Laminated Plastic Chip Scale Package (CSP)	SLB	Gold Flash
Laminated Plastic Fine Pitch Ball Grid Array (FBGA)	SLC	Solder Ball
Enhanced Ball Grid Array (EBGA)	UCK	Solder Ball
Super Ball Grid Array (SBGA)	UBC; UCC; UCD; UCG; UDB; UFD	Solder Ball

Lead Finish for Plastic Packages (Continued)

Package Type (Code)	Package Designator	External Lead Finish
Plastic Ball Grid Array (PBGA)	UBA; UBB; UBD; UBE; UCB; UCE; UDA; UDC; UDD; UEA; UFA; UFB; UFC	Solder Ball
micro-SMD	BPA	Solder Ball

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265