OBSOLETE

Application Report

SNOA366B–January 1993–Revised April 2013

OA-13 Current Feedback Loop Gain Analysis and Performance Enhancement

ABSTRACT

With the introduction of commercially available amplifiers using the current feedback topology by Comlinear Corporation in the early 1980's, previously unattainable gain and bandwidths in a DC coupled amplifier became easily available to any design engineer. The basic achievement realized by the current feedback topology is to de-couple the signal gain from the loop gain part of the overall transfer function. Commonly available voltage feedback amplifiers offer a signal gain expression that appears identically in the loop gain expression, yielding a tight coupling between the desired gain and the resulting bandwidth. This historically has led to the gain-bandwidth product idea for voltage feedback amplifiers. The current feedback topology transcends this limitation to offer a signal bandwidth that is largely independent of gain. This application report develops the current feedback transfer function with an eye towards manipulating the loop gain.

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3 Comlinear Hybrid, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information 13

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1 Current Feedback Amplifier Transfer Function Development

The equivalent amplifier circuit of Figure 1 is used to develop the non-inverting transfer function for the current feedback topology. The current feedback topology is also perfectly suitable for inverting mode operation, especially inverting summing applications. The non-inverting transfer function will be developed, in preference to the inverting, since the inverting transfer function development is a subset of the non-inverting.

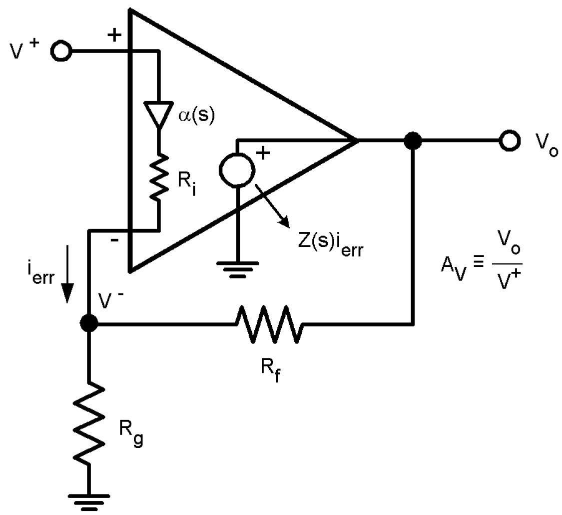

Figure 1. Current Feedback Amplifier Internal Elements

The amplifier's non-inverting input presents a high impedance to the input voltage, V^+, so as to not load the driving source. Any voltage appearing at the input node is passed through an open loop, unity gain, buffer that has a frequency dependent gain, α(s). α(s) is very neatly equal to 1 at DC (typically, .996 or higher, but always < 1.00) and typically has a −3dB point beyond 500MHZ. The output of the buffer ideally presents a 0Ω output impedance at the inverting input, V^-. It actually shows a frequency dependent impedance, Z_i, that is relatively low at DC and increases inductively at high frequencies. For this development, we will only consider that Z_i is a small valued resistive impedance, R_i. The intent of the buffer is to simultaneously force the inverting node voltage to follow the non-inverting input voltage while also providing a low impedance path for an error current to flow. Any small signal error current flowing in the inverting node, i_{err}, is passed through the buffer to a high transimpedance gain stage and on to the output pin as voltage. This transimpedance gain, Z(s), senses i_{err} and generates an output voltage proportional to it. Z(s) has a very high DC value, a dominant low frequency pole, and higher order poles. When the loop is closed, the action of the feedback loop is to drive i_{err} to zero much like a voltage feedback amplifier will drive the delta voltage across its inputs to zero. Z(s) ideally transforms the error current into a 0Ω output impedance voltage source.

The following equations will step through the transfer function development including the effect of R_i. This analysis neglects the impact of a finite output impedance from Z(s) to the output, output loading interactions with that output impedance, and the effect of stray capacitance shunting R_g.

Start by summing current at the V^- node of Figure 1.

$$ierr + \frac{V_O - V^-}{R_f} = \frac{V^-}{R_g} \tag{1}$$

You will also know that:

$$V^- = \alpha(s)V^+ - i_{err}R_i$$

$$\text{and, } i_{err}\, Z(s) = Vo \text{ then, } i_{err} = \frac{V_O}{Z(s)} \tag{2}$$

Multiply Equation 1 through by R_f and isolate:

$$V^- R_f i_{err} + V_o = V^-(1 + R_f/F_g) \tag{3}$$

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Now, substitute in for i_{err} and V^- from above:

$$\frac{R_f V_o}{Z(s)} + V_o = \left(\alpha(s)V^+ - \frac{R_i V_o}{Z(s)}\right)\left(1 + \frac{R_f}{R_g}\right) \tag{4}$$

Gather Vo terms and solve for V_o/v^+:

$$\frac{V_o}{V^+} = \frac{\alpha(s)\left(1 + \frac{R_f}{R_g}\right)}{1 + \frac{R_f + R_i\left(1 + R_f / R_g\right)}{Z(s)}} \tag{5}$$

It is instructive to consider the separate part of Equation 2 separately.

α(S.) → Frequency dependent buffer gain. Normally consider = 1

$1 + R_f/R_g$ → Desired signal gain. Identical to voltage feedback non-inverting amplifier gain.

$$\frac{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}{Z(s)} = \frac{1}{\text{Loop Gain}}$$

$$\text{Hence, Loop Gain (LG)} = \frac{Z(s)}{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}$$

$$= \frac{\text{internal forward transimpedance}}{\text{feedback transimpedance}} \tag{6}$$

The loop gain expression is of particular interest here. If Z(s), the forward transimpedance, is much greater than $R_f + R_i\ (1 + R_f/\ R_g)$, the feedback transimpedance, (as it is at low frequencies) then this term goes to zero leaving just the numerator terms for the low frequency transfer function. As frequency increases, Z(s) rolls off to eventually equal the feedback transimpedance expression. Beyond this point, at higher frequencies, this term increases in value rolling off the overall closed loop response.

The key thing to note is that the elements external to the amplifier that determine the loop gain, and hence the closed loop frequency response, do not exactly equal the desired signal gain expression in the transfer function numerator. **The desired signal gain expression has been de-coupled from the feedback expression in the loop gain.**

If the inverting input impedance were zero, the loop gain would depend externally only on the feedback resistor value. Even with small R_i, the feedback resistor dominantly sets the loop gain and every current feedback amplifier has a recommended R_t for which Z(s) has been optimized. As the desired signal gain becomes very high, the $R_i(1 + R_f/R_g)$ term in the feedback transimpedance can come to dominate, pushing the amplifier back into a gain bandwidth type operation.

2 Understand the Loop Gain

It is very useful, and commonly done for voltage feedback amplifiers, to look at the gain graphically. Figure 2 shows this for the CLC400, a low gain part offering DC to 200MHz performance. What has been graphed is 20*log(|Z(s)|), the forward transimpedance gain, along with its phase, and 20 log(Z_t). **This Z, is the feedback transimpedance, $R_f + R_i(1 + R_f/R_g)$, and where it crosses the forward transimpedance curve is the frequency at which the loop gain has dropped to 1.** Note that the forward transimpedance phase starts out with a 180° phase shift, indicating a signal inversion through the part, and could have plotted as continuing to 360° or, shown, going to zero. Using these axis allows a direct reading of the phase margin at unity gain crossover.

As with any negative feedback amplifier, the key determinant of the closed loop frequency response is the phase margin at unity gain crossover. If the phase has shifted completely around to 360°, or dropped to zero on the axis used above when the loop gain has decreased to 1, unity gain crossover - (where the 20 log(Z_t) line intersects the 20 log(|Z(s)|) curve), the denominator in closed loop expression will become (1-1), or infinity. (For the axis used above, the closed loop expression (Equation 2) would have a 1-1/LG in the denominator. The form developed as Equation 2 accounted for the inversion with the sign convention for i_{err} and V_o).

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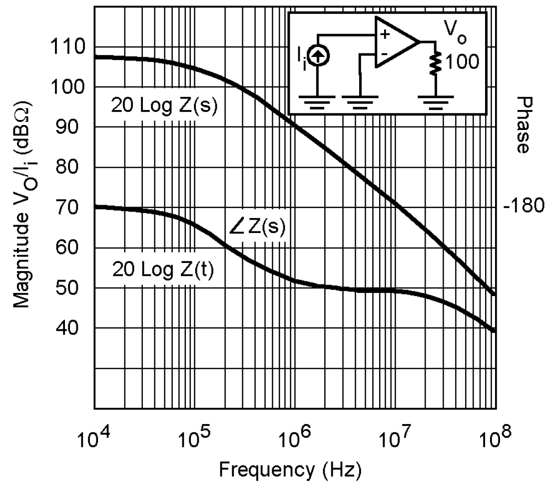

Figure 2. Feedback Transimpedance

It is critical for stable amplifier operation to maintain adequate phase margin at the unity gain crossover frequency. The feedback transimpedance that is plotted in Figure 2 is $R_t + R(1 + R_f/R_g)$ evaluated at the specifications setup point for the CLC400. This yields:

$$\begin{array}{ll} R_f = 250\Omega & \text{then} \\ A_v \equiv 1 + (R_f/R_g) = 2 & Z_i = 250\Omega + 500\Omega(2) = 350\Omega \\ & \text{and} \\ Z_i = 50\Omega & 20\log(350\Omega) = 50.9\text{dB} \end{array} \tag{7}$$

Looking at the unity gain crossover near 100MHz, you see somewhere in the neighborhood of a 60° phase margin. This is Comlinear's targeted phase margin at the gain and R_f used to specify any particular current feedback part. This phase margin, for simple 2 pole Z(s), yields a maximally flat Butterworth filter shape for the closed loop amplifier response (Q = .707). Note that the design targets reasonable flatness over a wide range of process tolerances and temperatures. This typically yields a nominal part that is somewhat overcompensated (phase margin > 60°) at room temperature.

Note that the closed loop bandwidth will only equal the open loop unity gain crossover frequency for 90° phase margins (single pole forward gain response). As the open loop phase margin decreases from 90°, with the impact of higher frequency poles in the forward transimpedance gain, the closed loop poles move off the negative real axis (in the s-plane) peaking the response up and extending the bandwidth. The actual bandwidth achieved by Comlinear's amplifiers is considerably beyond the unity gain crossover frequency due to these open loop phase effects.

3 Controlling the Loop Gain

One of the key insights provided by the loop gain plot is what happens when Z_t is changed. Decreasing Z_t (dropping the horizontal line of 20 log (Z_t)), will extend the unity gain crossover frequency but will sacrifice phase margin. This commonly seen in current feedback amplifiers when an erroneously low R_f value is used yielding an extremely peaked frequency response. In fact a very reliable oscillator can be generated with any current feedback amplifier by using R_f = 0 in a unity gain configuration. Conversely, increasing Z_t (raising the horizontal line of 20 log(Z_t)) will drop the unity gain crossover frequency and increase phase margin. Increasing R_f is in fact a very effective means of over compensating a current feedback amplifier. Increasing R_f will decrease the closed loop bandwidth and/or decrease peaking in the frequency response.

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4 Computing Z_t for the Design Point

Computing Z_t for the Design Point used in setting the specifications for any particular current feedback part indicates an optimum targeted feedback transimpedance under any condition.

In design, the internal Z(s) has been set up to yield a maximally flat closed loop response with the gain and R_f used to develop the performance specifications. if we then try to hold the same feedback transimpedance under different gain conditions, an option not possible with voltage feedback topologies, this optimum unity gain crossover for the open loop response can be maintained.

If we designate this optimum feedback transimpedance as Z_t*,

You would like to hold $R_f + R_i (1 + R_f/R_g) = Z_t^*$

where, R_f and $1 + R_f/R_g$ are those values shown at the top of the part performance specification.

Substituting $A_v = 1 + R_f/R_g$, you get:

$$R_f = Z_t^* - R_i A_v \quad (8)$$

where, R_f is a new value to be used at a gain other than the design point.

This is a design equation for holding optimum unity gain crossover. Having computed R_f to hold:

$$Z_t = Z_t^* R_g/R_f/(A_v - 1) \quad (9)$$

5 The Benefits of Controlling Z_t

As an example of adjusting R_f to hold a constant Z_t as the desired signal gain is changed, consider a CLC404 at gains of +2, +6 and +11.Figure 3 shows test results over these gains for a fixed R_f very similar to low the *CLC404 Wideband, High Slew Rate, Monolithic Op Amp Data Sheet* (SNOS851) plots were generated.

Using the CLC404 design and specifications points, see Appendix A.

$A_v = +6$

$R_f = 500\Omega$

$R_i = 30\Omega$

$Z_t^* = 500 + 30*6 = 680\Omega$

Figure 4 shows the same part operated with R_f adjusted as indicated by Equation 8. R_g in both cases is set using Equation 9.

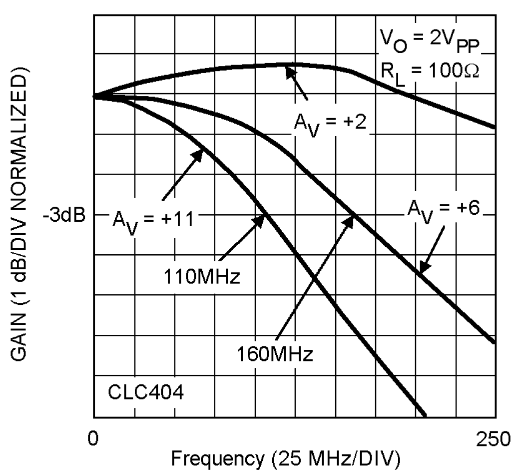

Figure 3. Frequency Response vs. Gain for R_f Fixed = 500Ω

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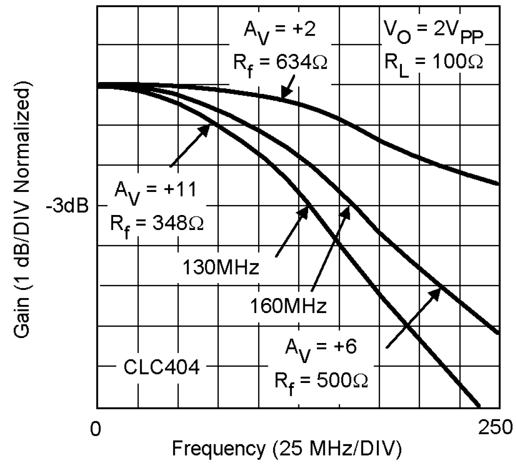
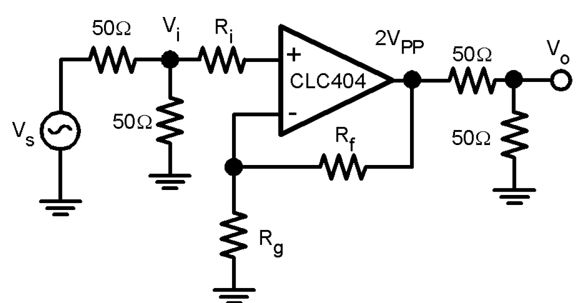


Figure 4. Frequency Response vs. Gain for Fixed $Z_t = Z_t^* = 680\Omega$

The results of Figure 4 vs. Figure 3 show that adjusting R_f does indeed hold a more constant frequency response over gain than a simple fixed R_f. The low gain response has flattened out while the high gain response has been extended.

The remaining variability in frequency response can be attributed to second order effects that have not yet been considered. As described in *OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers* (SNOA367), parasitic capacitance shunting the gain setting resistor, R_g, introduces a response zero for non-inverting gain operation. This zero location can be easily located by substitution $R_g||C_g$ into the numerator part of the transfer function, Equation 2. This yields a zero at $1/(R_f||R_g)/C_g$ in radians. This effect would not be observed in inverting mode operation yielding a much more consistent response over gains, especially with R_f adjusted as shown above.

If you assume equal parasitic capacitances on the two inputs, you can cancel this zero by introducing a series impedance into the non-inverting input that equals $R_f||R_g$. Figure 5 shows the test circuit and table of values used to test this for the same CLC404 used above. Note that you must include the equivalent source impedance of the source matching and termination resistors in (25Ω here). Note that the table shows actual standard values used, rather than the exact calculated values.



$R_f = 680 - A_V(30)$
$R_g = R_f / (A_V - 1)$
$R_i = (R_f || R_g) - 25\Omega$

A_V	R_f	R_g	R_i
+2	634	634	287
+6	500	100	56.2
+11	348	34	6

Figure 5. Test Circuit and Table of Values

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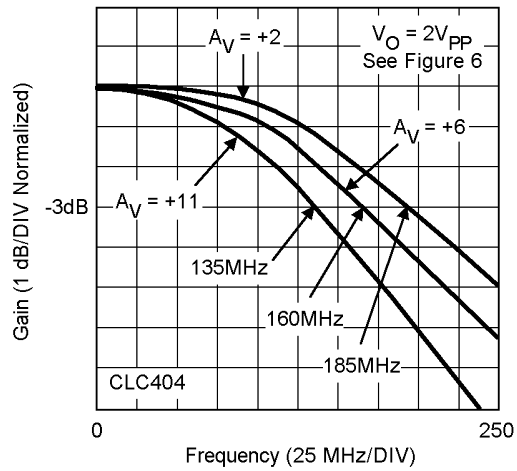

Figure 6. Frequency Response

Figure 6 shows the measured frequency responses under the conditions tabulated in Figure 5.

Clearly, adding R_i has brought the low gain response to be much more consistent with the higher gains. Little effect was observed by adding R_i at gains of 6 and 11. Generally, adding R_i is particularly effective at flattening out the frequency response for higher gain parts, which are designed using high value of feedback resistors, when they are operated at low gains.

An alternative to adding R_i is simply to continue to increase R_f until the loop gain is overcompensated enough to cancel the zero. This is increasingly ineffective as the resistor values get larger but was developed empirically for the CLC414 and CLC415 quad amplifiers. For details, see the device-specific data sheet. An alternative approach with those parts would be to adjust R_f using the data from Appendix A and then add an R as described above.

Note that Equation 3 will predict negative R_f values as the desired gain exceeds Z_t^*/R_i. From a loop gain standpoint, this is exactly correct. However, additional concerns (particularly distortion and output current limits) will come in to limit the applicable range of gains for Equation 3. Generally, the total loading on the amplifiers should not be allowed to drop below 65Ω. This is the actual load in parallel with $R_f + R_g$ for the non-inverting configuration. For a 100Ω load, this limits the minimum $R_f + R_g$ to about 200Ω. Lower values can be used if R_L is greater. For inverting mode, which has exactly the same loop gain expression as non-inverting, R_f alone appears in parallel with R_L as an additional load. This would limit R_f to a minimum of 200Ω in inverting mode operation. This does not, of course, limit the amplifier's maximum gain. When a minimum R_f has been reached, R_g can continue to decrease, yielding higher gains, with a gain bandwidth characteristic eventually developing as the R_i $(1 + R_f/R_g)$ part of Z_t comes to dominate.

6 Special Considerations for Variable Supply Current

The inverting input impedance, R_i, is essentially the output impedance of parallel/series combinations of emitter followers for most Comlinear amplifiers. Thus, R_i is some fraction or integer multiple of V_t/I_c, where $V_t = kT/q$ and I_c is the bias current in those transistors. For lower power parts, and parts with adjustable supply current, R_i can get very large, as I_c decreases quickly putting the parts into a gain bandwidth type operation. Appendix A shows the nominal design point I_c, along with a room temperature R_i, and, for the adjustable supply current, I_{cc}. Anything that adjusts the total quiescent supply current from its nominal design point, changing power supply voltage, using the bias adjust pins on some parts, and so forth will scale the I_c listed in Appendix A in direct proportion to I_{cc}.

7 Additional Loop Gain Control Applications

Recognizing that the inverting input impedance provides an opportunity to adjust the loop gain, without having any impact on the signal gain, we can add a resistor inside the loop that can act as an independent frequency response compensation element. This is very useful if a fine control over the frequency response shape is desired.

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Using the same CLC404 used in the earlier tests (a part that is nominally overcompensated as shown by the rolloff at its gain of +6 condition in Figure 3), the circuit of Figure 7 show an adjustment technique for the frequency response. Since we are intentionally adding R_i to the feedback transimpedance expression, Z_t, it is recommended to approximately set R_f to yield Z_t* when the adjustment to R_i is at midrange. This will yield a lower R_f as shown inFigure 7. Figure 8 shows the original gain of +6 response of Figure 3, along with the response achieved with the circuit of Figure 7 with R_p adjusted to yielded maximally flat frequency response. This circuit shows a ±.1dB gain flatness to beyond 100MHz.

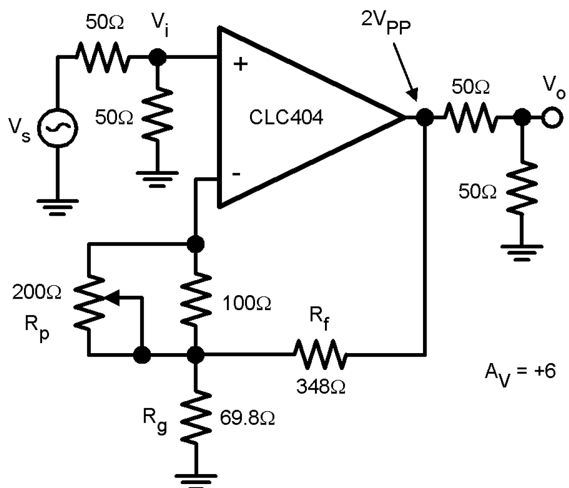

Figure 7. Adjustable Frequency Response

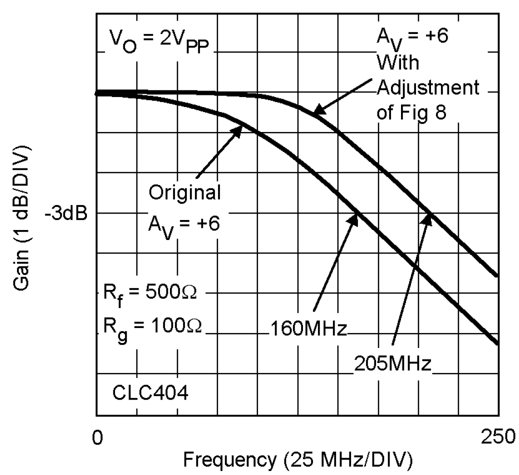

Figure 8. Frequency Response With Loop Gain Response

In inverting applications there is often times a conflict between the required gain setting resistors from an input impedance and signal gain standpoint, and what the amplifier would like to see from a loop gain phase margin standpoint. In a similar fashion to voltage feedback, in this case, an additional resistor to ground on the inverting input can be used to tune the loop gain independently of the inverting signal gain requirements. The drawback of this, is that, like voltage feedback, this increases the noise gain for the non-inverting input voltage noise.

Figure 9 shows an example of a transimpedance application using a CLC401 with a 1kΩ feedback resistor. In this case, the value of the feedback resistor is set by the desired signal gain, while R_g is used to satisfy the loop gain phase margin by setting the feedback transimpedance to Z* = 2.5k.

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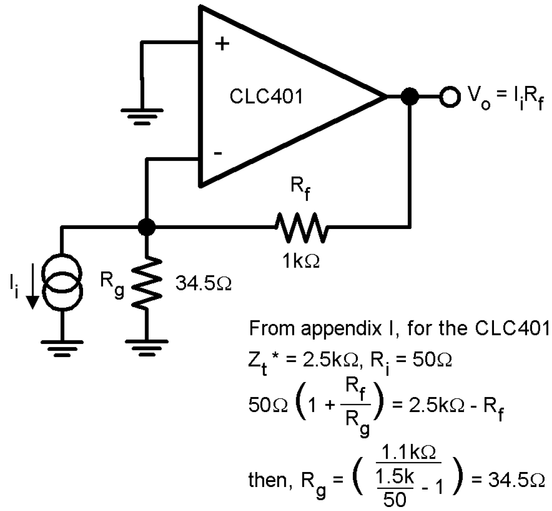

Figure 9. Transimpedance Application

Similarly, in an inverting summing application, once the desired gain and input impedance conditions are set, the loop gain can be independently controlled through the use of an additional resistor to ground on the inverting input. Figure 10 shows an example of this using the CLC401 summing 5 channels, at a gain of −1 for each channel, using 1kΩ input resistors.

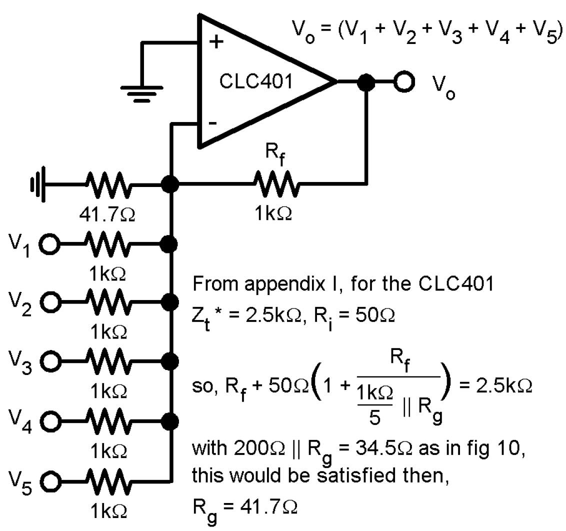

Figure 10. Loop Gain Adjusted in Inverting Summing Application

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8 Conclusions

The current feedback topology has allowed us to de-couple the signal gain from the loop gain expressions. This provides ample opportunity for independent control of both the signal gains and the frequency response by using only resistive elements. A thorough understanding of the loop gain mechanisms provides the designer with a flexibility unavailable to the voltage feedback op amp.

9 References

- *CLC to LMH Conversion Table* (SNOA428)
- *CLC404 Wideband, High Slew Rate, Monolithic Op Amp Data Sheet* (SNOS851)
- OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers (SNOA367)

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Appendix A Comlinear Linear Tables

The data tabulated here provide the necessary information to hold a constant feedback transimpedance over a wide range of closed loop signals gains for the current feedback amplifiers available from Comlinear at the time of this application reports publication. The data is broken into a set for the monolithic amplifiers, which generally have a higher R_i due to their lower quiescent bias current, and a set of data for the hybrid amplifier products.

Table 1. The Table Entries Show

1.	A_v ≥ Non-inverting voltage gain used to set device specs.
2.	R_f ≥ Feedback resistor value used to set the device specs.
3.	R_i ≥ Nominal inverting input impedance

These three items are used to compute the optimum feedback transimpedance for the particular part. This is given by

$$Z_t^* = R_f + RA_v \tag{10}$$

This information is used to compute a more optimum R_f as the desired closed loop gain moves away from the design point A_v.

It is important to note that, given any feedback R_f and any closed loop non-inverting signal gain, a feedback transimpedance can be computed using the equation for $Z_t = R_f + R_iA_v$. Z_t^* is the optimum value for open loop phase margin and closed loop response flatness found by evaluating the expression at the specific R_f and gain used in designing and specifying the part.

I_c ≥ Approximate collector current for the emmitter followers seen looking into the inverting input. The inverting inputs do not necessarily present an integer number of series/parallel emmitter followers. The approximate scale factors can be computed by solving for n in the following expression.

$$R_i = n\ V_t/I_c \text{ with } V_t = kT/q \text{ (=26mV at room temperature)} \tag{11}$$

I_c/I_{cc} ≥ Ratio of inverting input stage bias current to the total device quiescent current. With n determined from above, the adjusted value for R_i may be determined for a part that is being operated at a different quiescent current than is normally specified.

The data presented here represent a good approximation to the device characteristics. Several second order effects have been neglected for the sake of simplicity.

The CLC505, an adjustable supply current op amp, was optimized at 9mA supply current. No attempt was made in this table, or in the data sheet, to reset the optimum R_g as the supply current is decreased. At very low supply current, the CLC505's inverting input impedance dominates the feedback transimpedance expression. To compensate for this with a reduce R_f, as has been suggested in this document, would require such low values as to excessively load the limited output drive current available. The CLC505 at 1mA supply current shows a gain bandwidth product performance due to the dominance of R_i in the loop gain equation.

NOTE: The circuits included in this application report have been tested with Texas Instruments parts that may have been obsoleted and/or replaced with newer products. To find the appropriate replacement part for the obsolete device, see the *CLC to LMH Conversion Table* (SNOA428).

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Table 2. Comlinear Monolithic, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information[(1)(2)]

Part No	Design Point Information				Operating Current		Comments
	A_v	R_f (Ω)	R_i (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC400	+2	250	40	330	.67	.045	
CLC401	+20	1500	50	2500	.52	.035	
CLC402	+2	250	16	282	.82	.055	
CLC404	+6	500	30	680	.87	.080	
CLC406	+6	500	60	860	.43	.09	
CLC409	+2	250	25	300	1.05	.08	
CLC410	+2	250	35	320	.74	.05	disable left open
CLC411	+2	301	50	400	.52	.05	disable left open
CLC414	+6	500	250	2000	.105	.05	each amplifier of quad
CLC415	+6	500	60	860	.43	.09	each amplifier of quad
CLC430	+2	750	60	870	.43	.04	disable left open
CLC500	+2	250	32	314	.82	.05	
CLC501	+20	1500	30	2100	.86	.05	see [(3)]
CLC505	+6	1000	50	1300	.52	.06	I_{cc} = 9.0mA R_p = 33kΩ
CLC505	+6	1000	150	1900	.175	.06	I_{cc} = 3.3mA R_p = 33kΩ
CLC505	+6	1000	490	3950	.053	.06	I_{cc} = 1.0mA R_p = 33kΩ

(1) Power supplies at ±5V
(2) 25°C temperature assumed: yields kT/q = .26V
(3) CLC501 specification point at A_v = +32, R_f = 1500Ω Design point, however is at A_v = +20, R_f = 1500Ω

Table 3. Comlinear Hybrid, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information [(1)(2)]

Part No	Design Point Information				Operating Current		Comments
	A_v	R_f (Ω)	R_i (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC103	20	1500	8.5	1670	1.57	.054	Fixed internal R_f. See [(3)]
CLC203	20	1500	11.8	1736	2.21	.072	Fixed internal R_f. See [(3)]
CLC200	20	2000	8.5	2170	1.54	.053	See [(4)]
CLC201	20	2000	17	2340	1.54	.053	See [(4)]
CLC205	20	2000	23Ω	2460	.74	.037	see [(5)]
CLC206	20	2000	15Ω	2300	1.10	.038	see [(5)]
CLC207	20	2000	23Ω	2460	.74	.030	see [(5)]
CLC220	20	1500	8.5	1670	1.54	.053	see [(4)]
CLC221	20	1500	17	1840	1.54	.053	see [(4)]
CLC231	2	250	15	280	1.78	.093	
CLC232	2	250	15	280	1.78	.071	
CLC300A	20	1500	7.5	1650	1.73	0.70	see [(4)]

(1) Power supplies at ±15V
(2) 25°C temperature assumed; yields kT/q = .26V
(3) CLC103 & CLC203 have fixed internal R_f. Cannot, therefore increase the R_f value or insert additional R_i for loop gain control.
(4) These parts include an optional internal feedback resistor that may or may not be used in applying the part. Not using this internal R_f allows adjusting the R_f over gain and/or inserting additional R_i.
(5) CLC205, CLC206, & CLC207 use a small shunting capacitance across the internal R_f to extend the bandwidth. Using a standard RN55D external R_f, with lower shunt capacitance, will require a large nominal design point value for Z_t* to hold optimum loop gain. At A_v = +20, an external R_f = 2.74kΩ yields the desired Z_t.

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