Application Report
SNOA475E–November 2006–Revised May 2020

AN-1516 Pspice Universal Test Circuits

SOUFANE BENDAOUD

ABSTRACT
This application report provides a collection of circuits that allow users to test any op amp model, in a way somewhat universal test circuits for op amp macro models.

Contents
1 Introduction ................................................................................................................... 3
2 What Parameters Should Be Tested? ............................................................................ 3
  2.1 Open-Loop Gain and Phase Margin ............................................................................ 3
  2.2 Slew Rate .................................................................................................................. 5
  2.3 CMRR and PSRR .................................................................................................... 6
  2.4 Closed-Loop Output Impedance .............................................................................. 7
  2.5 Voltage and Current Noise ..................................................................................... 10
  2.6 Input Bias Current and Input Offset Voltage ............................................................ 12
  2.7 Output Saturation Voltage ..................................................................................... 12
  2.8 Supply Current vs Supply Voltage ......................................................................... 14
  2.9 Overshoot and Transient Response ........................................................................ 15
  2.10 Common-Mode Voltage Range ............................................................................. 16
  2.11 Phase Reversal ..................................................................................................... 18
3 Conclusion .................................................................................................................. 18

List of Figures
1 Open-Loop Gain and Phase Test Circuit ................................................................. 4
2 Simulated Open-Loop Gain and Phase ..................................................................... 4
3 Measured Open-Loop Gain and Phase ...................................................................... 4
4 Slew Rate Test Circuit ............................................................................................. 5
5 Simulated Slew Rate ................................................................................................. 5
6 CMRR Test Circuit .................................................................................................. 6
7 Simulated CMRR Response vs Frequency ............................................................... 6
8 Measured CMRR vs Frequency ............................................................................... 6
9 PSRR Test Circuit ..................................................................................................... 7
10 Simulated PSRR Response vs Frequency ............................................................... 7
11 Measured PSRR vs Frequency ................................................................................ 7
12 Output Impedance Test Circuits for a Gain of 1, 10, and 100 .................................... 8
13 Simulated Closed-Loop Output Impedance ............................................................ 9
14 Voltage Noise Density Test Circuit ........................................................................ 10
15 Simulated Voltage Noise Density ........................................................................... 10
16 Current Noise Density Test Circuit ......................................................................... 11
17 Simulated Current Noise Density ........................................................................... 11
18 Offset Voltage and Input Bias Current .................................................................... 12
19 Output Saturation Voltage vs Load Current Test Circuit ....................................... 13
20 Simulated Output Saturation Voltage .................................................................... 13
<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>Supply Current vs Supply Voltage</td>
<td>14</td>
</tr>
<tr>
<td>22</td>
<td>Simulated Supply Current vs Supply Voltage</td>
<td>14</td>
</tr>
<tr>
<td>23</td>
<td>Overshoot Test Circuit</td>
<td>15</td>
</tr>
<tr>
<td>24</td>
<td>Simulated Overshoot</td>
<td>15</td>
</tr>
<tr>
<td>25</td>
<td>CMVR Test Circuit</td>
<td>16</td>
</tr>
<tr>
<td>26</td>
<td>Simulated CMVR</td>
<td>16</td>
</tr>
<tr>
<td>27</td>
<td>CMVR Test Circuit (Optional)</td>
<td>17</td>
</tr>
<tr>
<td>28</td>
<td>Simulated CMVR</td>
<td>17</td>
</tr>
<tr>
<td>29</td>
<td>No Phase Reversal Test Circuit</td>
<td>18</td>
</tr>
<tr>
<td>30</td>
<td>No Phase Reversal</td>
<td>18</td>
</tr>
</tbody>
</table>

**Trademarks**

All trademarks are the property of their respective owners.
1 Introduction

There is no doubt that Spice models have gained a lot of popularity over the past years. While IC manufacturers strive to provide their customers with accurate models, the system designer is really who dictates the trend of this accuracy and innovation in the development of Spice macro models.

Many IC companies praise and brag about how their models are the best or offer revolutionary features. But what these companies often fail to provide is some sort of circuit that allows the user to verify the accuracy of the macro model. Op amps macro models are probably the most sought after; while extremely helpful when accurate, these macro models can also cause serious problems, especially when not in the hands of experts.

Most system design engineers take the time to test the op amp macro model individually, before implementing the macro model in a more comprehensive circuit. Unfortunately, sometimes the use of inaccurate models leads designers and users to think that the amplifier is faulty, when the actual problem lies either in the model, or in not properly setting the SPICE test environment. The truth is, all models are not the same, and some may not work in a particular setting.

2 What Parameters Should Be Tested?

Macro models differ in the level of complexity. Much like data sheets, the models should emulate parameters that are relevant to applications in which the op amp is thought to be appropriate. For example, if a rail-to-rail output op amp is used, then the user should be able to test and verify the output saturation voltage versus the load current. Likewise, a low-noise amplifier should have a model that emulates at least the voltage, noise among other modeled parameters.

Despite their differences, amplifier macro models have a lot in common; these parameters are of the greatest interest and they are usually the starting point of the simulation. The following sections list these parameters, along with the corresponding test circuits and simulations.

2.1 Open-Loop Gain and Phase Margin

Open-loop gain versus frequency is probably the very first test that engineers perform to evaluate an amplifier macro-model performance. This test is important because the results show the dc gain, the ~3-dB frequency, the unity gain bandwidth, and the phase margin. Figure 1 shows the test circuit. The RC network makes sure that the output is biased at an acceptable dc voltage, (mid-rail in this case). At higher frequencies, the capacitor shorts the inverting input to ground, which in turn places the op amp in an open loop. The capacitor is chosen to be large to provide an early roll off \( f = 1/2\pi R_1 C_2 \) so that even if the op amp tested has a very low frequency dominant pole, the simulation shows a smooth transition and a 20 dB per decade roll off.

When testing open-loop gain and phase, choose an upper frequency limit that goes beyond the unity-gain bandwidth of the amplifier.

When using rail-to-rail output models, use the test circuit with the same load indicated in the data sheet. Otherwise, the result might not reflect the actual amplifier capabilities; especially true about the dc gain \( A_{\text{dc}} = g_m R_L \).
Figure 1. Open-Loop Gain and Phase Test Circuit

Figure 2. Simulated Open-Loop Gain and Phase

Figure 3. Measured Open-Loop Gain and Phase
2.2 Slew Rate

Slew rate is another element that defines the amplifier speed and is frequently modeled. Slew rate is usually determined by the ratio of the tail current and the compensation capacitance (I/C).

We already know the relationship \( I \times dt = C \times dv \); therefore, simply use the circuit in Figure 4 and take the derivative of the output to get the slew rate. Use the insert command in the probe screen of Pspice to add the letter “d” preceding the output voltage probe.

To make sure this test circuit works properly, make sure the input step function has an amplitude large enough so that the effects of slew rate limitation are visible. When running the simulation for slew rate, make sure the input signal rise and fall times are shorter than the amplifier expected slew rate. This procedure is to make sure that the test results are dominated by the amplifier slew rate. On the other hand, choose the input signal frequency accordingly with the op amp speed. An input signal that is too fast causes convergence problems.

![Figure 4. Slew Rate Test Circuit](image)

![Figure 5. Simulated Slew Rate](image)
2.3 CMRR and PSRR

These two parameters are not always modeled, but can be equally important. CMRR and PSRR are fairly easy to implement in a model because they usually consist of a simple RC network, a resistor divider, and a voltage-controlled voltage source.

CMRR is especially important in noninverting configurations because of the modulation of the noninverting input with the input signal. PSRR on the other hand is important in any application where the voltage supply is susceptible to any interference, or for dc PSRR where the supplies can experience significant variation.

The test circuits presented in Figure 6 and Figure 9 allow the user to simulate these two parameters. If they are modeled correctly, the pole and zero location should match the graphs in the data sheet.

Figure 6. CMRR Test Circuit

Figure 7. Simulated CMRR Response vs Frequency

Figure 8. Measured CMRR vs Frequency
2.4 Closed-Loop Output Impedance

Closed-loop output impedance is a specification that is often omitted from the data sheets altogether, but is sometimes needed.

When modeled correctly, the output impedance helps get a more accurate settling time behavior under various capacitive loads.

The output impedance is also needed to calculate the proper component values when a compensation scheme is considered for stability purposes.

The test circuits of Figure 12 provide the user with three curves for the output impedance versus frequency at different gains: 1, 10, and 100. The output impedance is obtained by taking the ratio of the output voltage over the current (1-A source at the output of the amplifier).

The graph in Figure 13 shows the closed-loop output impedance of the LMV791. At higher frequencies (where the curves flatten), the value is approximately 120 Ω. Make sure to plot the curves on a log-log scale.
Figure 12. Output Impedance Test Circuits for a Gain of 1, 10, and 100
Figure 13. Simulated Closed-Loop Output Impedance
2.5 Voltage and Current Noise

If there is an area where the creation of amplifier macro models has progressed, voltage and current noise is one of these areas. Some of today’s models allow users to simulate voltage noise with a flicker noise component and current noise with excellent accuracy. Modeling noise into the macro model does not take much more computing or simulation time, but is a somewhat difficult task; at least until the right equations are figured out to make the voltage noise density curve mimic the data sheet graph with the 1/f corner. The voltage noise density can easily be tested by taking the output of a voltage follower (with a voltage source of 0 V) on a log-log scale. To simulate the current noise density, the same circuit can be used with a 100-kΩ resistor placed in series with the noninverting terminal for bipolar op amps. For CMOS amplifiers, use a current-controlled voltage source in series with the noninverting terminal as shown in Figure 16.

![Figure 14. Voltage Noise Density Test Circuit](image)

![Figure 15. Simulated Voltage Noise Density](image)
Figure 16. Current Noise Density Test Circuit

Figure 17. Simulated Current Noise Density
2.6 **Input Bias Current and Input Offset Voltage**

The input bias current and input offset voltage parameters are probably the easiest to model. Input offset voltage can easily be implemented as a voltage-controlled voltage source at the input, with a value that is taken from the datasheet.

In general, no specific test circuit is needed for testing bias current or offset voltage. Any of the circuits already discussed in this document can be used. In order to view the values of offset voltage and bias current, activate the voltage and current labels in SPICE, as shown in Figure 18 where the input bias current is 1.5 pA and the input offset voltage is 1.48 mV.

![Figure 18. Offset Voltage and Input Bias Current](image)

2.7 **Output Saturation Voltage**

Output saturation voltage is also known as the dropout voltage. This parameter is particularly important in rail-to-rail output amplifier models because this parameter represents the output voltage swing as a function of the load current, and can help the system designer choose the appropriate op amp; especially, when driving heavy loads or when dynamic range is a concern.

The test circuit shown in Figure 19 uses a simple dc sweep with two equal input voltages of opposite magnitude to replicate the sourcing and sinking of the load current.
Figure 19. Output Saturation Voltage vs Load Current Test Circuit

Figure 20. Simulated Output Saturation Voltage
2.8 Supply Current vs Supply Voltage

The test circuit shown in Figure 21 sweeps the current across the supply, and determines how much current is drawn by the amplifier at different supply voltages. This test is particularly helpful for low-power applications. The slope of the supply current curve can easily be added into the model.

![Figure 21. Supply Current vs Supply Voltage](image1)

![Figure 22. Simulated Supply Current vs Supply Voltage](image2)
2.9 Overshoot and Transient Response

The test circuit shown in Figure 23 serves two purposes: testing the transient response (whether small signal or large signal), and the overshoot.

Overshoot is important because overshoot indicates how much ringing an amplifier has in the presence of a capacitive load. Overshoot is a measure of stability in time domain; the equivalent of what peaking is in the frequency domain.

Some macro models use extra passive components to mimic the overshoot accurately; but generally, if the phase margin is accurate, the overshoot should also be accurate.

The transient response can be tested using the test circuit used for the overshoot test, without the 100-pF capacitor. Some data sheets indicate whether a small capacitance is used as a load when measuring the small-signal transient. In that case, simply use the same value of capacitance.

![Figure 23. Overshoot Test Circuit](image)

![Figure 24. Simulated Overshoot](image)
2.10 Common-Mode Voltage Range

The common-mode voltage range is important because this parameter allows the user to see the head room, or how far away the input signal needs to be from the supply.

The first test circuit in Figure 25 uses a voltage-controlled voltage source. In the second test circuit, Figure 27, the voltage is swept from $-2.5 \text{ V}$ to $+2.5 \text{ V}$.

![Figure 25. CMVR Test Circuit](image)

![Figure 26. Simulated CMVR](image)
Figure 27. CMVR Test Circuit (Optional)

Figure 28. Simulated CMVR
2.11 Phase Reversal

Phase reversal occurs in some amplifiers when the input signal exceeds the input common-mode voltage range. During a phase reversal, the output changes polarity and may cause damage to the op amp resulting in system lockups.

The test circuit shown in Figure 29 is a simple voltage follower with a sine-wave input that goes beyond the common-mode voltage range of the amplifier; 6 V in this example. The output waveform shown in Figure 30 indicates that just like the op amp, the macro model does not exhibit any phase reversal; it is clipped at ±2.5 V.

![Figure 29. No Phase Reversal Test Circuit](image)

![Figure 30. No Phase Reversal](image)

3 Conclusion

The test circuits described in the previous sections are not meant to replace the evaluation of the device on the bench. Rather, these test circuits provide the user with the flexibility to make quick assessments with respect to the accuracy of the macro model.

Special thanks to the applications group and the design community at Texas Instruments for their thoughtful insights.
**Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>Changes from D Revision (April 2013) to E Revision</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed Figure 16; replaced with new figure</td>
<td>11</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated