

AN-1733 Load Transient Testing Simplified

ABSTRACT

The load transient test may be the simplest diagnostic tool available to instantly analyze the loop stability of a system: the visual appearance of the output voltage as the voltage regulator responds to a change in load current directly correlates to phase margin. This article will demonstrate how to easily perform load transient testing, and how to estimate phase margin based upon the results of this test.

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1 Introduction

The load transient test may be the simplest diagnostic tool available to instantly analyze the loop stability of a system: the visual appearance of the output voltage as the voltage regulator responds to a change in load current directly correlates to phase margin. This article will demonstrate how to easily perform load transient testing, and how to estimate phase margin based upon the results of this test.

2 Voltage Regulation

Virtually all electronic devices require a supply voltage that is held within a specified tolerance range, even when the load current varies. This fixed voltage is provided by a voltage regulator (Figure 1).

The output voltage is sensed through a resistive divider and the error amplifier adjusts the current source I_{REG} to hold the output at the nominal voltage.

The voltage regulator must be able to hold its output voltage constant as the load current demand varies anywhere from zero up to full load, even if the change occurs in a relatively short time: such sudden changes in load current are called **load transients**. How well a voltage regulator holds its output voltage constant during a load transient is defined as its **load transient response**.

It's fairly easy to hold the output voltage constant as long as the load current changes slowly. But, when the load current "steps" quickly enough, the output voltage will change. It is how much the output voltage changes when subjected to a change in load current that defines load transient performance.

Key principles in understanding load transients:

- 1) A voltage regulator acts as a voltage-controlled current source which drives current to the load (the current source is adjusted by voltage feedback from the output). The regulator's current source can never be changed in zero time, so it follows that if we make the load current change quickly enough, it will force the output voltage to change. How much it changes will be dependent on the speed of the regulator, amount and type of output capacitor, and the di/dt of the load current change.
- 2) During the time interval while the regulator's control loop is adjusting for the change in load, the only thing supplying the difference in load current between the former steady-state value and the new load current value is the output capacitor. So, output capacitors are essential to controlling the output voltage during load transients, and the electrical characteristics of these capacitors significantly affect transient response.
- 3) The faster the regulator's control loop can respond, the less the output capacitor's voltage will change before the loop corrects to the new value of load current. Therefore, it follows that a faster regulator can hold the same V_{OUT} tolerance range with less output capacitance (which can save money).

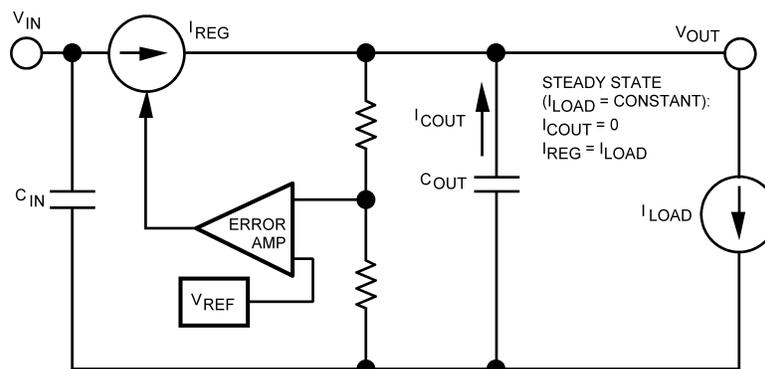


Figure 1. Basic Voltage Regulator Operation

3 Anatomy of a Load Transient

To see how a load transient works, we will analyze an example where the load current goes from I_{L1} to a higher value (I_{L2}) in essentially zero time (Figure 2).

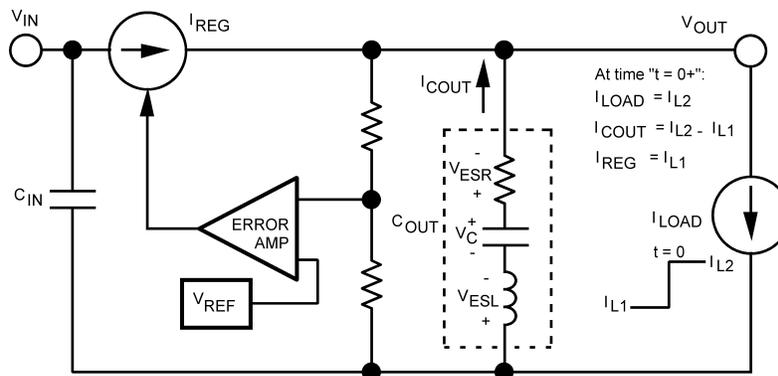


Figure 2. Regulator Responds To Change In Load Current

The regulator's current source (I_{REG}) can not change instantly, therefore at time "t = 0+" (the instant after the load increases to I_{L2}), $I_{REG} = I_{L1}$. By simple node analysis, it follows that the output capacitor is required to source:

$$I_{COUT} = I_{L2} - I_{L1} \tag{1}$$

C_{OUT} will continue to supply some of the load current until the control loop adjusts I_{REG} to the new value I_{L2} , causing the voltage across the capacitor to decrease as it discharges. The voltage across C_{OUT} is also reduced by the voltage drops across the capacitor's internal ESR (equivalent series resistance) and ESL (equivalent series inductance), which are present in every capacitor.

4 Output Voltage Transient Response

As shown in Figure 2, capacitors contain parasitic resistance (called "ESR" for equivalent series resistance) and also parasitic inductance (called "ESL" for equivalent series inductance), both of which affect transient response. Figure 3 shows an actual voltage waveform recorded on the output of a linear regulator when the load current was increased very quickly (similar to the example shown in Figure 2):

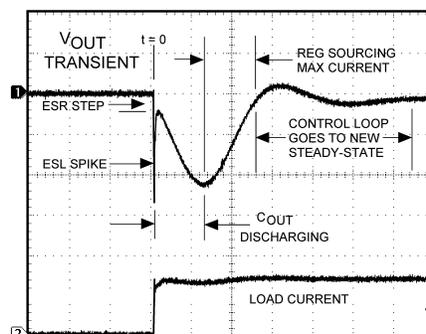


Figure 3. Output Voltage Transient

It can be seen that ESL causes a narrow spike voltage drop which is highly dependent upon the rise time of the load transient: the faster the load changes, the bigger the ESL spike on the output voltage waveform will be. The spike only exists during the time the load current is changing, since inductance only creates a voltage in response to a changing current as given by:

$$V = L \times di/dt \tag{2}$$

When the load current reaches the new value (I_{L2}), the ESL voltage spike will be over. The faster the rise time of the load current transient is, the more critical inductance becomes, both in the output capacitor as well as the PC board traces connecting it to the load. Large value ceramic capacitors are extremely low in both ESR and ESL, and are usually placed at the load terminals of devices with fast rising load transient requirements. They also improve transient response if used on the output of voltage regulators.

The output capacitor's ESR causes a change in output voltage anytime C_{OUT} is sourcing (or sinking) current, and this is shown on the waveform as the "ESR step". During the interval of time before the control loop increases I_{REG} , the output voltage is reduced by both the voltage drop across the ESR and the amount that C_{OUT} discharges.

Eventually, the error amplifier begins to increase I_{REG} in response to the drop in V_{OUT} . It should be noted that the value of I_{REG} typically does not go directly to the new value of I_{L2} , rather the error amplifier will usually turn the current source on fully to try to drive the output voltage up (often going into current limiting). Then, in most cases, the output voltage overshoots the nominal value and then falls back and eventually locks into the new equilibrium (this settling action can be seen in [Figure 3](#)). The distinctive appearance of V_{OUT} as it settles gives an accurate indication of phase margin (detailed in the next section).

When the control loop reaches the new steady-state condition (where the regulator's current source is providing I_{L2}), the output capacitor is again providing no current to the load. It is important to note that the "ESR step" is a DC voltage change in the regulated output during a load transient. The ESR step can be quite significant, which means ESR is a critical consideration when designing for the maximum allowable "voltage tolerance window" the regulated voltage must meet. High performance aluminum and tantalum electrolytic capacitors are made specifically to meet the needs of ultra low ESR applications.

5 Transient Response and Phase Margin

When the load current is suddenly changed, the operating point of the control loop is "unsettled", and it is forced to go to a new operating point. The appearance of the output voltage waveform during this transition is a very accurate indicator of the phase margin the loop has at the new operating point.

To illustrate this, [Figure 4](#) is a scope plot of the output of a voltage regulator which was subjected to a fast load current step. The phase margin was measured using a network analyzer and determined to be 49° :

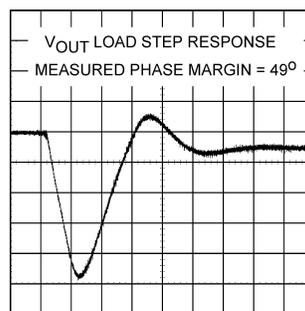


Figure 4. Output Voltage Transient Response for 49° Phase Margin

The appearance is what is known as "critically damped", which means it extinguishes very cleanly in only a single complete ring. This is ideal performance, because it gives the fastest possible settling time (and very good stability).

In [Figure 5](#), we see how the transient response is degraded if the phase margin is reduced to 30° :

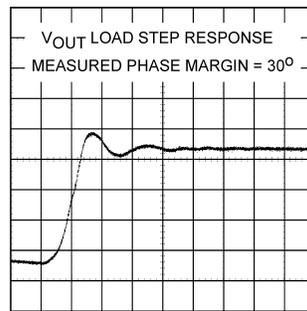


Figure 5. Output Voltage Transient Response for 30° Phase Margin

The settling characteristics now show a bit more ringing after the transient occurs (the higher DC level after the load change is a result of poor load regulation for this particular device, it is not related to phase margin or transient response). It can be seen that even though the phase margin is only 30°, the settling is fairly clean and probably acceptable for most applications.

However, if the phase margin is further reduced to 17°, we see the settling of the loop beginning to show more pronounced ringing (Figure 6):

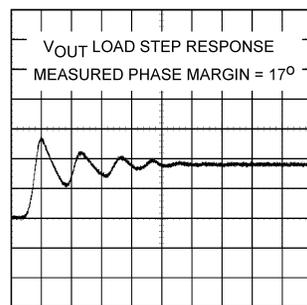


Figure 6. Output Voltage Transient Response for 17° Phase Margin

It can be seen that the ringing is beginning to take on the appearance of a sine wave oscillation, becoming even more obvious as the phase margin is reduced to only 5° (Figure 7):

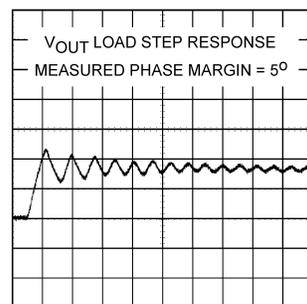


Figure 7. Output Voltage Transient Response for 5° Phase Margin

With only 5° of phase margin, the waveform shows an unmistakable sine wave which barely extinguishes. This tells the designer that the phase margin is so low the loop is on the verge of sustaining oscillations. The progressive change in the appearance of the output voltage waveforms as the phase margin diminishes illustrates how a designer can estimate phase margin using only a load transient test. This can be done very easily without special equipment, and the following section shows how.

6 Manually Testing Load Transients

A “load step” can be implemented by simply connecting (or disconnecting) the load resistor(s) to the regulator’s output and observing the change in V_{OUT} (Figure 8).

Manual testing provides a quick and easy way to check phase margin and transient response, but does not allow for adjustment of the rise time of the load current pulse. The di/dt rate of the current pulse is primarily determined by the lead inductance in series with the load resistor.

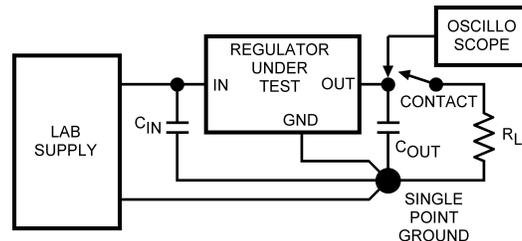


Figure 8. Circuit For Manually Testing Load Transient Response

7 Guidelines For Getting Accurate Data When Testing Load Transients

1. The switch shown as “contact” can be a mechanical switch or the ends of two clip leads. The load resistor can also be soldered to the ground pad on the PC board and tapped on the output terminal to create the load pulse.
2. The negative side of the output capacitor MUST be used as a single point ground for all connections.
3. The oscilloscope used to read the output waveform must be connected DIRECTLY across C_{OUT} .
4. Use a storage scope with single sweep capture capability (TEKTRONIX TDS 3014 or similar). Set the scope to trigger on negative going transients, since the output will drop the instant the load is connected.
5. The input capacitor C_{IN} must be sufficient to keep the input source to the regulator under test from ringing when the load step is applied. Any high frequency ringing on the input will be conducted through and seen on the output waveform. To prevent this, C_{IN} may need to be substantial: recommended values for C_{IN} are about 100 μF ceramic capacitance paralleled by an ultra-low ESR electrolytic capacitor of at least 1000 μF . The grounds of these capacitors must connect directly to the single point ground.
6. Metal-oxide or metal-film resistors work best as load resistors for transient load testing because they are non-inductive.
7. If the current step is to be measured on an oscilloscope, use a resistor and NOT a current probe (Figure 9). The scope’s trigger can be activated by the rising edge of the current pulse seen across R_{SENSE} .

A sense resistor should be used because the bandwidth limitations of even very good current probes will not allow them to accurately measure the rising edges of the current waveform which may exceed slew rates of 50A/ μs . A metal-film resistor of 50 m Ω value was used for my data. Make certain the ground end of this resistor is tied directly to the negative side of the output capacitor, or ringing will be induced by the inductance between the ground node and the resistor.

Figure 10 shows a comparison of the actual current waveform (measured across the 50 m Ω resistor) produced by a 0.1A - 3A load step and the waveform produced by a Tektronix AM503 current probe measuring the same current. The rate of change of the load current was measured as about 75A/ μs (3A rise in about 40 ns).

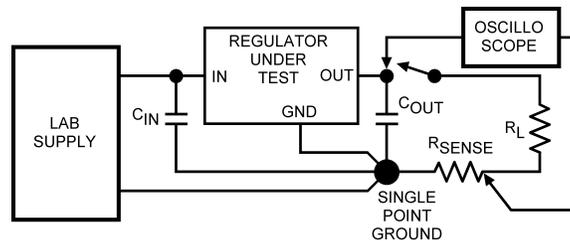


Figure 9. Using a Sense Resistor To Measure Load Current

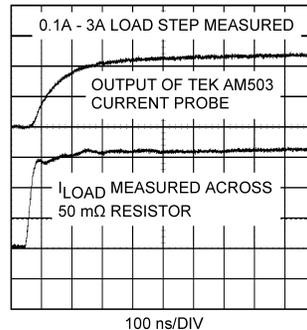


Figure 10. Comparison Showing Current Probe Bandwidth Limitations

As shown, the waveform from the current probe shows a slow and rounded leading edge due to its bandwidth limitations when trying to measure a very fast current change.

Manual testing gives an easy technique to evaluate loop stability, but the main limitation of this method is that the rise and fall times of the current step are not adjustable. The next section presents how to build an electronic load with adjustable slew rate.

8 Electronic Load Transient Tester

An inexpensive electronic load can be built which allows the user to adjust the rise and fall time of the load current (Figure 11).

The circuit uses N-FET (Q1) as a switch, which allows current to flow through the load resistance (R10) when its gate is driven on. R10 should be selected to provide the desired load current when Q1 is on. The 50 mΩ resistor (R11) is used to sense the current in case a current waveform is desired (it can be deleted if current monitoring is not needed). Any good N-FET with low ON resistance and good switching characteristics can be used for Q1. Since the tester usually operates at a low duty cycle, power dissipation in the FET is not excessive and PCB copper can provide adequate heatsinking for most applications. C6 and R9 are used to reduce the ringing across Q1 when it switches.

U1 is a free-running oscillator whose frequency is adjusted by R2. U2 is a one-shot triggered by U1, and the on time of the one shot is adjusted by R6. Using R2 and R6, both the frequency and duty cycle of the load pulse may be varied. For the components shown, the frequency can be adjusted from about 130 Hz up to about 2 kHz, and the pulse width can be adjusted from about 20 μs to 400 μs.

The rise and fall times of the load current pulse can be adjusted by varying the rise and fall time of the voltage applied to the gate of Q1. Since the output of U2 drives the gate of Q1, an R-C network which slows the rise (and fall) time of this voltage will provide the desired adjustment to the di/dt rate of the load current pulse. R8 working with C5 slows the rise time of the gate voltage, while R7 working with C5 slows the fall time (D1 and D2 isolate the rising and falling drive signals so they can be adjusted independently).

The value of C5 must be adjusted based on the rise/fall times desired: for fastest possible rise times (50A/μs or more) C5 can be omitted. For slow rise times (like 0.5A/μs), a value of about 0.1 μF can be used, with R7 and R8 dialing in the slew rate of each edge.

When selecting C5, it should be noted the drive to the gate of Q1 is not symmetric: the output of U2 pulls up to about 11V, but only pulls down to ground. So, the FET has much stronger gate drive turning ON than OFF, which will tend to make the rising edge of the load pulse faster than the falling edge.

Table 1 shows the load current pulse slew rates which can be obtained by adjusting R7 and R8 from minimum to maximum for various values of C5. This data was taken for a 0 – 3A load current pulse.

If equal times are desired for the rising and falling edges: The rising edge has a wider min/max range of slew rate for any given value of C5. Therefore, C5 should be selected so the desired value of the falling edge slew rate is within the ranges shown in Table 1. Then, adjust R7 until the falling edge slew rate is correct and adjust R8 to get the rising edge to match the falling edge.

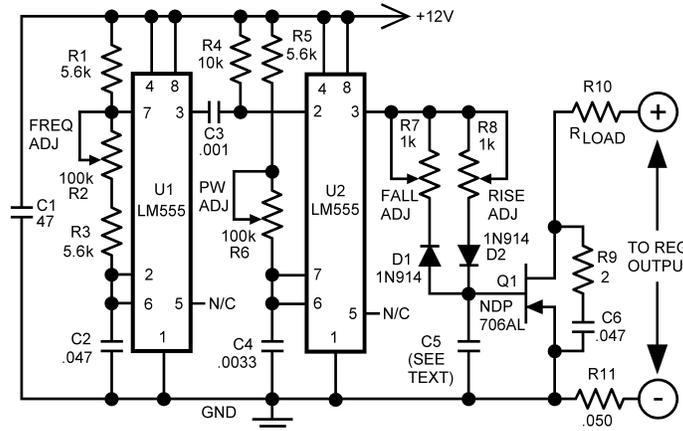


Figure 11. Electronic Load Transient Tester

Figure 12. Table 1. Load Current Pulse Slew Rates For Various Values of C5

C5 VALUE	RISING EDGE (A/ μ s)		FALLING EDGE (A/ μ s)	
	MIN	MAX	MIN	MAX
ZERO	0.50	85	2.2	15
1000 pF	0.45	75	1.9	12
0.01 μ F	0.38	70	1.5	11
0.047 μ F	0.25	50	0.75	10
0.1 μ F	0.21	38	0.50	7.5

9 Guidelines For Using the Electronic Load Tester

1. Minimize all trace lengths along the current path from the input to output, through the FET. Inductance along this path will degrade rise time and cause ringing.
2. Use low inductance resistors like metal-film or metal-oxide for load and sense resistors.
3. The ground connection tying the tester negative terminal to the negative output of the regulator is most critical: the scope probe measuring V_{OUT} has its ground lead connected to the ground side of C_{OUT} . The probe measuring across the current sense resistor (R11) has its ground connected to the negative side of the sense resistor. The electrical connection between those two nodes must be low inductance or ringing will occur, distorting the current waveform. If necessary, the current sense resistor can be physically moved to the regulator ground (on the negative side of C_{OUT}) so there will be no ground bounce between the scope ground points.

To illustrate the effects of ground bounce caused by inductance between the two ground points, [Figure 13](#) shows a transient scope shot of both the regulated output and the current waveform measured across R11. In this case, the tester negative load terminal was connected to the regulator's output capacitor negative terminal via a piece of copper braid about 1/4" wide and 3/4" in length, which has fairly low inductance:

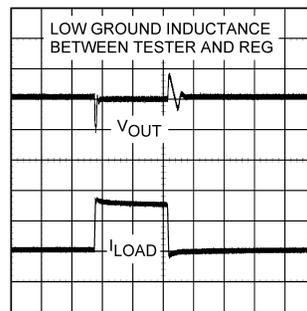


Figure 13. Transient Waveforms With Low Inductance Ground Connection Between the Pulse Tester and Regulator Under Test

To increase the amount of ground lead inductance, the same measurement as shown in [Figure 13](#) was repeated EXCEPT that the ground lead between the negative side of the regulator’s output capacitor and the negative terminal of the pulse tester was connected using a 2” piece of 18# wire (which has more inductance than the short lead used in the first test). [Figure 14](#) shows the degradation in the load current waveform due to ground bounce resulting from the voltage developed across the inductance of the 2” wire which causes the ground of the scope probe connected across the current sense resistor to bounce with respect to probe measuring the output voltage.

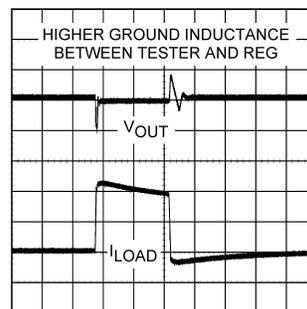


Figure 14. Load Current Waveform Distorted By Increased Ground Inductance Between Pulse Tester and Regulator Under Test

In comparing with [Figure 13](#), it can be seen that the current waveform in [Figure 14](#) shows excessive overshoot in both directions and also the peak amplitude is larger than actual value. A very close examination of [Figure 13](#) shows the current waveform there also shows very slight overshoot (the effects of ground lead inductance) since no lead has zero inductance. But, when inductance is excessive the accuracy of the reading is corrupted ([Figure 14](#)). This illustrates why when two scope probes are used, care must be taken that the grounds are not bouncing with respect to each other.

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