AN-2029 Handling and Process Recommendations

Application Report

Literature Number: SNOA550H
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Contents

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ABSTRACT

This application report provides recommendations for handling, storing, and mounting Texas Instruments' surface mount IC packages. Please reference published IPC-J-STD-004, IPC-JEDEC J-STD-020, and IPC-JEDEC J-STD-033 documents for their latest versions.

1 Trademarks

All trademarks are the property of their respective owners.

2 Introduction

The final manufacturing yield and board level reliability are influenced by various factors and processes outside the control of the IC manufacturer. This application note is intended only as a guideline or reference. Due to the variety of possible board assembly materials and equipments, Texas Instruments advises the user to consult their individual suppliers and vendors.

3 Moisture Sensitivity Level

Due to the hygroscopic nature of the plastic encapsulants, the plastic ICs absorb a certain amount of moisture. When subjecting a SMT device to a reflow soldering process (such as infrared, convection, or vapor phase), the moisture inside the package can create excessive internal pressure resulting in delamination or even a cracked package (popcorn effect).

TI's components that are considered moisture sensitive are sealed in moisture barrier bags (MBB) together with a desiccant and a Humidity Indicator Card (HIC). Texas Instruments generally follows Industry Standards IPC/JEDEC J-STD-020 and J-STD-033 to determine the moisture sensitivity level and corresponding floor life time for TI's plastic package types. To quickly locate *Moisture Sensitive Level (MSL) Rating* and *Peak Reflow* information, search by part number using the *Moisture sensitivity level search tool* or see the device data sheet.

The floor life time is the maximum time period from the opening of the MBB to the final reflow soldering process. The MSL Level and floor life time as per Table 1 is provided on TI's immediate and intermediate packing container label. Additionally, the MSL level and the maximum peak package temperature for TI's devices can be found within the Product Folder of TI's website.

Table 1. Moisture Sensitivity Levels (According to IPC-JEDEC J-STD-033)

MSL Level	Floor Life (out of MBB)	
	Time	Conditions
1	Unlimited (no moisture barrier bag)	≤ 30ºC / 85% RH
2	1 year	≤ 30ºC / 60% RH
2A	4 weeks	≤ 30ºC / 60% RH
3	168 hours	≤ 30ºC / 60% RH
4	72 hours	≤ 30ºC / 60% RH
5	48 hours	≤ 30ºC / 60% RH
5A	24 hours	≤ 30ºC / 60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label	≤ 30ºC / 60% RH

4 Storage and Shelf Life

Solderability tests were conducted on components after long term storage in warehouse conditions and after exposure to accelerated aging environment. Based upon the results, TI's shelf life of dry-packaged moisture sensitive devices inside the unopened moisture barrier bag is 3 (SSL: Standard Shelf life) or 6 (ESL: Extended Shelf Life) years from the time it was manufactured or one year from the date of delivery by TI or a TI authorized distributor, unless otherwise specified when stored in an environment not exceeding 30ºC / 40%–85% RH per TI's recommendation. MBB has 40ºC / 90% RH capability maximum per JEDEC.

Component storage outside the MBB should be soldered within floor life specification on the moisture bag for SMT instruction or placed in a dry storage cabinet at < 25°C and < 10% RH to prevent moisture absorption.

The shelf life with regard to soldering of non dry-packed devices, that is, the MSL1 product has the capability of three years for SSL or six years for ESL product from the time it was manufactured or one year from the date of delivery by TI or a TI authorized distributor. To quickly locate shelf life information (SSL or ESL) , see the packing label sample in Figure 1. +5 is the ESL product. See the product shelf life FAQs at https://www.ti.com/quality/docs/productshelflife.tsp.

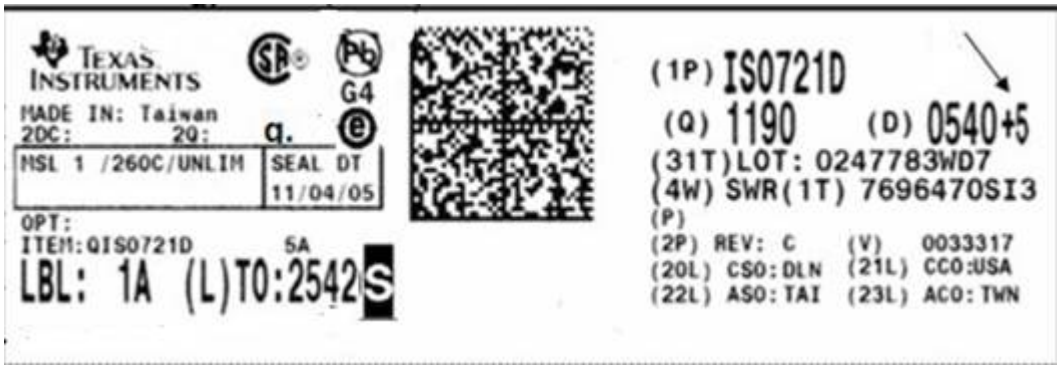

Figure 1. Packing Label

5 Reflow Soldering

The most popular soldering method for surface mount devices is forced convection reflow and therefore the topic of this chapter. Other possible solder processes for surface mount devices are, with restrictions, infrared reflow (IR) and vapor phase.

NOTE: SMD (Surface Mount Device) is not recommended for flow soldering (wave soldering). TI cannot guarantee device quality if customer applies flow soldering. TI devices are qualified to J-STD-020 standard.

It is not possible for an IC manufacturer to provide a general reflow profile recommendation for a customer in charge of board assembly. Reflow furnace settings depend, for example. on the number of heating and cooling zones, type of solder paste/flux used, board and component size as well as component density.

The actual temperature setting needs to be above the liquidus temperature (solder melting point) of the solder paste in order to form a reliable solder joint, while the upper limit is clearly defined by the maximum peak package body temperature depending on package thickness and volume as provided by IPC /JEDEC J-STD-020; see Table 2 and Table 3.

Table 2. Maximum Peak Package Body Temperature Tp (According to IPC-JEDEC J-STD-020 for Pb-Free Process)

Package Thickness	Volume < 350 mm^3	Volume 350-2000 mm^3	Volume > 2000 mm^3
<1.6 mm	260 °C	260 °C	260 °C
1.6 to 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Table 3. For SnPb Eutectic Process

Package Thickness	Volume < 350 mm^3	Volume ≥ 350 mm^3
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

NOTE: Package volume excludes external terminals (such as balls, bumps, lands, leads) and nonintegral heat sinks.

It is important to understand that the temperature profile provided within IPC/JEDEC J-STD-020 reflects the profile used for device (MSL) classification; see Figure 2 and Table 4 with the temperature measured on the top package surface during the reflow soldering process and subject to three cycles of the appropriate reflow conditions as defined in Table 2 and Table 3.

The actual board assembly reflow furnace settings need to be developed separately depending on furnace characteristics and board design. The selected temperatures should not exceed the parameters used for MSL classification.

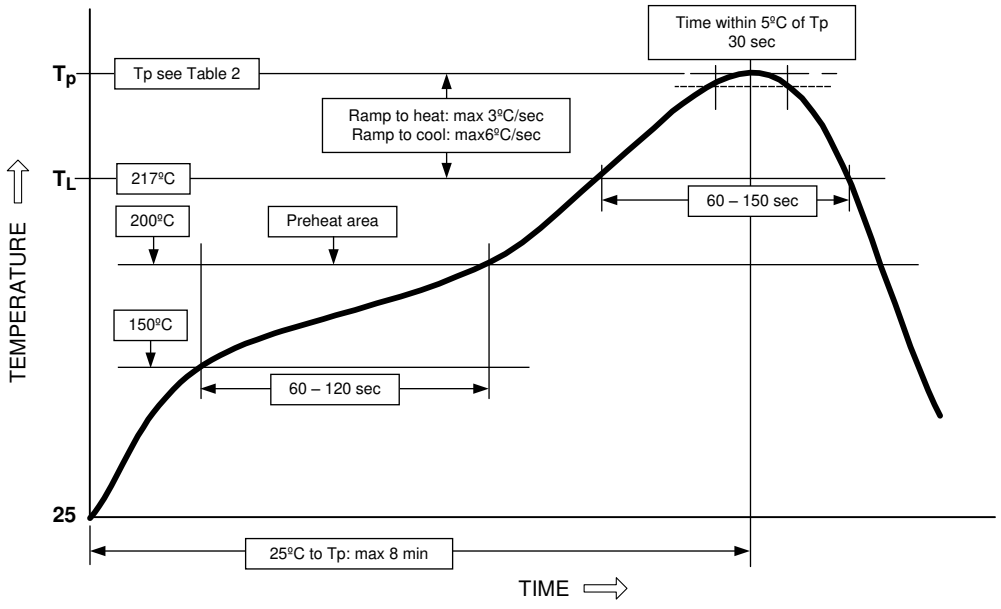

Figure 2. Classification Reflow Profile (Peak Package Body Temperature) for Pb-Free Reflow Soldering

Table 4. Classification Reflow Profile Parameters (According to IPC-JEDEC J-STD-020)

Profile Parameter	Pb-Free Assembly	SnPb Assembly
Preheat temperature range	150°C to 200°C	100°C to 150°C
Duration	60 to 120 sec	60 to 120 sec
Ramp-up rate	Max 3°C/sec	Max 3°C/sec
Liquidus temperature T_L	217°C	183°C
Time above T_L	60 to 150 sec	60 to 150 sec
T_P peak package body temperature	See Table 2	See Table 3
Dwell time within 5°C of TP	Max 30 sec	Max 20 sec
Ramp-down rate	Max 6°C/sec	Max 6°C/sec

6 Flow Soldering (Wave Soldering)

The most popular soldering method for through hole devices is forced flow soldering (wave soldering). It is not possible for an IC manufacturer to provide a general soldering recommendation for a customer in charge of board assembly. It is important to understand that the solder temperature should be within JESD22-B106E for SnPb and Pb-free solder. The temperature should not exceed the solder heating condition and only devices' leads should be immersed in solder.

6.1 Flux Selection

The key function of flux is to dissolve the oxides on the metal surface to facilitate the wetting of the molten solder. The most commonly used flux is Rosin based with low flux residue activity (ROL0 and ROL1 per IPC-J-STD-004). Certain active and aggressive fluxes are easy to use but may cause corrosion and contamination if not cleaned properly.

TI recommends using ROL0 or ROL1 type flux with a minimum level of corrosive elements, mild activity level and a pH value close to 7. Fluxes containing chloride should be avoided.

6.2 Wave Soldering Profile

Below are two examples of wave soldering profiles using Eutectic (tin-lead solder) and lead free solder. Neither example is intended to be used *as is*. Actual wave soldering profiles should be optimized based on PCB thickness, component density and guidelines provided by the solder material supplier.

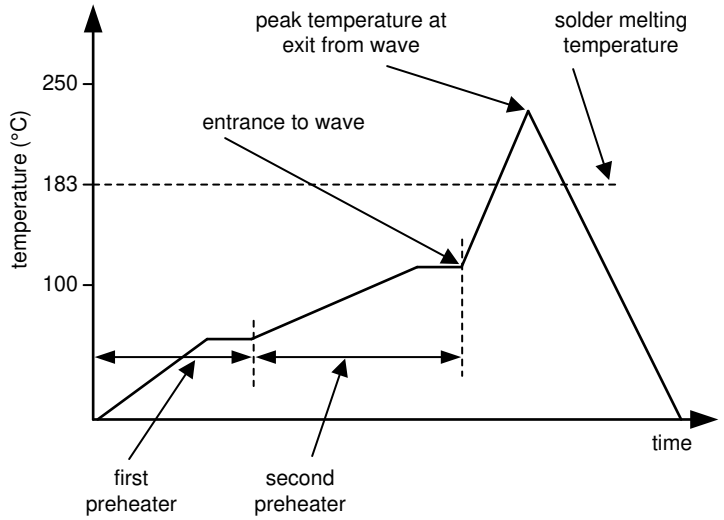

Figure 3. Example of Eutectic (SnPb) Wave Soldering Profile

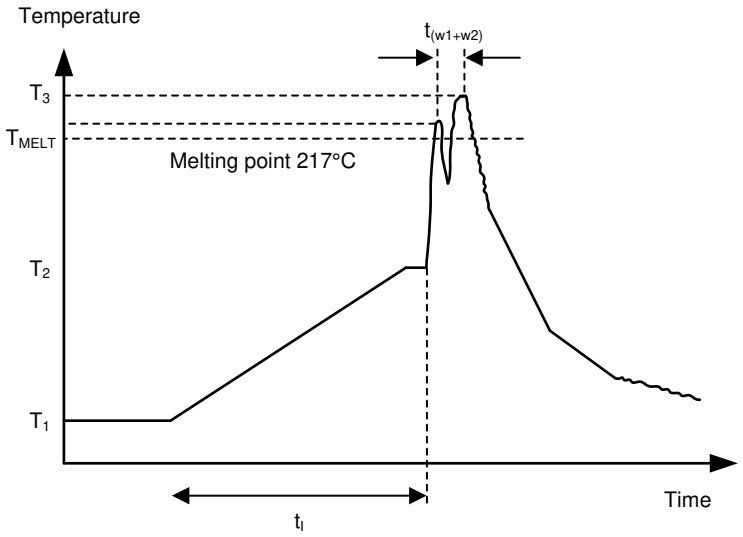

Figure 4. Example of Lead Free Wave Soldering Profile

7 Drying of Components

If the Floor Life time is exceeded or the Humidity Indicator Card indicates excessive moisture after opening the MBB (the color change is described on the HIC card; see Figure 5), baking is required prior to the reflow process in order to remove any moisture out of the plastic package.

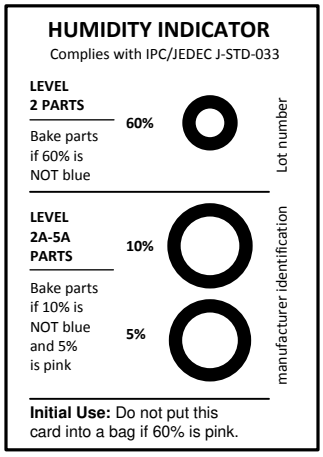

Figure 5. Humidity Indicator Card as per IPC/JEDEC J-STD-033

Conditions for drying components depend on package thickness, MSL Level, and baking temperature. Table 5 provides an excerpt of IPC/JEDEC J-STD-033 on drying mounted or unmounted SMD packages. Please note that standard packing material such as tape, reel, and tubes are considered low temperature carriers, and SMD packages may not be baked in these carriers at any temperatures higher than 40°C. Only high temperature trays are able to withstand baking process at 125 ºC.

Table 5. Reference Conditions for Drying Mounted and Unmounted SMD Packages (as per IPC-JEDEC J-STD-033)

Package Body	Level	Bake @ 125 °C + 10/-0 ºC < 5% RH		Bake @ 90 °C + 8/-0 ºC ≤ 5% RH		Bake @ 40 °C + 5/-0 ºC ≤ 5% RH	
		Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by < 72 h
Thickness < 0.5 mm (see Note 5)	2	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)
	2a	1 hour	1 hour	2 hours	1 hour	12 hours	8 hours
	3	1 hour	1 hour	3 hours	1 hour	22 hours	8 hours
	4	1 hour	1 hour	3 hours	1 hour	22 hours	8 hours
	5	1 hour	1 hour	3 hours	1 hour	23 hours	8 hours
	5a	1 hour	1 hour	4 hours	1 hour	26 hours	8 hours
Thickness > 0.5 mm ≤ 0.8 mm (see Note 5)	2	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)
	2s	4 hours	3 hours	15 hours	13 hours	4 days	3 days
	3	4 hours	3 hours	15 hours	13 hours	4 days	3 days
	4	4 hours	3 hours	16 hours	13 hours	4 days	3 days
	5	4 hours	3 hours	16 hours	13 hours	4 days	3 days
	5a	4 hours	3 hours	16 hours	13 hours	4 days	3 days

Table 5. Reference Conditions for Drying Mounted and Unmounted SMD Packages (as per IPC-JEDEC J-STD-033) (continued)

Package Body	Level	Bake @ 125 °C + 10/-0 °C < 5% RH		Bake @ 90 °C + 8/-0 °C ≤ 5% RH		Bake @ 40 °C + 5/-0 °C ≤ 5% RH	
Thickness > 0.8 mm ≤ 1.4 mm (see Note 5)	2	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)	Not Required (see Note 4)
	2a	8 hours	6 hours	25 hours	20 hours	8 days	7 days
	3	8 hours	6 hours	25 hours	20 hours	8 days	7 days
	4	9 hours	6 hours	27 hours	20 hours	10 days	7 days
	5	10 hours	6 hours	28 hours	20 hours	11 days	7 days
	5a	11 hours	6 hours	30 hours	20 hours	12 days	7 days
Thickness > 1.4 mm ≤ 2.0 mm (see Note 5)	2	18 hours	15 hours	63 hours	2 days	25 days	20 days
	2a	21 hours	16 hours	3 days	2 days	29 days	22 days
	3	27 hours	17 hours	4 days	2 days	37 days	23 days
	4	34 hours	20 hours	5 days	3 days	47 days	28 days
	5	40 hours	25 hours	6 days	4 days	57 days	35 days
	5a	48 hours	40 hours	8 days	6 days	79 days	56 days
Thickness > 2.0 mm ≤ 4.5 mm (see Note 5)	2	48 hours	48 hours	10 days	7 days	79 days	67 days
	2a	48 hours	48 hours	10 days	7 days	79 days	67 days
	3	48 hours	48 hours	10 days	8 days	79 days	67 days
	4	48 hours	48 hours	10 days	10 days	79 days	67 days
	5	48 hours	48 hours	10 days	10 days	79 days	67 days
	5a	48 hours	48 hours	10 days	10 days	79 days	67 days
Exception for BGA package > 17 mm x 17 mm or any stacked die package	2–5a	96 hours (See Note 2 and Note 5)	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level

Note 1: Table 5 is based on worst-case molded lead frame SMD packages. Users may reduce the actual bake time if technically justified (that is, absorption and desorption data, and so forth). In most cases it is applicable to other non-hermetic surface mount SMD packages. If parts have been exposed to > 60% RH it may be necessary to increase the bake time by tracking desorption data to insure parts are “dry”.

Note 2: For BGA packages > 17 mm x 17 mm, that do not have internal planes that block the moisture diffusion path in the substrate, may use bake times based on the thickness/moisture level portion of the table.

Note 3: If baking of packages > 4.5 mm thick is required see appendix B of J-STD-033.

Note 4: Baking not required if Floor Life exposure is limited to < 30C and < 60%RH for thin (< 1.4 mm) MSL2 devices. This is due to the moisture diffusion behavior of the thin devices, which were fully saturated after the absorption at MSL 2 (168 hours @85C/60%RH).

Note 5: The bake times specified are conservative for packages without blocking planes or stacked die. For a stacked die or BGA package with internal planes that impede moisture diffusion the actual bake time may be longer than that required in Table 5.

8 Repair

In case repair or even replacement of a component is needed, it is important that the temperature used for repairing, desoldering, or replacing the component is selected as low as possible to avoid any damage to the adjacent components or PC board. The repair profile should be similar to the actual reflow profile. Common rework tools are either hot gun or available rework machines.

In addition, depending on the MSL level of the component and if the floor life time from initial reflow soldering process to the repair process is exceeded, a baking process is required with parameters provided in IPC/JEDEC J-STD-033. Otherwise, the accumulated moisture can cause damage as described in the previous chapters.

Proper handling practices are required to prevent any ESD damages during any handling of the components.

9 Manual Repair Procedure

Definition of repair: To fix missing solder or solder bridging on PCB after SMT for production soldering methods.

Scope: This is applied to all surface mount packages without solder balls attached, and 8- to 20-pin DIP and TO packages.

1. Solder wire with flux core is used for repair.
2. Solder iron temperature setting: <360°C ±10°C.
3. Solder iron should be contacting to the lead.
4. Contact duration: 4 ±2 seconds per lead x 2 times.
5. The package surface temperature should be less than their peak reflow temperature (245°C, 250°C, or 260°C).
6. Follow shelf life/floor life specification on the moisture bag for SMT instruction.
7. The repaired part should be baked at 125°C for 48 hours or per J-STD-033 if the shelf life of the part has exceeded the MSL specification or if it is unknown.

10 Manual Rework Procedure

Definition of rework: To remove or replace IC package on PCB after SMT for production soldering methods.

Scope: This is applied to all surface mount packages without solder balls attached, and 8- to 20-pin DIP and TO packages.

1. Solder wire with flux core is used for rework.
2. Solder iron temperature setting: <360°C ±10°C.
3. Solder iron should be contacting to the lead.
4. Contact duration: 4 ±2 seconds per lead × 2 times.
5. The package surface temperature should be less than their peak reflow temperature (245°C, 250°C, or 260°C).
6. Follow shelf life/floor life specification on the moisture bag for SMT instruction.
7. The rework part and PCB should be baked at 125°C for 48 hours or per J-STD-033 if the shelf life of the part has exceeded the MSL specification or if it is unknown.
8. Use a hot gas rework station for removing and placing the package on a PCB during rework.
   - Example: See the All-Spec website for MetCal equipment, techniques and procedures.

11 PCB Assembly Cleaning

If the printed circuit boards were assembled using a rosin based or other flux system which requires removal from the board surface after reflow, the subsequent cleaning operation should be performed as shortly after reflow as possible. The timely initiation of the cleaning operation is dictated by the ability of the flux to collect and harden with additional residues under and around traces and the bodies of components. The lack of attention to the timely removal of this residue present additional and unneeded removable difficulties, with the possibility that some contaminates may be trapped in flux and remain on the surface of the board, potentially compromising quality of the finished product. TI recommends that the customer works with their supplier of flux or cleaning solvent to determine the optimum cleaning conditions.

Pre-Wash Section	Top	30 – 50 psi
	Bottom	30 – 50 psi
Wash Section	Top	30 – 50 psi
	Bottom	30 – 50 psi
Pre-Rinse Section	Top	90 – 110 psi
	Bottom	100- 120 psi
Rinse Section	Top	90 – 110 psi
	Bottom	100 – 120 psi
Final Rinse Section	Top	5 – 30 psi
	Bottom	10 – 35 psi

Dryer Temperature:

	170 - 190° F

Pre-Wash, Wash, and Rinse Tank Temperature:

	140 - 160° F

Conveyor Speed:

	2.8 - 3.2 ft/min

Figure 6. Example of In-Line Cleaning Set Up Conditions

12 Permissions

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from G Revision (March 2020) to H Revision **Page**

- Revised *Storage and Shelf Life* section 4

Changes from F Revision (November 2019) to G Revision **Page**

- Updated *Moisture Sensitive Level (MSL) Rating* and *Peak Reflow* information and added link to the *Moisture sensitivity level search tool* in Section 3. 3
- Changed JSTD-22 B106 to JESD22-B106E in the *Flow Soldering (Wave Soldering)* section. 6
- Changed 'greater than' symbol to 'less than' symbol in three columns of Table 5..... 8

Changes from E Revision (June 2016) to F Revision **Page**

- Replaced Table 5 with new table 8
- Removed section numbers from table and figure titles 8
- Removed the 'B.1/C' from 'JEDEC J-STD-033B.1/C' throughout the document. 10

Changes from D Revision (March 2016) to E Revision **Page**

- Revised *Storage and Shelf Life* section 4

Changes from C Revision (July 2015) to D Revision **Page**

- Added *Flux Selection* 6
- Added *Wave Soldering Profile* 6
- Added *Example of In-Line Cleaning Set UP Conditions* graphic 11

Changes from B Revision (June 2014) to C Revision **Page**

- Changed to IPC-JEDEC J-STD-033C throughout document 3
- Added information to *Reflow Soldering* 4
- Changed to IPC-JEDEC J-STD-020E throughout document 5
- Added *Flow Sodering (Wave Soldering)* 6
- Added *PCB Assembly Cleaning* 11

Changes from A Revision (June 2012) to B Revision **Page**

- Changed format from National Semiconductor to Texas Instruments 3
- Changed link to SNOA549 IN *Moisture Sensitivity Level* 3
- Added *Manual Repair Procedure* and *Manual Rework Procedure* 10

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