Analog Engineer's Circuit Amplifiers

Zero cross detection using comparator with dynamic reference

Design Goals

Input		SUPPLY
V_{sig} (min)	$V_{baseline}$ (max)	V_{CC}
500 mVpp	4.75 V	5 V

Design Description

This cookbook design allows the detection of the zero crossings of an AC waveform superimposed on a varying DC baseline component, such as signals from a photo diode, wireless receiver, pick-up coil or sensor amplifier outputs with a DC offset.

The comparators reference voltage is dynamically created from the average of the varying DC offset component (offset) and centered on the midpoint of the AC signal. The generated reference voltage and the original signal containing the AC component are compared to create the actual zero cross detection.

In order for the circuit to work properly, the following criteria must be met:

- The signal frequency must be significantly higher than any shifts in the baseline voltage (at least 10 times higher).
- The signal should be symmetrical around the waveform midpoint, such as a sine wave, 50% duty cycle square wave or NRZ digital waveform.
- The signal must have adequate amplitude to overcome any added hysteresis and comparator input offset voltage.

The TLV7011 is selected for this application. TLV7011 has sufficiently low propagation delay (260 ns), a push-pull output with rail-to-rail inputs and low supply current (5 µA). The low input bias current (5 pA typical) allows it to be driven directly with a high impedance source (for example, passive sensors) and utilize large resistors and small value filter capacitors. For lower power and lower frequency applications (<100 kHz) , the TLV7031 may be used to save some power. For even lower frequencies (<5 kHz), the TLV3691 may be used for the ultimate power savings (<100 nA).

Figure 1-1 shows the schematic of the circuit.

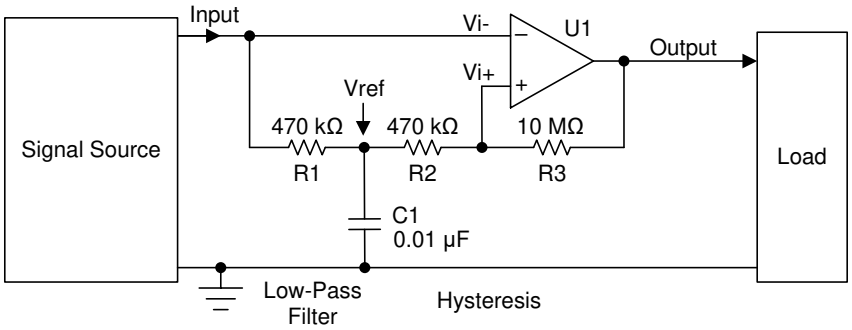

Figure 1-1. Input Signal Processor Using Dynamic Reference

The Signal Source consists of a AC signal superimposed on a slowly varying DC offset (baseline). The RC network (C_1 and R_1) forms a low-pass filter to establish the dynamic reference voltage, V_{ref}, which "tracks" the

offset but not the superimposed AC signal. It's designed as a first order low-pass filter with a cutoff frequency set well above the baseline shift frequency, but far below the AC signal frequency. The V_{ref} voltage is passed to the non-inverting input V_i+ of the comparator and the unfiltered input signal containing the AC component is applied to the inverting input V_i-. Consequently the filtered baseline shift of the input signal is canceled out at the inputs and only the AC signal is used to produce the binary output.

R_2 and R_3 introduce additional hysteresis to make the circuit more robust with noisy signals. If hysteresis is not desired, R2 can be 0 ohms and R3 removed.

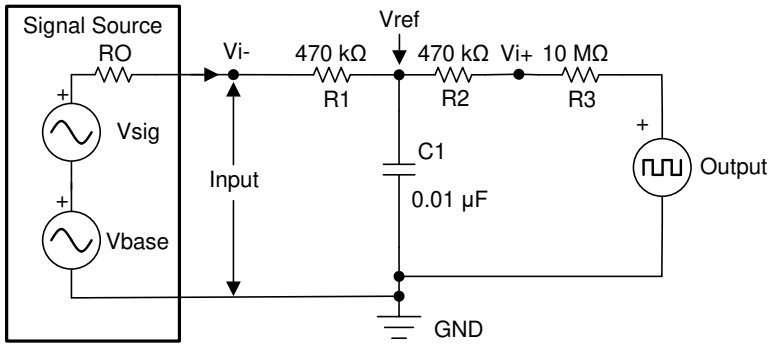

Figure 1-2. Equivalent Circuit of Sensor Signal Processor

Figure 1-2 shows an equivalent circuit of Figure 1-1. The inputs to U1 have been omitted due to their negligible input bias current (pA's). The Signal Source is composed of two parts: the actual AC input signal V_{sig} and the DC baseline voltage, V_{base}. The source internal output impedance is denoted as R_0. The U1 output is represented as a square wave voltage source which toggles between 0V and V_{cc}.

Dynamic reference node V_{ref}

Figure 1-3 shows a simplified equivalent circuit for Vref node. The output voltage source has been omitted for its frequency is well above the cut-off frequency. However the asymmetry of output signal creates a DC offset V_{offset} which will be described later.

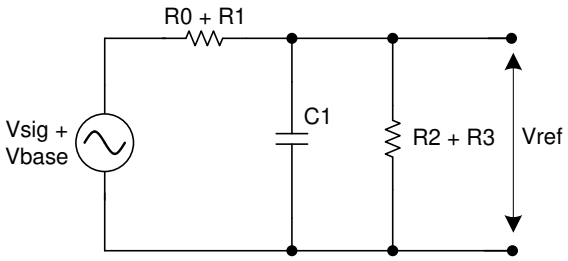

Figure 1-3. Dynamic Reference Node V_{ref}

Figure 1-4 shows a further simplified equivalent circuit of Figure 1-3.

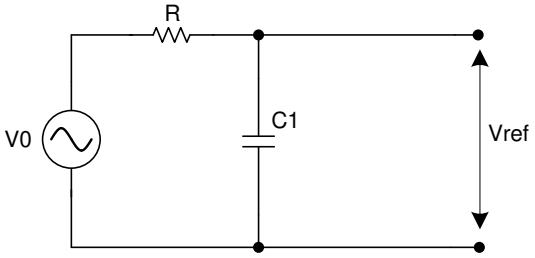

Figure 1-4. Simplified Reference Node V_{ref}

Where R and v_0 is defined in Equation 1.

$$v_o = \frac{R_2 + R_3}{(R_O + R_1 + R_2 + R_3)} \times (V_{base} + V_{sig}) \quad (1)$$

- Where: $R = (R_0 + R_1) \parallel (R_2 + R_3)$

Also in Equation 2 is the cutoff frequency, f_0, which is crucial in order for the circuit to work. f_0 must be higher than the baseline frequency, but significantly lower than the AC signal frequency.

$$f_0 = \frac{1}{2 \times \pi \times R \times C_1} \quad (2)$$

$$f_0 = \frac{1}{2 \times \pi \times ((R_O + R_1) \parallel (R_2 + R_3)) \times C_1} \quad (3)$$

Adding hysteresis adds a DC offset component, V_{offset}, introduced by the input signal and comparator output. Eliminating the V_{sig} from the source, we get Equation 1.

The shifting DC offset, V_{offset} , is introduced primarily by the comparator binary output. The input signal term V_{sig} has been dropped for being well beyond the cut-off frequency.

$$V_{ref} = v_o + V_{offset} \quad (4)$$

$$V_{ref} = \frac{R_2 + R_3}{R_O + R_1 + R_2 + R_3} \times V_{base} + V_{offset} \quad (5)$$

Inverting input node V_i-

Figure 1-5 shows an equivalent circuit for V_i- derived from Figure 1-2. The output voltage source has been dropped due to the higher frequency.

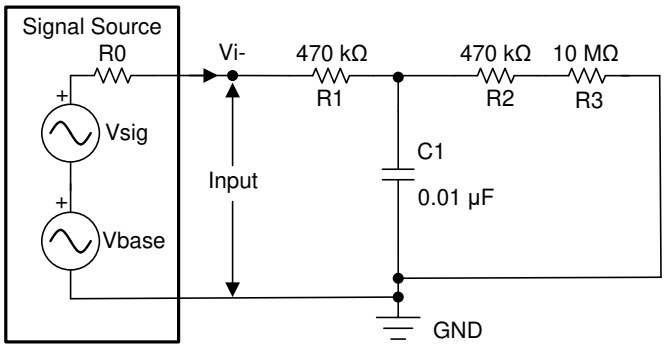

Figure 1-5. Inverting Input Node V_i-

Figure 1-6 separates the input signal path and the baseline path to further simplify the analysis. It uses the fact that the impedance of $C_1$is negligibly small at the input signal frequency f_{sig} but much greater at the baseline frequency f_{base}.

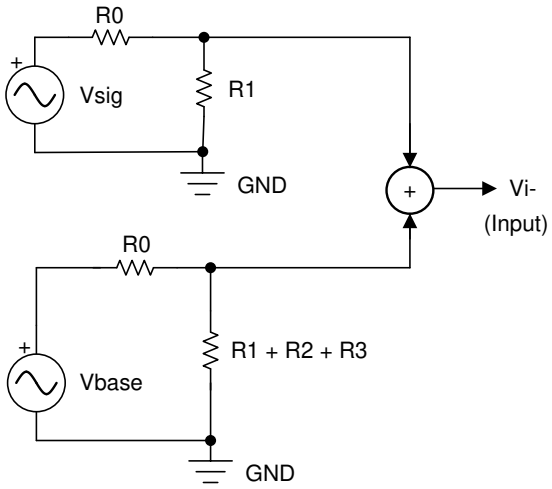

Figure 1-6. Inverting Input Node V_i- (Separated Paths)

$$V_i - = \frac{R_1 + R_2 + R_3}{R_O + R_1 + R_2 + R_3} \times V_{env} + \frac{R_1}{R_O + R_1} \times V_{sig} \quad (6)$$

Equation 6 shows the calculation result from Figure 1-6.

Non-inverting input node V_i+

Figure 1-7 shows the equivalent circuit for the non-inverting input path which derived from Figure 1-2. Equation 7 and Equation 8 shows the equations of the amplitude when output is "Low" (0 V) and "High" (V_{CC}) respectively.

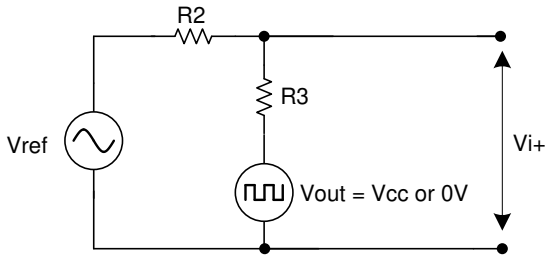

Figure 1-7. Non-inverting Input Node V_i+

$$V_i + = \frac{R_3}{R_2 + R_3} \times V_{ref} \quad when\ Output = 0\ V \quad (7)$$

$$V_i + = \frac{R3}{R2 + R3} \times V_{ref} + \frac{R2}{R2 + R3} \times V_{CC} \quad when\ Output = V_{CC} \quad (8)$$

Substitute V_{ref} with what has been defined in Equation 9, the non-inverting input node V_i+ can be expressed in terms of baseline V_{base} and a modified offset voltage V'_{offset} followed by the hysteresis term Equation 9.

$$V_i + = \frac{R_3}{R_O + R_1 + R_2 + R_3} \times V_{base} + V_{offset} + \frac{R_2}{R_2 + R_3} \times V_{CC} \times (0,1) \quad (9)$$

Maximum Frequency

The maximum theoretical toggle frequency (f_{toggle}) of the comparator can determined from the inverse of the sum of the positive propagation delay (t_{PLH}), output risetime (t_r), negative propagation delay (t_{PHL}), and output falltime (t_f), as shown in Equation 10. Since comparators respond faster to larger input signals, the propagation delay time should reflect the actual amount of overdrive (AC signal) that is applied to the input. Large propagation

delay variations can occur when the input overdrive is less than 100 mVpp. For worst-case analysis, use the slowest propagation time.

$$f_{toggle} = \frac{1}{t_{PLH} + t_r + t_{PHL} + t_f} \quad (10)$$

For the TLV7011, the theoretical highest operational frequency is 1.7 MHz, as shown in Equation 11, whereas the lower power TLV7031 is good to 166 kHz, and the much slower, nanopower TLV3691 is good to 11.6 kHz.

$$f_{toggle} = \frac{1}{310\,ns + 5\,ns + 260\,ns + 5\,ns} = 1.7\ MHz \quad (11)$$

The above formula does not take into account output waveform distortions or device-to-device variations. TI recommends to run the device well below the theoretical limits and to have at least a 50% margin from the calculated the prop delay values to insure reliable operation. A faster comparator will reduce the phase-lag between the actual zero crossing point and output transition, but at the expense of more quiescent supply power.

Power-On Behavior

It should be noted that upon first power-on of the circuit, or the first application of the input signal from 0 V, will take a period of time for the filter capacitors to charge-up. During this time the output will not transition. This may take up to several time constants of the RC combination of the low-pass filter components, initial output state and the chosen signal thresholds.

Conclusion

If we choose the value of R3 significantly greater than the sum of R1 and R2, the v_{base} terms are be canceled out. Now we've successfully removed the baseline term V_{base} from comparators operation, and only the input signal V_{sig} and the generated V_{ref} are used for producing the comparator output.

Design Simulations

The input signal frequency f_{sig} is set as 11 kHz and the baseline frequency f_{base} is set to 0.5 Hz on top of 2.5 V. The cutoff frequency of the low-pass filters is set to 3.6 Hz.

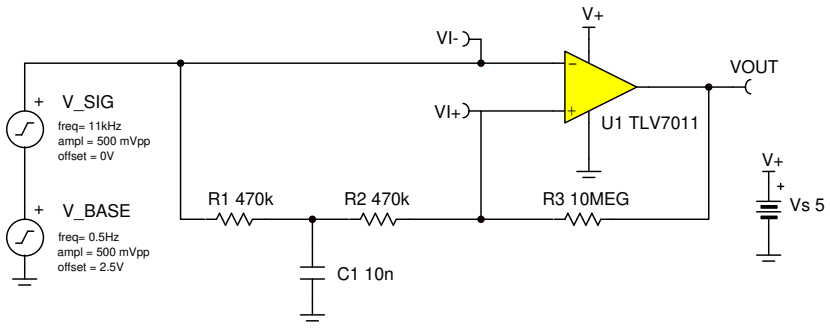

Figure 1-8. Circuit Simulation Schematic

Dynamic Simulation Results (Output)

Figure 9 shows the simulation result including the input/output terminals and the key nodes.

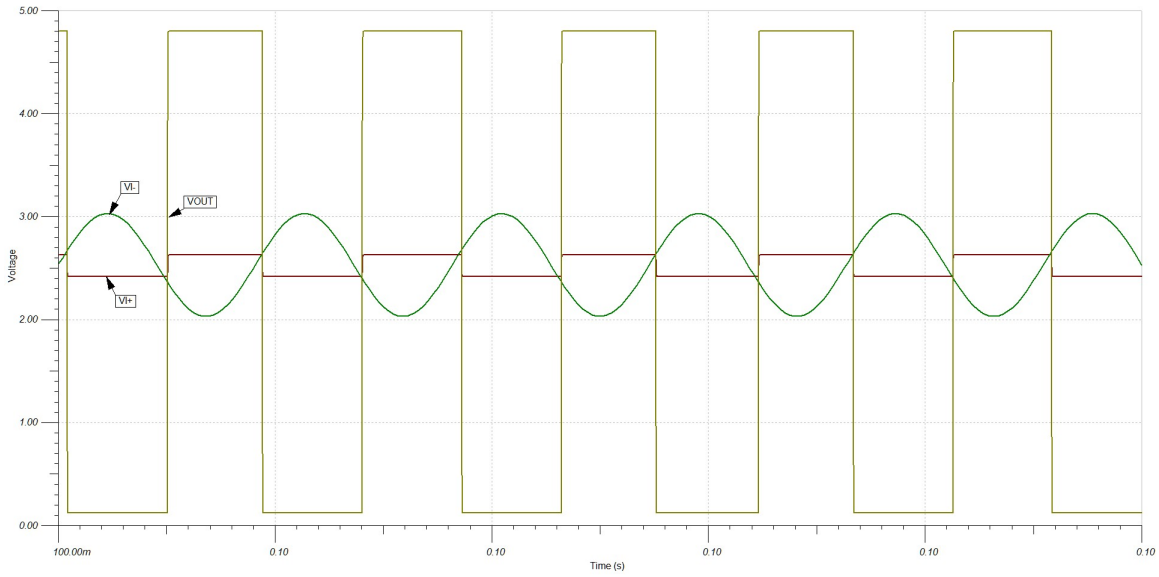

Figure 1-9. Simulation Waveforms

Design Notes

1. We have covered how the circuit works with equivalent circuits. The selection of the cutoff frequency f_0 is critical for the circuit to work. The simulation shows a working example which can serve as a starting point for further customization.
2. In the simulation example the cutoff frequency f_0 is set to 3.6 Hz, the V_{base} frequency to 0.5 Hz, and the input signal frequencies to 11 kHz.

Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See *Inverting Comparator With Hysteresis Circuit* (SNOA997) for more information about hysteresis.

See TINA-TI™ circuit simulation file for this circuit, SNOM706

See *Zero crossing detection using comparator circuit (Ground Referenced)* (SNOA999) for a ground-referenced zero crossing detector.

Design Featured Comparator

TLV7011	
V_S	1.6 V to 5.5 V
I_{CC}	5 µA
I_{sc}	65 mA
t_P	260 ns
I_b	5 pA
CMRR	78 dB
PSRR	78 dB
Theoretical f_{toggle}	1.7 MHz
TLV7011	

Design Alternate Comparator (lower power)

TLV7031	
V_S	1.6 V to 6.5 V
I_{CC}	315 nA
I_{sc}	29 mA
t_P	3 µs
I_b	2 pA
CMRR	73dB
PSRR	77 dB
Theoretical f_{toggle}	166 kHz
TLV7031	

Design Alternate Comparator (ultra-low power)

TLV3691	
V_S	0.9 V to 6.5 V
I_{CC}	75 nA
I_{sc}	42 mA
t_P	24 µs
I_b	8 pA
PSRR	< 54 dB
Theoretical f_{toggle}	11.6 kHz
TLV3691	

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