Relaxation oscillator circuit

Design Goals

<table>
<thead>
<tr>
<th>Supply</th>
<th>Oscillator Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{cc}$</td>
<td>$V_{ee}$</td>
</tr>
<tr>
<td>5V</td>
<td>0V</td>
</tr>
<tr>
<td></td>
<td>1 MHz</td>
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</table>

Design Description

The oscillator circuit generates a square wave at a selected frequency. This is done by charging and discharging the capacitor, $C_1$, through the resistor, $R_1$. The oscillation frequency is determined by the RC time constant of $R_1$ and $C_1$, and the threshold levels set by the resistor network of $R_2$, $R_3$, and $R_4$. The maximum frequency of the oscillator is limited by the toggle rate of the comparator and the capacitance load at the output. This oscillator circuit is commonly used as a time reference or a supervisor clock source.

Design Notes

1. Comparator toggle rate and output capacitance are critical considerations when designing a high-speed oscillator.
2. Select $C_1$ to be large enough to minimize the errors caused by stray capacitance.
3. If using a ceramic capacitor, select a COG or NPO type for best stability over temperature.
4. Select lower value resistors for the $R_2$, $R_3$, and $R_4$ resistor network to minimize the effects of stray capacitance.
5. $R_2$, $R_3$, and $R_4$ can be adjusted in order to create a duty cycle other than 50%.
Design Steps

1. When \( R_2 = R_3 = R_4 \), the resistor network sets the oscillator trip points of the non-inverting input at one-third and two-thirds of the supply.

\[
V_o = V_s \left( \frac{R_3}{(R_3 + R_2 + R_4)} \right) = \frac{2}{3} V_s = 3.33 V
\]

2. When the output is high, the upper trip point will be set at two-thirds of the supply to bring the output back low.

\[
V_o = V_s \left( \frac{-R_2}{(R_3 + R_2 + R_4)} \right) = \frac{1}{3} V_s = 1.67 V
\]

3. When the output is low, the lower trip point will be set at one-third of the supply in order to bring the output back high.

\[
V_c = V_s \left( 1 - e^{-\frac{t}{R_1 C_1}} \right)
\]

\[
\frac{1.67}{3.33} = 1 - e^{-\frac{t}{R_1 C_1}}
\]

\[
t = 0.69 R_1 C_1
\]

4. The timing of the oscillation is controlled by the charging and discharging rate of the capacitor \( C_1 \) through the resistor \( R_1 \). This capacitor sets the voltage of the inverting input of the comparator. Calculate the time to discharge the capacitor.

\[
V_c = V_s \left( 1 - e^{-\frac{t}{R_1 C_1}} \right)
\]

\[
\frac{1.67}{3.33} = 1 - e^{-\frac{t}{R_1 C_1}}
\]

\[
t = 0.69 R_1 C_1
\]

5. Calculate the time to charge the capacitor.

\[
V_i = V_c \left( 1 - e^{-\frac{t}{R_1 C_1}} \right)
\]

\[
\frac{1.67}{3.33} = 1 - e^{-\frac{t}{R_1 C_1}}
\]

\[
t = 0.69 R_1 C_1
\]

6. The time for the capacitor to charge or discharge is given by \( 0.69 R_1 C_1 \). With a target oscillator frequency of 1MHz, the time to charge or discharge should be 500ns.

\[
0.69 R_1 C_1 = 500 \text{ns}
\]

\[
R_1 C_1 = 724 \text{ns}
\]

7. Select \( C_1 \) as 100 pF and \( R_1 \) as 6.8kΩ (the closest real world value).
Design Simulations

Transient Simulation Results
Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See circuit spice simulation file, SBOMAO3.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, TI Precision Labs.

Design Featured Comparator

<table>
<thead>
<tr>
<th>TLV3201</th>
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</thead>
<tbody>
<tr>
<td>( V_{ss} )</td>
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<tr>
<td>( V_{inCM} )</td>
</tr>
<tr>
<td>( t_{pd} )</td>
</tr>
<tr>
<td>( V_{os} )</td>
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<tr>
<td>( V_{HYS} )</td>
</tr>
<tr>
<td>( I_q )</td>
</tr>
<tr>
<td>Output Type</td>
</tr>
<tr>
<td>#Channels</td>
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Design Alternate Comparator

<table>
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<tr>
<th>TLV7011</th>
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</thead>
<tbody>
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<tr>
<td>( V_{os} )</td>
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<tr>
<td>( I_q )</td>
</tr>
<tr>
<td>Output Type</td>
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<tr>
<td>#Channels</td>
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www.ti.com/product/tlv3201

www.ti.com/product/tlv7011
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